Intel® 820 Chipset Family: 82820 Memory Controller Hub (MCH)

Specification Update

January 2001

Notice: The Intel® 82820 MCH may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 290696-001

Contents

Revision History

Rev.	Draft/Changes	Date
-001	Initial Release	January 2001

Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents/Related Documents

Document Title	Document Number
Intel® 820 Chipset Family: 82820 Memory Controller Hub (MCH) datasheet	290630-002

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the Intel® 82820 MCH's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Identification via Programming Interface

Intel® 82820 MCH stepping can be identified by the following register contents:

Intel® 82820 MCH Stepping	Features	Vendor ID[1]	Device ID[2]	Revision Number[3]
B1	Note 3	8086h	2500 (device #0) 2501(device #0) 250B (device #0) 250F(device #1)	03
B2	Note 3	8086h	2500 (device #0) 2501(device #0) 250B (device #0) 250F(device #1)	04

NOTES:
1. The Vendor ID corresponds to bits 15-0 of the Vendor ID Register located at offset 00-01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15-0 of the Device ID Register located at offset 02-03h in the PCI function 0 configuration space.
3. **Device ID 2500:** Is the full SKU; **Device ID 2501**: UP only SKU; **Device ID 250B:** 266 & 300 MHz RDRAM only SKU (no SDRAM support).

Component Marking Information

The Intel® 82820 MCH may be identified by the following component markings:

Stepping	S-Spec	Top Marking	Notes
B1	SL3FT SL353 SL3NF	FW82820 FW82820DP FW82820	MCH UP Standard MCH DP Standard MCH PC600 Standard
B2	SL47D SL47F	FW82820 FW82820DP	MCH UP Standard MCH DP Standard

Summary Tables of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed MCH steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component, if the component is stepped in the future.
Fixed:	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This item is either new or modified from the previous version of the document.

Number	SPECIFICATION CHANGES
	There are no specification changes in this Specification Update revision

Number	Steppings			Plans	ERRATA
	B1	B2			
1	X	X		NoFix	AC'97 Snoop Cycle Delay by MCH
2	X	X		Fixed	Thermal Throttle
3	X	X		NoFix	Nap Pool Limitation
4	X	X		Fixed	2K Page Crossing Append May Corrupt Data
5	X	X		NoFix	Fast Write Append and Read Fence Failure Causes MCH to Hang
6	X	X		Fixed	SCK Tri-States during STR Entry Causing Failure Resuming from S3
7	X	X		Fixed	Missing Defer Reply May Occur under Certain Conditions
8	X	X		NoFix	RDRAM Counters/Timers Thermal Throttle May Throttle Incorrectly
9	X	X		NoFix	Illegal AGP Strobe Assertion

Number	SPECIFICATION CLARIFICATIONS
1	Multi-Bit Memory Error Clarification

Number	DOCUMENTATION CHANGES
	There are no documentation changes in this Specification Update revision

Specification Changes

There are no specification changes in this Specification Update revision.

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Errata

1. AC'97 Snoop Cycle Delay by MCH

Problem: Under heavy inbound ICH-to-Hub interface snooped traffic and heavy outbound processor-to-Hub interface traffic the MCH has been observed to delay the return of data to the Hub interface by as much ~80 µsec.

Implication: This MCH-to-Hub interface delay can result in a data under-run, which can cause an AC'97 timeout. However, no actual system failures have been reported. The impact to the end user is none or extremely low.

Workaround: None identified

Status: There are currently no plans to fix this erratum.

2. Thermal Throttle

Problem: The MCH will not always engage throttles correctly. If the programmable bandwidth (MTC register bits 30:17) threshold during the sampling window (DTC register bits 45:38) is exceeded, the MCH should engage throttles to protect the MCH from exceeding the package capabilities.
Definition: Engage throttles if bandwidth **(" >=")** threshold
Implementation: Engage throttles **("==")** threshold
Note: This issue only affects MCH weighted throttles, not RDRAM memory throttles.

Implication: The MCH sampling window not finite enough to always capture **("==")** threshold. A malicious software generating 100% toggle patterns could potentially exceed the maximum package capability of **3.3W**.

Workaround: None identified.

Status: Fixed in B2 stepping.

3. Nap Pool Limitation

Problem: The MCH may send an incorrect device ID with a NAP entry command that was caused by the NAP down timer expiring with following RDRAM power management (RPMR-53h) configurations:
4 devices in Pool A / 4 devices active.
2 devices in Pool A / 2 devices active.
Note: All other configurations work fine (1/1, 2/1, 4/1, 4/2, 4/3, 8/1, 8/2, 8/3, 8/4).

Implication: System is not stable using these particular configurations.

Workaround: Do not use 4/4 and 2/2 combinations or Disable NAP mode (i.e., Limited RDRAM power management set DNE=1)

Status: There are currently no plans to fix this erratum.

4. 2K Page Crossing Append May Corrupt Data

Problem: The MCH may incorrectly append two consecutive processor-to-AGP writes. This will happen when writes to the top QWord/DWord of a 2K page are followed by writes to the bottom of a non-contiguous 2K page.

Implication: Data corruption occurs on the system.

Workaround: BIOS can set the Append Disable bit to "1" (bit 1 in register offset FEh). When this bit is set, the MCH will not append AGP writes.

Status: Fixed in B-2 stepping.

5. Fast Write Append and Read Fence Failure Causes MCH to Hang

Problem: The MCH may hang if appendable processor-to-AGP 4X FW accesses are interspersed with AGP FRAME# read accesses.

Implication: The system may hang.

Workaround: BIOS can set the Append Disable bit to "1" (bit 1 in register offset FEh). When this bit is set, the MCH will not append AGP writes.

Status: There are currently no plans to fix this erratum.

6. SCK Tri-States during STR Entry Causing Failure Resuming from S3

Problem: The MCH tri-states SCK during STR entry causing a "glitch" on SCK. This "glitch" results in a protocol violation to the RDRAMs and the system will not resume. The MCH is much more susceptible to this problem when VDDQ = 1.5V.

Implication: The system will not resume from S3.

Workaround: Instead of using 56 Ω / 56 Ω SCK and CMD termination, terminate with a **91 Ω pull-up (to vterm) and a 39 Ω pull-down**. This is a stuffing change and does not require a board spin.

Status: Fixed in B2 stepping.

7. Missing Defer Reply May Occur under Certain Conditions

Problem: The MCH may stop responding to AGP FRAME# read cycles correctly if the following conditions are met:
- Heavy AGP FRAME# Traffic (reads and writes
- processor-to-AGP Reads
  and
- LPC, AC'97 traffic or processor locked cycles

Implication: Data corruption may occur or the MCH AGP interface may hang.

Workaround: None

Status: Fixed in B2 stepping.

8. RDRAM Counters/Timers Thermal Throttle May Throttle Incorrectly

Note: This RDRAM Counters/Timers Thermal Throttle is not the Thermal Throttle in Errata# 6 or the RDRAM On-die Thermal Sensor Throttle.

Problem: The RDRAM Counters/Timers-based thermal throttle mechanism does not function properly.

Implication: High temperature may reduce product longevity.

Workaround: Ensure proper airflow for cooling.

Status: There are currently no plans to fix this erratum.

9. Illegal AGP Strobe Assertion

Problem: When processor-to-AGP Fast Writes are being driven out and Write Appending is enabled, an AGP failure may occur resulting from an unexpected one clock assertion of AD strobe by the MCH during a processor wait state between Fast Write data blocks. The failure occurs only during Front Side Bus back-to-back cycles as a result of a specific sequence of writes:

- Two 32-byte (processor cache line) transfers.
- Two 8-byte transfers – all write appending (i.e., contiguous address stream).
- A 32-byte write to a non-contiguous address.

If this sequence of cycles occurs, the MCH may generate an illegal AD strobe assertion during a processor wait state.

Implication: During AGP Read or Write transactions, a data strobe occurring during a processor wait state may place incorrect data in the AGP data buffer which may cause the AGP card to hang.

Workaround: None identified. Write Appending, which is currently disabled for 820 MCH B1step for AGP Fast Writes, must remain disabled with B2 step.

Status: There are currently no plans to fix this erratum.

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Specification Clarifications

1. Multi-Bit Memory Error Clarification

When an Intel® 820 chipset platform is configured for ECC support, if a multi-bit uncorrectable memory error is detected during a memory read by a system device, an SERR, SCI, or SMI will be generated. This typically results in an NMI; however, bad data may still reach the intended target before the NMI can be generated or before NMI interrupt handler can service the problem. This may result in bad data being returned to the target and may be permanently stored, resulting in system data corruption. This chipset was not architected or designed to ensure that targets are protected from this corrupted data in these situations.

Documentation Changes

There are no documentation changes in this Specification Update revision.