# Intel® 840 Chipset: 82840 Memory Controller Hub (MCH)

## Specification Update

***January 2001***

**Notice:** The Intel® 840 chipset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 290697-001

# Contents

# Revision History

| Rev. | Draft/Changes | Date |
|---|---|---|
| -001 | Initial Release | January 2001 |

# Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

### Affected Documents/Related Documents

| Document Title | Document Number |
|---|---|
| *Intel® 840 Chipset: 82840 Memory Controller Hub (MCH)* | 298020-002 |

## Nomenclature

**Specification Changes** are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

**Errata** are design defects or errors. Errata may cause the Intel® 82840 MCH, behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

**Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

**Documentation Changes** include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

# Component Identification via Programming Interface

The 82840 MCH may be identified by the following register contents:

| Stepping | Vendor ID[1] | Device ID[2] | Revision Number[3] |
|---|---|---|---|
| B1 | 8086h | 1A21 (device #0, DP)<br>1A22 (device #0, QP)<br>1A23 (device #1)<br>1A24 (device #2) | 01h |
| B2 | 8086h | 1A21 (device #0, DP)<br>1A23 (device #1)<br>1A24 (device #2) | 02h |

**NOTES:**

1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00–01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15:0 of the Device ID Register located at offset 02–03h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

# Component Marking Information

The 82840 MCH may be identified by the following component markings:

| Stepping | S-Spec | Top Marking | Notes |
|---|---|---|---|
| B1 | Q881<br>SL3QR<br>SL3QT | FW82840-DP, Q881<br>FW82840-DP, SL3QR<br>FW82840-DP, SL3QT | Supports 2 way only. |
| B1 | Q878 | FW82840-QP, Q878 | Supports 4-way. |
| B2 | SL3TA | FW82840-DP, SL3TA | Supports 2 way only. |

# Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed 82840 MCH stepping. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

### Codes Used in Summary Table

| | |
|---|---|
| X: | Erratum, Specification Change or Clarification that applies to this stepping. |
| Doc: | Document change or update that will be implemented. |
| Fix: | This erratum is intended to be fix in a future stepping of the component. |
| Fixed: | This erratum has been previously fixed. |
| No Fix: | There are no plans to fix this erratum. |
| (No mark) or (Blank Box): | This erratum is fixed in listed stepping or specification change does not apply to listed stepping. |
| Shaded: | This item is either new or modified from the previous version of the document. |

| Number | SPECIFICATION CHANGES |
|---|---|
| 1 | MCH/MRH-R RDRAM Refresh Policy |

| Number | Steppings | | | Plans | ERRATA |
|---|---|---|---|---|---|
| | B1 | B2 | | | |
| 1 | X | X | | NoFix | MCH Hub Interface B Buffer Strength |
| 2 | X | X | | NoFix | Current Calibration |
| 3 | X | | | Fixed | Powerdown Exit |
| 4 | X | | | Fixed | Target Abort of PCI Device PAM Accesses |
| 5 | X | X | | NoFix | NAP Exit |
| 6 | X | X | | NoFix | AGP Fast Write Append and Read Fence Failure |
| 7 | X | X | | NoFix | AGP 2K Page Crossing Append |
| 8 | X | | | Fixed | 82840 MCH Error Address Segment |
| 9 | X | | | Fixed | 82840 MCH Processor Lock Read to AGP |
| 10 | X | X | | NoFix | SCK Tri-States during STR |
| 11 | X | X | | NoFix | Back-to-Back AGP Fast Writes |
| 12 | X | X | | NoFix | Split Lock Cycles |
| 13 | X | X | | NoFix | CTM Detect Bit |
| 14 | X | X | | NoFix | System Interface Voltage Level |
| 15 | X | | | Fixed | False ECC Error |
| 16 | X | X | | NoFix | Lock Cycle Hang |
| 17 | X | X | | NoFix | MRH-R Stick Channel Swap |
| 18 | X | | | Fixed | Missing Defer Reply Occurs under Certain Conditions |
| 19 | X | X | | NoFix | Hub Interface B Spurious Request |
| 20 | X | X | | NoFix | Suspend to RAM (S3) Entry |
| 21 | X | X | | NoFix | Nap Failure |
| 22 | X | X | | NoFix | Illegal AGP Strobe Assertion |

| Number | SPECIFICATION CLARIFICATIONS |
|---|---|
| 1 | Multi-Bit Memory Error Clarification |
| 2 | IIO Bit Cleared Prematurely |

| Number | DOCUMENTATION CHANGES |
|---|---|
| | There are no documentation changes in this Specification Update revision |

# Specification Changes

## 1. MCH/MRH-R RDRAM Refresh Policy

The 82840 MCH may hang under heavy memory traffic with an MRH-R, with the following configuration:

1. The system bus is running at 133 MHz,
2. Both stick channels of each MRH-R are populated,
3. The default channel refresh policy is used with the MRH-R.

This affects only the 82840 with MRH-R memory configurations, and requires the following workaround:

In MCH register offset 9Fh, device 0, set bit 7 to “1.” This bit changes the channel refresh policy in the MRH-R configuration.

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# Errata

### 1. MCH Hub Interface B Buffer Strength

**Problem:** The 82840 MCH hub interface B and host interface buffer strength is set to the maximum strength.

**Implication:** This issue could affect signal integrity quality. No system failures have been seen as a result of this issue.

**Workaround:** None identified.

**Status:** There are currently no plans to fix this erratum.

### 2. Current Calibration

**Problem:** The 82840 MCH drives the RDRAM DQB signals following current calibration operation.

**Implication:** This may interfere with the current calibration activity that is occurring simultaneously. This issue only affects designs with memory repeater hubs, MRH-R.

**Workaround:** Current calibration should be disabled when using the MRH-R.

**Status:** There are currently no plans to fix this erratum.

### 3. Powerdown Exit

**Problem:** At 400 MHz, the 82840 MCH issues incorrect powerdown exit command to the RDRAM channels. All powerdown exit commands from the MCH will be issued to device 0.

**Implication:** Systems with either RIMM-only or MRH-Rs will not be able to access any device that was powered down with device ID other than 0.

**Workaround:** BIOS can issue the powerdown exit command to the RDRAM devices through the broadcast mechanism. This will allow the RDRAM device to exit powerdown during memory setup.

**Status:** This erratum was fixed in the B2 stepping.

### 4. Target Abort of PCI Device PAM Accesses

**Problem:** The 82840 MCH will target abort all PCI devices that issue transactions directly to the PAM region.

**Implication:** This will affect PCI devices that attempt to access the PAM region during boot time. These devices will not function correctly during boot time. It is known that some PCI cards and legacy USB devices can attempt to access the PAM region to enable functionality during boot time. The number of devices that generate these types of accesses is a small subset of the total PCI devices available in the market.

**Workaround:** Move the legacy BIOS USB data area into the base 640KB of system memory and use BIOS memory resource reporting mechanisms to prevent the operating system from using this memory resource. There is no workaround for the PCI devices.

**Status:** This erratum was fixed in the B2 stepping.

### 5. NAP Exit

**Problem:** At 400 MHz, the 82840 MCH incorrectly issues the NAP exit command to RDRAM devices. All NAP exit commands issued by the MCH appears on the channel as a transaction to device 0.

**Implication:** This issue will affect both RIMM-only and MRH-R systems. System BIOS cannot access devices that are placed in NAP mode with a serial device ID greater than 0.

**Workaround:** None identified. The NAP feature should not be used.

**Status:** There are currently no plans to fix this erratum.

### 6. AGP Fast Write Append and Read Fence Failure

**Problem:** The MCH may hang if appendable processor-to-AGP 4X FW accesses are interspersed with AGP FRAME# read accesses.

**Implication:** The system may hang.

**Workaround:** BIOS can set the append disable bit to ‘1’ (bit 21, register offset F4-F6h). When this bit is set, the MCH will not append AGP writes.

**Status:** There are currently no plans to fix this erratum.

### 7. AGP 2K Page Crossing Append

**Problem:** The MCH may incorrectly append two consecutive processor-to-AGP writes. This will happen when writes to the top Qword/Dword of a 2K page are followed by writes to the bottom 2K page (non-contiguous).

**Implication:** Data corruption occurs on the system.

**Workaround:** BIOS can set the append disable bit to ‘1’ (bit 21, register offset F4-F6h ). When this bit is set, the MCH will not append AGP writes.

**Status:** There are currently no plans to fix this erratum.

### 8. 82840 MCH Error Address Segment

**Problem:** The MCH posts the wrong value in the “Error Segment Address” bit of the EAP debug register when a single bit ECC error occurs on the third QWord of a cache line.

**Implication:** Software will not be able to tell whether the ECC error was attributed to channel A or channel B. However, software can still determine single bit ECC error events and the 4 KB memory block of which the error occurred.

**Workaround:** None identified.

**Status:** This erratum was fixed in the B2 stepping.

### 9. 82840 MCH Processor Lock Read to AGP

**Problem:** An AGP deadlock will occur during a locked processor-to-AGP read cycle under the following sequence:

- Heavy processor-to-AGP traffic must exist.
- An AGP device launches an AGP high-priority read to two or more cache lines.
- A snoopable read or write access to system memory is received (e.g., PCI FRAME transaction), which propagates up from AGP, hub interface A or hub interface B. This cycle must access, or prefetch into, one of the cache lines being requested by the AGP high priority read generated in sequence #2, above.
- The processor issues a locked read toward AGP.

**Implication:** The OS/driver must allow sequence 2 and 3 to access the same page. This combination conditions and sequence will cause the system to hang.

**Workaround:** None identified

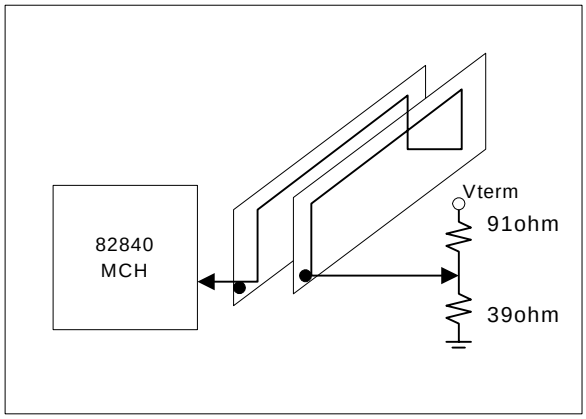
**Status:** This erratum was fixed in the B2 stepping.

### 10. SCK Tri-States during STR

**Problem:** The MCH tri-states SCK during STR entry causing a “glitch” on SCK. This “glitch” results in a protocol violation to the RDRAM devices and the system will not resume.

**Implication:** The system will not resume from the S3.

**Workaround:** Instead of using 56 Ω/56 Ω, SCK and CMD should be terminated with 91 Ω pull-up resistor (to Vterm) and 39 Ω pull-down resistor. These are new termination values. **These termination values are applicable for all memory configurations including RIMM and MRH-R (expansion channel).**




**Status:** There are currently no plans to fix this erratum.

### 11. Back-to-Back AGP Fast Writes

**Problem:** The MCH may hang if appendable back-to-back fast write cycles are issued to an AGP device.

**Implication:** The system may hang.

**Workaround:** BIOS can set the append disable bit to ‘1’ (bit 21, register offset F4-F6h). When this bit is set, the MCH will not append AGP writes.

**Status:** There are currently no plans to fix this erratum.

### 12. Split Lock Cycles

**Problem:** When two locked cycles to a write-only PAM region are issued and are followed by 2 writes to the same region (these are redirected to DRAM) the MCH will lock up.

**Implication:** The system may hang.

**Workaround:** BIOS should not issue locked cycles to write-only PAM regions during boot time.

**Status:** There are currently no plans to fix this erratum.

### 13. CTM Detect Bit

**Problem:** The CTM detection bit can be set incorrectly if the CTM clock is not present.

**Implication:** BIOS will not be able to isolate the levelization failure related to improperly installed CRIMMs or RIMMs.

**Workaround:** The status of the CTM detection bit is unreliable and should not be checked by BIOS.

**Status:** There are currently no plans to fix this erratum.

### 14. System Interface Voltage Level

**Problem:** Under high toggle rate conditions the system interface Voh may only reach 1.4V. The internal n-clamps on these signals are not functioning correctly.

**Implication:** This low voltage swing will decrease margin on the system interface.

**Workaround:** BIOS can disable the n-clamp on the MCH system interface.

**Status:** There are currently no plans to fix this erratum.

### 15. False ECC Error

**Problem:** The MCH can incorrectly report an ECC single bit error in QW0 or QW2 when the MCH is running in ECC Mode or ECC Mode with hardware scrubbing. This incorrect reporting is isolated to the first ECC bit transported on the DQB8 signal in either QW0 or QW2.

**Implication:** False single bit errors can be reported by the MCH.

**Workaround:** This isolated ECC error can be filtered by BIOS.

**Status:** This erratum was fixed in the B2 stepping.

### 16. Lock Cycle Hang

**Problem:** The problem occurs when the processor issues two consecutive lock cycles directed toward the P64H (or ICH). During the first lock cycle, the MCH must have at least 6 memory read transactions posted by the P64H (or ICH) and an ICH DMA transaction in progress. This ICH DMA must be targeted toward main memory by the 8237 DMA controller in the ICH, an LPC SIO device, or ISA device.

**Implication:** The above conditions will lead to system lockup. The conditions required for this erratum to occur appear to be unlikely in actual PC systems. In many hours of testing on a number of actual PC systems, Intel did not observe this erratum. However, customers should be aware of this erratum and determine its potential applicability to their system configuration.

**Workaround:** None identified.

**Status:** There are currently no plans to fix this erratum.

### 17. MRH-R Stick Channel Swap

**Problem:** When the MCH Stick Channel Swap feature (Device 0, Function 0, Register 97h, Bit 6) is enabled the MCH can incorrectly swap stick channel operations during data transfers. This issue only occurs when the MCH Rambus interface is operating at 400 MHz.

**Implication:** This causes the MCH to receive incorrect data when operating in this mode. This erratum does not affect MCH Stick Channel Swap feature when the MCH Rambus interface is operating at 300 MHz.

**Workaround:** Do not enable this stick channel swap feature when the MCH Rambus interface is operating at 400 MHz.

**Status:** There are currently no plans to fix this erratum.

### 18. Missing Defer Reply Occurs under Certain Conditions

The 82840 MCH may stop responding to AGP FRAME# read cycles if the following conditions occur:

- Heavy AGP FRAME# traffic (reads and writes)
- Processor -to-AGP reads
- Heavy PCI, LPC, AC'97, traffic or processor Lock cycles

**Implication:** Data corruption may occur on AGP FRAME# reads.

**Workaround:** There are two possible workarounds to this erratum:

- Disable Hub Interface A Combining, and AGP Write Streaming by writing a "1" to register F4h, bits 19 & 20.
- Disable AGP Read Snoop Ahead by writing a "1" to register F4h, bit 0.

***Note:*** Workaround #2 could have a performance impact on AGP.

## MCHTST – MCH Test Register

| | |
|---|---|
| PCI Device | 0 |
| Address Offset | F4-F6h |
| Default | RO R/W |
| Size | 32 bit |
| Default | 00F874h |

| Bit Field | Default & Access | Description |
|---|---|---|
| [31:22] | RO | Reserved |
| [21] | R/W | **Append Disable** – When this bit is set to "1", the MCH will not append AGP writes. When this bit is set to "0" (default), write append is enabled. |
| [20] | R/W | **Hub Interface A Write Combining (HLWCD**) – When this bit is set to "1", Write Combining is disabled for Host Bus Writes targeting the Hub Interface A. When this bit is a "0" (default), Write Combining is enabled. |

| Bit Field | Default & Access | Description |
|---|---|---|
| [19] | R/W | **AGP Write Streaming (AGPWSD)** – When this bit is set to "1", AGP Write Streaming is disabled. When this bit is a "0" (default), AGP Write Streaming is enabled. |
| [18:1] | R/O | Reserved |
| [0] | R/W | **Read Snoop Ahead Disable (RSAD)** – When this bit is a "1", the MCH will snoop 1 cache line, read the line and then disconnect the transfer at the line boundary. When this bit is a "0" (default), the normal operation of AGP read is performed. |

**Status:** This erratum was fixed in the B2 stepping.

### 19. Hub Interface B Spurious Request

**Problem:** In an Intel 840 chipset platform, upon a power-up cycle, it has been observed that a spurious initialization cycle request may be initiated on the Hub Interface B when the system does not support the P64H component.

**Implication:** An initialization cycle on the Hub Interface B, without a P64H, may result in the MCH interpreting a cycle request from the Hub Interface B. This will result in a system hang.

**Workaround:** Place a pull-up resistor on the HLB17 signal of the MCH to insure no spurious requests from the Hub Interface B. The pull-up resistor value range is 65 KΩ to 110 KΩ, and should be pulled up to 1.8 V.

**Status:** There are currently no plans to fix this erratum.

### 20. Suspend to RAM (S3) Entry

**Problem:** In the Intel 840 MCH, a boundary condition between the "S3" (Suspend to RAM) State entry and a regularly scheduled refresh request causes the bank counter to miss an increment, leaving some banks in a non-precharged state. As a result these banks are not refreshed during the S3 state. This issue affects the Intel 840 MCH to RIMMs, or 840 MCH to MRH-R systems only.

**Implication:** This issue may cause data corruption and/or system hang upon resume from a power-down state (S3/STR).

**Workaround:** The system BIOS can insure that all banks are closed before executing the memory power down sequence. There are currently no plans to fix this erratum.

### 21. NAP Failure

**Problem:** With NAP mode enabled the MCH may hang, causing an infinite number of random cycles to be issued to the memory interface.

**Implication:** NAP mode is not functional. System may hang if NAP mode is enabled.

**Workaround:** None identified. NAP mode, which is currently disabled in 82840 MCH B1 silicon, must remain disabled with B2 silicon.

**Status:** There are currently no plans to fix this erratum.

## 22. Illegal AGP Strobe Assertion

**Problem:** When processor-to-AGP Fast Writes are being driven out and Write Appending is enabled, an AGP failure may occur resulting from an unexpected one clock assertion of AD strobe by the MCH during a processor wait state between Fast Write data blocks. The failure occurs only during Front Side Bus back-to-back cycles as a result of a specific sequence of writes:

- Two 32-byte (processor cache line) transfers.
- Two 8-byte transfers – all write appending (i.e. contiguous address stream).
- A 32-byte write to a non-contiguous address.

If this sequence of cycles occurs, the MCH may generate an illegal AD strobe assertion during a processor wait state.

**Implication:** During AGP Read or Write transactions, a data strobe occurring during a processor wait state may place incorrect data in the AGP data buffer which may cause the AGP card to hang.

**Workaround:** None identified. Write Appending, which is currently disabled in 82840 MCH B1 silicon for AGP Fast Writes, must remain disabled with B2 silicon.

**Status:** There are currently no plans to fix this erratum.

# Specification Clarifications

## 1. Multi-Bit Memory Error Clarification

**Issue:** When an 840 chipset platform is configured for ECC support, if a multi-bit uncorrectable memory error is detected during a memory read by a system device, an SERR, SCI, or SMI will be generated. This typically results in an NMI. However, bad data may still reach the intended target before the NMI can be generated or before NMI interrupt handler can service the problem. This may result in bad data being returned to the target and may be permanently stored, resulting in system data corruption. This chipset was not architected or designed to ensure that targets are protected from this corrupted data in these situations.

## 2. IIO Bit Cleared Prematurely

**Issue:** Following SETF, SETR or CLRR commands, the IIO bit (Initiate Initialization Operation) is polled by software and cleared by the MCH. By clearing the IIO bit, the MCH indicates that it is safe to issue the next IOP command. If the IOP command is sent within 1 µs of IIO clear, the SIO command may be corrupted on the CMOS bus, which could result in a failure during RDRAM Initialization.

NOTE: If the Intel® 840 BIOS Reference Code has been followed, the delay between IIO bit clear and the next IOP command will always be greater than 1µS. To insure that commands are not sent during the 1µs “at risk” window, insure that there is at least a 1µS delay loop in the “poll for IIO clear” routine in BIOS.

# Documentation Changes

There are no documentation changes in this Specification Update revision.