Intel® 440LX AGPset: 82443LX PAC

Specification Update

January 2001

Notice: Intel® 440LX AGPset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 297655-005

Contents

Revision History

Rev.	Draft/Changes	Date
-001	Initial Release	October 1997
-002	Added Specification Change #1 and Documentation Change #1	April 1998
-003	Added Specification Change #1 and Documentation Change #1	August 1998
-004	Added SLKN to Component Markings. Added Specification Clarification #2	April 2000
-005	Editorial and formatting changes only. No technical information changes.	January 2001

Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents/Related Documents

Document Title	Document Number
Intel® 440LX AGPset: 82443LX PAC datasheet	290564-002

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the Intel 82443LX PAC behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Identification via Programming Interface

The Intel 82433LX PAC may be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
A-3	8086h	7180h	03h

NOTES:
1. The Vendor ID corresponds to bits 15-0 of the Vendor ID Register located at offset 00-01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15-0 of the Device ID Register located at offset 02-03h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7-0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

Intel® 82443LX (PAC)

Stepping	S-Spec	Top Marking	Freq.	Notes
A-3	SL2KK	FW82443LX SL2KK	66	Production
A-3	SL2KN	FW82443LX SL2KN	66	Production – tape and reel remnant

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed Intel 82443LX PAC steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This item is either new or modified from the previous version of the document.

Number	SPECIFICATION CHANGES
1	x4 and x32 SDRAM DIMM Not Supported
2	Intel® 440LX AGPset Identification Test Mode

Number	Steppings		Plans	ERRATA
	A3			
1	X		NoFix	Hard Reset Failure with EDO ECC DRAM
2	X		NoFix	Hard Reset Failure with SDRAM
3	X		NoFix	No SERR# Generation above 4 Gbytes
4	X		NoFix	Clock Throttling Not Supported in Intel® 440LX AGPset
5	X		NoFix	IOQ Depth of 1 Not Supported
6	X		NoFix	PCI to AGP Writes When SMM Is Programmed OPEN
7	X		NoFix	x32/x8 SDRAM Support in 3 DIMM Design

Number	SPECIFICATION CLARIFICATIONS
1	EDO/SDRAM Timing Performance Summaries
2	Multi-Bit Memory Error Clarification

Number	DOCUMENTATION CHANGES
1	PAC Configuration Register: Reinstate Bit 11, Bit 14 Now Reserved
2	DRAM Memory: Buffered/Unbuffered EDO Support

Specification Changes

1. x4 and x32 SDRAM DIMM Not Supported

The 82443LX PAC no longer supports x4 or x32 SDRAM DIMM. Support for the x4 and x32 SDRAM DIMM has been dropped because the older technology x4 configuration has not been included in the *Intel 4 Clock 66 MHz Unbuffered SDRAM DIMM Specification*, and due to lack of availability neither x4 or x32 SDRAM DIMM have been validated on 82443LX platforms.

Therefore, in the datasheet, replace Table 14, *Minimum (Upgradeable) and Maximum Memory Size for Each Configuration*, page 86, with the following:

Minimum (Upgradeable) and Maximum Memory Size for Each Configuration

DRAM Tech.	DRAM Depth	DRAM Width	DRAM DIMM		DRAM Addressing	Address Size		DRAM Array Size			
			SD	DD		Row	Col	Config #1		Config #2	
4M EDO	1M	4	1Mx72	2Mx72	Symmetric	10	10	8 MB	128 MB[4]	---	---
16M EDO	1M	16	1Mx72	2Mx72	Symmetric	10	10	8 MB	128 MB	8 MB	96 MB
16M EDO	1M	16	1Mx72	2Mx72	Asymmetric	12	8	8 MB	128 MB	8 MB	96 MB
16M EDO	2M	8	2Mx72	4Mx72	Asymmetric	11	10	16 MB	256 MB	16 MB	192 MB
16M EDO	2M	8	2Mx72	4Mx72	Asymmetric	12	9	16 MB	256 MB	16 MB	192 MB
16M EDO	4M	4	4Mx72	8Mx72	Symmetric	11	11	32 MB	512 MB[4]	---	---
16M EDO	4M	4	4Mx72	8Mx72	Asymmetric	12	10	32 MB	512 MB[4]	---	---
64M EDO	2M	32	2Mx72	4Mx72	Asymmetric	11	10	16 MB	256 MB	16 MB	192 MB
64M EDO	2M	32	2Mx72	4Mx72	Asymmetric	12	9	16 MB	256 MB	16 MB	192 MB
64M EDO	2M	32	2Mx72	4Mx72	Asymmetric	13	8	16 MB	256 MB	16 MB	192 MB
64M EDO	4M	16	4Mx72	8Mx72	Symmetric	11	11	32 MB	512 MB	32 MB	384 MB
64M EDO	4M	16	4Mx72	8Mx72	Asymmetric	12	10	32 MB	512 MB	32 MB	384 MB
64M EDO	8M	8	8Mx72	16Mx72	Asymmetric	12	11	64 MB	1 GB[3]	64M	384 MB
64M EDO	16M	4	16Mx72	32Mx72	Symmetric	12	12	128 MB	1 GB[3]	---	---
16M[1] SDRAM[1]	1M	16	1Mx72	2Mx72	Asymmetric	11	8	8 MB	128 MB	8 MB	96 MB
16M[1] SDRAM[1]	2M	8	2Mx72	4Mx72	Asymmetric	11	9	16 MB	256 MB	16 MB	192 MB
64M[1] SDRAM[1]	4M	16	4Mx72	8Mx72	Asymmetric	11	10	32 MB	512 MB	32 MB	384 MB
64M[1] SDRAM[1]	4M	16	4Mx72	8Mx72	Asymmetric	13	8	32 MB	512 MB	32 MB	384 MB

Minimum (Upgradeable) and Maximum Memory Size for Each Configuration

DRAM Tech.	DRAM Depth	DRAM Width	DRAM DIMM		DRAM Addressing	Address Size		DRAM Array Size			
			SD	DD		Row	Col	Config #1		Config #2	
64M[1] SDRAM[1]	8M	8	8Mx72	16Mx72	Asymmetric	13	9	64 MB	512 MB	64 MB	384 MB
64M[2] SDRAM[1]	4M	16	4Mx72	8Mx72	Asymmetric	12	8	32 MB	512 MB	32 MB	384 MB
64M[2] SDRAM[1]	8M	8	8Mx72	16Mx72	Asymmetric	12	9	64 MB	512 MB	64 MB	384 MB

NOTES:
1. 2-bank SDRAM DIMMs
2. 4-bank SDRAM DIMMs
3. 1-GB memory array is achieved by using Double-Sided Buffered EDO DIMMs.
4. Single-sided DIMMs only

2. Intel® 440LX AGPset Identification Test Mode

This procedure describes a new method of identifying the 82443LX chip using Automated Test Equipment (ATE) board level testing.

Activation of the Test Mode

- Drive ‘1’ on MECC5, MECC6, TEST, RSTIN#.
- Drive “0000” on GNT[3:0] signals, drive 0’s on MECC4-MECC0, MECC7, PCLKIN and HCLKIN.
- Drive HCLKIN 16 clock cycles.
- Drive “0” on RSTIN# and then drive HCLKIN 16 clock cycles.
- Drive “1” on RSTIN#, then drive HCLKIN, PCLKIN 200 clock cycles
- Observe the signature.

Signature Observation

Once the chip is in test mode, the following output signals become observability signals.

Device ID = 7180h (i.e., 0111_0001_1000_0000)

Revision ID = 03h (only last two bits are displayed on GGNT# and ST[2]); this value varies with revision ID.

Vendor ID is not visible on 82443LX chip.

82443LX Pin Name	Bit Displayed	Bit Value
MAA[13]	Dev ID(0)	0
WE[0]	Dev ID(1)	0
WE[1]	Dev ID(2)	0
WE[2]	Dev ID(3)	0
WE[3]	Dev ID(4)	0
SRAS[0]#	Dev ID(5)	0
SRAS[1]#	Dev ID(6)	0
SRAS[2]#	Dev ID(7)	1
SRAS[3]#	Dev ID(8)	1
SCAS[0]#	Dev ID(9)	0
SCAS[1]#	Dev ID(10)	0
SCAS[2]#	Dev ID(11)	0
SCAS[3]#	Dev ID(12)	1
WSC#	Dev ID(13)	1
ST[0]	Dev ID(14)	1
ST[1]	Dev ID(15)	0
ST[2]	Rev ID(0)	1
GGNT#	Rev ID(1)	1

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Errata

1. Hard Reset Failure with EDO ECC DRAM

Problem: PAC continues to drive CAS# and RAS# active after PCIRST# is asserted. This causes ECC EDO DRAMs to drive MECC[7:0] signals. These MECC[7:0] signals are sampled on the rising edge of PCIRST# and can cause PAC to enter into manufacturing test mode if these bits match certain bit patterns. MECC[7:0] signals must be driven to all 0s to enter into normal operation mode.

Implication: PAC enters manufacturing test mode and the system will not function properly.

Workaround: Invert PCIRST# signal and connect it to the output enable (OE#) pin on the DIMM. This tri-states the outputs of EDO DRAM when PCIRST# is asserted and the internal pull-downs on MECC[7:0] signals pull these signals low. This ensures the proper behavior.

Status: There are no plans to fix this erratum.

2. Hard Reset Failure with SDRAM

Problem: A condition similar to previous errata (#11) occurs with SDRAMs if CKE is driven low during reset. In this situation manufacturing test mode is invoked.

Implication: PAC enters manufacturing test mode and the system will not function properly.

Workaround: Invert PCIRST# signal and connect it to the output enable of tri-state buffer that drives the CKE signal to the DIMM. Also, place 8.2 KΩ pull-ups to 3.3V on each of the CKE signals on the DRAM side of the buffer. This workaround ensures that CKE signals on the DRAM side is pulled high during reset.

Status: There are no plans to fix this erratum.

3. No SERR# Generation above 4 GB

Problem: AGP sideband protocol allows for encoding of address bits A[35:0]. This allows for addresses above 4 GBs. PAC ignores all address bits above bit 31. Thus, bits A35:32 are ignored by the PAC and no SERR# is generated for out of aperture addressing.

Implication: ISVs and device driver writers cannot use SERR# as an indicator of code jumps or other accesses above 4 GB.

Workaround: None Identified.

Status: There are no plans to fix this erratum. ISVs and device driver writers should not use SERR# as an indicator of code jumps above 4 GB.

4. Clock Throttling Not Supported in Intel® 440LX AGPset

Problem: In systems that support clock throttling, PIIX4 asserts stop clock (STPCLK#) to the processor. Processor sends Stop Grant acknowledge cycle which is deferred by the PAC. PAC then completes the cycle on the PCI bus (PIIX4) and is then suppose to complete the defer acknowledge to the processor. In Intel® 440LX AGPset systems, if there is high priority AGP traffic, then PAC may not be able to complete the defer acknowledge cycle until the AGP cycles are completed.

When PIIX4 receives the Stop Grant acknowledge cycle and STPCLK# low time is reached, PIIX4 deasserts STPCLK#. It then re-asserts STPCLK# at the end of the clock throttle period. If the processor does not see the Stop Grant acknowledge cycle (defer acknowledge) until after the STPCLK# is re-asserted, it goes into Stop Grant state and will not issue another Stop Grant acknowledge cycle. PIIX4 not receiving another Stop Grant acknowledge cycle will keep the STPCLK# low.

Implication: The system remains in the Stop Grant state.

Workaround: Do not enable manual (BIOS) or thermal (tying the THRM# pin high) clock throttling as defined by PIIX4.

Status: There are no plans to fix this erratum.

5. IOQ Depth of 1 Not Supported

Problem: When AGP Master does frame-based memory read from the DRAM and PAC is in the process of completing the configuration cycle, a system hang may occur if the IOQ Depth is programmed to 1.

Implication: This may result in no defer reply being given to the processor, or the AGP read cycle may not complete, or PAC may give snoop stalls on the system bus.

Workaround: IOQ Depth must be programmed to 4.

Status: There are no plans to fix this erratum.

Note: During BIST the IOQ Depth value changes to 1. Refer to the BIOS workaround to change this value back to 4 after BIST.

6. PCI to AGP Writes When SMM Is Programmed OPEN

Problem: If the SMM space is programmed as OPEN by setting bit 6 in register 72h (Dev 00h), and a PCI master does a write to VGA space when VGA is located on AGP, the PAC will hang.

Implication: This scenario is unlikely to actually happen in a real system because the SMM space would only be OPEN during boot-up to load the SMM code and data into SMM space. The space would then be locked down and could only be accessed during an SMI event.

Workaround: Software should NOT enable PCI masters to write to VGA space while SMM is programmed as OPEN.

Status: There are no plans to fix this erratum.

7. x32/x8 SDRAM Support in 3 DIMM Design

Problem: For a 3 DIMM (Configuration #2) SDRAM design, the memory interface of PAC can not support a combination of x32 SDRAM DIMM on slot#3 (the closest DIMM socket to the PAC and is driven by MAB copy), and x8 SDRAM DIMM on slot#1 or/and slot #2.

Implication: If an 82443LX system violates this rule in a 3 DIMM SDRAM design, it can potentially encounter data corruption or intermittent hang.

Workaround: Do not use a combination of x32 DIMM on slot#3 and x8 DIMM on slot#1 or/and slot #2 in the Intel® 440LX AGPset system at the same time.

Status: There are no plans to fix this erratum.

Note: This restriction does not apply to EDO DIMM in a 3 DIMM configuration, it also does not affect 4 DIMM configuration at all.

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Specification Clarifications

1. EDO/SDRAM Timing Performance Summaries

Replace Table 18, *CPU-to Main Memory Performance Summary*, with the following:

DRAM Timing Relationships with Register Settings

This section shows the DRAM timing relationship with respect to bit settings in the DRAM Timing (DRAMT) register (address offset 58h). The values in this register affect both leadoff and burst timings. The processor to DRAM memory read performance summary for EDO and SDRAM are shown below.

Notes

1. PH is page hit.
2. RM is row miss.
3. PM is page miss.
4. The leadoff clock counts of a back-to-back burst cycle is also shown as a pipeline leadoff.
5. All leadoff counts will add one more clock when ECC is enabled.

EDO Timing Performance Summary

Possible Valid Setting	Affect Leadoff			Leadoff Clock Count		Burst Clock Count [4]	
	RCD [1] 1 (2 clocks) 0 (3 clocks)	MAWS [5] 1 (fast) 0 (slow)	RPT [6] 1 (3 clocks) 0 (4 clocks)	First Leadoff (PH/RM[2]/RM[3]/ PM)	Pipeline Leadoff (PH/RM[3]/PM)	Read	Write
a	0	1	1	8/10/11/13	2/6/8	222 or 333	222 or 333
b	0	1	0	8/10/11/14	2/6/9	222 or 333	222 or 333
c	0	0	1	9/12/13/15	3/7/9	222 or 333	222 or 333
d	0	0	0	9/12/13/16	3/7/10	222 or 333	222 or 333

NOTES:

1. RAS to CAS delay, RCD (bit 1 of Register DRAMT), is always set to 0 for a 3 clock delay to have a positive tRAC margin.
2. Row miss numbers assume that no RAS# is currently active.
3. One more clock should be added if the current RAS# has to be negated and the new RAS# has to be asserted.
4. The EDO burst timing is also determined by the setting DRAMT bits [3,4].
5. MAWS is the EDO Memory Address Wait State. The setting of MAWS affects all cases. When MAWS is set to 0 (slow), an extra clock is added for each CAS# and RAS# assertion.
6. RPT is EDO RAS Precharge time. This only affects a page miss.

SDRAM Timing Performance Summary

Possible Valid Setting	Affects Leadoff			Leadoff Clock Count		Burst Clock Count
	SCLT [1] 1 (2 clocks) 0 (3 clocks)	SRCD [2] 1 (2 clocks) 0 (3 clocks)	SRPT [3] 1 (2 clocks) 0 (3 clocks)	First Leadoff PH/RM [4]/RM [5] /PM	Pipeline Leadoff PH/RM [6]/PM	Read & Write
a	1	1	1	8/10/11/12	2/4/5	111
b	1	1	0	8/10/11/13	2/4/6	111
c	0	1	1	9/11/12/13	1/5/6	111
d	1	0	1	8/11/12/13	2/5/6	111
e	0	1	0	9/11/12/14	1/5/7	111
f	0	0	0	9/12/13/15	1/6/8	111
g	1	0	0	8/11/12/14	2/5/7	111
h	0	0	1	9/12/13/14	1/6/7	111

NOTES:

1. SCLT is SDRAM CAS Latency. The setting of SCLT affects all cases (page hit, page miss, and row miss).
2. SRCD is SDRAM RAS to CAS delay. The setting of this bit affects both page miss and row miss.
3. SRPT is SDRAM RAS precharge time. The setting of this bit affects only page miss.
4. Row miss numbers assume that no RAS# is currently active.
5. Row miss numbers assume that the current RAS# has to be negated and the new RAS# has to be asserted.
6. The same MAWS control bit for EDO timing in register 58h of PAC (device 0) has a different timing effect for SDRAM. All the clock counts are based on MAWS = 1 (fast). When MAWS = 0 (slow), an extra clock is added before each CS# assertion.

2. Multi-Bit Memory Error Clarification

When an Intel® 440LX AGPset platform is configured for ECC support, if a multi-bit uncorrectable memory error is detected during a memory read by a system device, an SERR, SCI, or SMI will be generated. This typically results in an NMI; however, bad data may still reach the intended target before the NMI can be generated or before NMI interrupt handler can service the problem. This may result in bad data being returned to the target and may be permanently stored, resulting in system data corruption. This chipset was not architected or designed to ensure that targets are protected from this corrupted data in these situations.

Documentation Changes

1. PAC Configuration Register: Reinstate Bit 11, Bit 14 Now Reserved

In Section 3.3.12, *PACCFG-PAC Configuration Register (Device 0),* offset 50-51h, page 41, replace register description with the following:

PACCFG—PAC Configuration Register (Device 0)

Offset: 50–51h
Default: 0s00_s000_0000_0s00b
Access: Read/Write, Read Only

The PACCFG is a 16-bit register that is used for indicating the system level configuration

Bit	Description
15	**WSC# Handshake Disable—R/W.** This bit disables the internal WSC# handshake mechanism for the configurations in which an I/O APIC is NOT used as a system interrupt controller. 1 = Disable 0 = Enable (default)
14:12	**Reserved**
11	**DRAM Configuration:** The polarity of this bit reflects the value sampled on CKE, on the rising edge of CPURST#. A “0” (default) indicates Memory Configuration #2, a “1” indicates Memory Configuration #1.
10	**PCI Agent to Aperture Access Disable—R/W.** This bit is used to prevent access to the aperture from the primary PCI side (i.e., PAC’s PCI interface does not respond as a target with DEVSEL# if the access is within the aperture). This bit is don’t care if bit 9 is 0. 1 = Disable 0 = Enable. If this bit is 0 (default) and bit 9 of this register is 1, then accesses to the aperture are enabled for the primary PCI side.
9	**Aperture Access Global Enable—R/W.** This bit is used to prevent access to the aperture from any port (processor, PCI or AGP) before aperture range is established by the configuration software and appropriate translation table in the main DRAM has been initialized. 1 = Enable. It must be set after the system is fully configured for aperture accesses. 0 = Disable (default) Note: This bit globally controls accesses to the aperture and that bit 10 provides the next level of control for accesses originated from the primary PCI side.
8:7	**DRAM Data Integrity Mode (DDIM) —R/W** . These bits provide software configurability of selecting between ECC mode, EC-only (error checking only) mode, or non-ECC mode of operation of the DRAM interface in the following manner: 00 = Non-ECC (Byte-Wise Writes supported) (Default) 01 = EC only - Checking with No correction 10 = Reserved 11 = ECC Generation and Checking/Correction

Bit	Description
6	**ECC _TEST Diagnostic Mode Enable (ETPDME)—R/W.** 1 = Enable. PAC enters an ECC Diagnostic test mode. 0 = Disable (default). Normal mode.
5	**MDA Present—R/W.** This bit works with the VGA Enable bit in the BCTRL register of device 1 to control the routing of processor-initiated transactions targeting MDA compatible I/O and memory address ranges. When the VGA Enable bit is set to 1, and this bit is reset to 0, references to MDA resources are sent to AGP. In all other cases references to MDA resources are sent to PCI. MDA resources are defined as the following: Memory: 0B0000h - 0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, (including ISA address aliases, A[15:10] are not used in decode) Any I/O reference that includes the I/O locations listed above, or their aliases, will be forwarded to PCI even if the reference includes I/O locations not listed above. The following table shows the behavior for all combinations of the MDA present and VGA forward bits: **VGA / MDA / Behavior** 0 / 0 / All references to MDA and VGA go to PCI 0 / 1 / Reserved 1 / 0 / All references to VGA got to AGP - MDA-only (I/O 3BFh and aliases) references go to PCI 1 / 1 / VGA references go to AGP; MDA references go to PCI
4:0	Reserved

2. DRAM Memory: Buffered/Unbuffered EDO Support

Table 14 contains four notes. Note 3 indicates “1-GB memory array is achieved by using Double-Sided Buffered EDO DIMMs.” This is incorrect.

Note 3 is changed to: “1-GB memory array is achieved by using single sided 128 MB technology buffered EDO DIMMs. Double-sided buffered EDO DIMMs have not been evaluated nor validated for use in Intel® 440LX chipset -based platforms. In addition, buffered EDO DIMMs are keyed differently than unbuffered EDO DIMMs. Therefore, buffered and un-buffered EDIO DIMMs are not interchangeable in a Intel® 440LX chipset-based platform.”