# Intel® 82803AA Memory Repeater Hub for RDRAM* Devices(MRH-R)

## Specification Update

***June 2001***

**Notice:** The Intel® 82803AA MRH-R may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 298181-004

# Contents

# Revision History

| Rev. | Draft/Changes | Date |
|---|---|---|
| -001 | Initial Release | March 2000 |
| -002 | Formatting changes only. No technical information changes | March 2001 |
| -003 | Added Specification Change #2, Added Documentation Change #2 | May 2001 |
| -004 | Added Specification Clarification: Electrical Characteristics | June 2001 |

# Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

### Affected Documents/Related Documents

| Document Title | Document Number |
|---|---|
| *Intel® 82803AA Memory Repeater Hub for RDRAM* Devices (MRH-R) Datasheet* | 298022-002 |

## Nomenclature

**Specification Changes** are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

**Errata** are design defects or errors. Errata may cause the Intel® 82803AAMRH-R behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

**Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

**Documentation Changes** include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

# Component Marking Information

The Intel® 82803AA MRH-R may be identified by the following component markings:

| Stepping | S-Spec | Top Marking | Notes |
|---|---|---|---|
| A-2 | SL3ML | FW82803AA, SL3ML | |

# Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes which apply to the listed Intel® 82803AA MRH-R steppings. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

## Codes Used in Summary Table

### Stepping

| | |
|---|---|
| X: | Erratum, Specification Change or Clarification that applies to this stepping. |
| (No mark) or (Blank Box): | This erratum is fixed in listed stepping or specification change does not apply to listed stepping. |

### Status

| | |
|---|---|
| Doc: | Document change or update that will be implemented. |
| Fix: | This erratum is intended to be fixed in a future stepping of the component. |
| Fixed: | This erratum has been previously fixed. |
| No Fix | There are no plans to fix this erratum. |
| Eval | Plans to fix this erratum are under evaluation. |

### Other

| | |
|---|---|
| Shaded: | This item is either new or modified from the previous version of the document. |

| NO. | A2 | SPECIFICATION CHANGES |
|---|---|---|
| 1 | X | Correction of 82803AA MRH-R Auto Levelization Process |
| 2 | X | S3 Not Supported |

| Number | Steppings | | Plans | ERRATA |
|---|---|---|---|---|
| | A2 | | | |
| 1 | X | | NoFix | 82803AA MRH-R SMBus Controller |
| 2 | X | | NoFix | 82803AA MRH-R IRO Bit |
| 3 | X | | NoFix | 82803AA MRH-R Single Channel Powerdown |

| Number | SPECIFICATION CLARIFICATIONS |
|---|---|
| 1 | Electrical Characteristics |

| NO. | A2 | DOCUMENTATION CHANGES |
|---|---|---|
| 1 | X | 82803AA MRH-R ST—Stepping Register |
| 2 | X | Ballout # D5 Changed from Reserved to VSS |

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# Specification Changes

## 1. Correction of 82803AA MRH-R Auto Levelization process

The ‘Stick’ Channel Time Domain delay is programmed via the tRDLY_stick bits[2:0] in the 82803AA MRH-R LMTR register.

The 82803AA MRH-R updates this delay during the levelization process by measuring on-the-fly, the number of rclks from an expansion SCP read command to the first non-zero data seen on ‘stick’ channel signal DQA5 at the 82803AA MRH-R. This automatic process is being de-featured.

The correct method of levelizing ‘stick’ channel B is documented in the *Intel® 82840 MCH BIOS Specification*.

## 2. S3 Not Supported

S3 (Suspend-to-RAM) is not supported by the 82803AA MRH-R. Delete Section 4.4, *STR Support*, from the *Intel® 82803AA Memory Repeater Hub for RDRAM* Devices (MRH-R) Datasheet*.

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# Errata

## 1. 82803AA MRH-R SMBus Controller

**Problem:** The SMBus controller in the 82803AA MRH-R will fail intermittently when reading data from RDRAM devices.

**Implication:** BIOS algorithms that use the 82803AA MRH-R SMBus controller to detect memory will encounter unreliable results. This can cause the BIOS to hang during boot time. The 82803AA MRH-R SMBus controller should not be used.

**Workaround:** The ICH SMBus controller should be used in place of the 82803AA MRH-R SMBus controller. Careful attention should be given to selecting SMBus addresses to avoid address contention when making this change.

**Status:** There are currently no plans to fix this erratum.

## 2. 82803AA MRH-R IRO Bit

**Problem:** The 82803AA MRH-R does not clear the IRO bit (Initiate RIC Operation) after issuing the SET Fast clock command. The BIOS will check this bit for completion of the SET Fast clock command.

**Implication:** This will result in a system hang if the BIOS uses this bit to determine a SET Fast clock command completion.

**Workaround:** No workarounds are required. The 82803AA MRH-R will issue the SET Fast clock command within 1 SCLK of the IRO bit being set in the RIC register. The time necessary to program the RIC register with another command is greater than 1 SCLK.

**Status:** There are currently no plans to fix this erratum.

## 3. 82803AA MRH-R Single Channel Powerdown

**Problem:** The MCH will issue a powerdown entry command to each individual stick channel that will power down the devices, MRH-R clocks and RAC on the targeted stick channel. Upon the receipt of an individual stick channel powerdown command, the 82803AA MRH-R will power down the MRH-R clocks and RACs on the intended stick channel as well as the unintended one.

**Implication:** The stick channel that did not receive the powerdown command will be inaccessible to proper powerdown entry commands. The improper powerdown will result in the loss of data content on that channel. The system will not be able to return from *Suspend-to-RAM* properly.

**Workaround:** The MRH-R will set the RC bit after both the expansion and slave RACs have been initialized. The BIOS should write a ‘1’ to the RC bit (MRH-R RIR Register at 0Fh, bit 4) after it is set by the MRH-R.

**Status:** There are currently no plans to fix this erratum.

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# Specification Clarifications

## 1. Electrical Characteristics

Add *Section 5 Electrical Characteristics*, pages 11–14, to the *Intel*® 82803AA *Memory Repeater Hub for RDRAM Devices (MRH-R) Datasheet*:

# 5 Electrical Characteristics

This section contains the AC/DC specifications for the Intel® 82803AA[MRH-R] component.

The Direct RDRAM Interface introduces a new type of signaling interface called RSL (Rambus Signaling Level). RSL signals are open-drain drivers, and must be terminated to 1.8 V via a 28 Ω termination resistor.

## 5.1 Absolute Maximum Ratings

| | |
|---|---|
| Case Temperature under Bias | 0 °C to +105 °C (no heatsink) |
| Storage Temperature | -55 °C to +150 °C |
| 1.8 V Supply Voltage with Respect to Vss | -0.5 V to +2.5 V |

***Warning:*** Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operating beyond the "Operating Conditions" is not recommended and extended exposure beyond "Operating Conditions" may affect reliability.

## 5.2 Thermal Characteristics

The MRH-R is designed for operation at case temperatures between 0 °C and +105 °C. The thermal resistance of the package is given in Table 4.

**Table 4. 82803AA [MRH-R] Package Thermal Resistance**

| Parameter | Air Flow Meters/Second (Linear Feet per Minute) | |
|---|---|---|
| | 0 (0) | 1.0 (196.9) |
| Psijt (°C/Watt)(1) | 0.8 | 0.9 |
| $Theta_{ja}$ (°C/Watt)(1) | 22.7 | 20.8 |

**NOTES:**
1. Typical value measured in accordance with EIA/JESD 51-2 testing standard.

## 5.3 Power Characteristics

### Table 5. DC Characteristics

**Functional Operating Range (VCC1_8 = 1.8 V ± 5%; $T_{CASE}$ = 0 °C to +105 °C)**

| Symbol | Parameter | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $P_{MRH-R}$ | Thermal Power Dissipation for 82803AA [MRH-R] | 2.2 | -- | W | Note 1, at 300 MHz/400 MHz |
| $I_{CC-SUS}$ | 1.8 V VCC Power Supply Sustain Current | 1.565 | -- | mA | Note 3, 1.8 V at 400 MHz |

**NOTES:**

1. This spec is the Thermal Design Power of 82803AA [MRH-R] component, and it is the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations in both hardware and software technology over the life of the component. It does not represent the expected power generated by a power virus.
2. This is the maximum supply current consumption when all interfaces are idle and the clock inputs are turned off.
3. This is the maximum sustained current.

## 5.4 I/O Interface Signal Groupings

The signal description includes the type of buffer used for the particular signal:

**SMBus** System Management Interface at 2.5 V.

**RSL** Rambus Signaling Level interface signal. Refer to www.rambus.com for more information.

**Rambus CMOS** Rambus CMOS buffers are used for the CMOS signals on Rambus Interface. These CMOS buffers have a different DC specification than the non-Rambus CMOS buffers.

### Table 6. Signal Groups

| Signal Group | Signal Type | Signals |
|---|---|---|
| (a) | Rambus CMOS I/O | ExSIO, CHA_SIO, CHB_SIO, MRH_SIO |
| (b) | Rambus CMOS Input | ExSCK, ExCMD |
| (c) | Rambus CMOS Output | CHA_CMD, CHA_SCK, CHB_CMD, CHB_SCK |
| (d) | RSL I/O | ExDQA[8:0], ExDQB[8:0], CHA_DQA[8:0], CHA_DQB[8:0], CHB_DQA[8:0], CHB_DQB[8:0] |
| (e) | RSL Output | CHA_RQ[7:0], CHA_CFM, CHA_CFM#, CHB_RQ[7:0], CHB_CFM, CHB_CFM# |
| (f) | RSL Input | EXP1, EXP0, ExRQ[7:5], ExRQ[4:0], ExCTM, ExCTM#, ExCFM, ExCFM#, CHA_CTM, CHA_CTM#, CHB_CTM, CHB_CTM# |
| (g) | SMBus CMOS I/O | SMBDATA, SMBCLK |
| (h) | CMOS Output | SYNCLKNA, SYNCLKNB, PCLKMA, PCLKMB, STOPA#, STOPB#, PWRDNA#, PWRDNB#, REFCLK |
| (i) | CMOS Input | RST# |
| (j) | 1.8V Power Input | VCC1_8 |

# 5.5 DC Characteristics

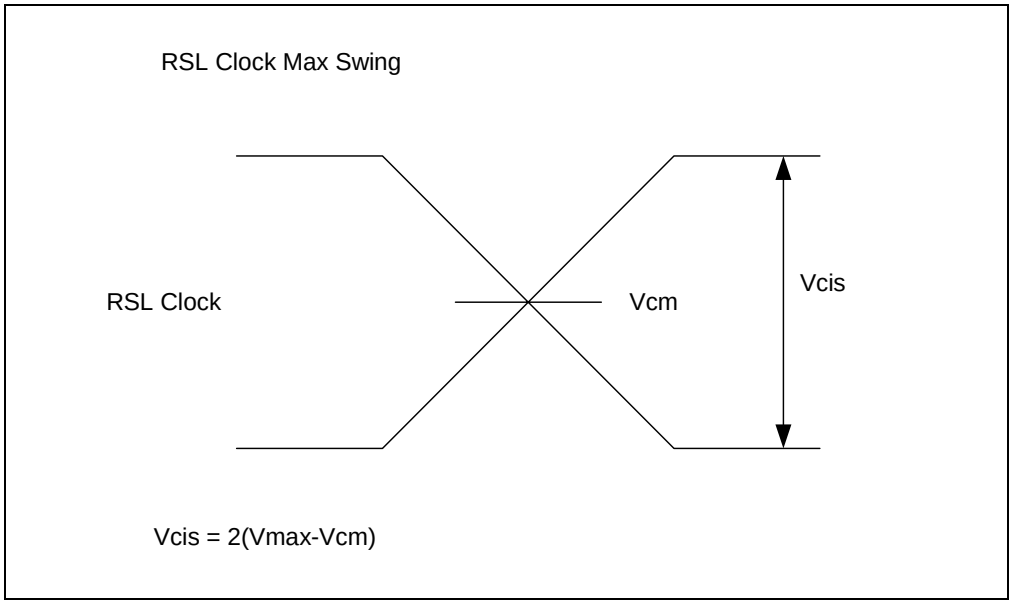
### Table 7. DC Characteristics

**Functional Operating Range ( VCC1_8 ± 5%, Tcase = 0 °C to 105 °C )**

| Symbol | Signal Group | Parameter | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| VCC1_8 | (j) | Core Voltage of the MRH-R | 1.71 | 1.89 | V | |
| VOL2 | | RSL Output Low Voltage | -- | 1.0 | V | |
| VOH2 | | RSL Output High Voltage | Vterm | | V | 1 |
| VIL2 | (f) | RSL Input Low Voltage | | Vref – 0.175 | V | 2 |
| VIH2 | (f) | RSL Input High Voltage | Vref + 0.175 | | V | 2 |
| | | | | | | |
| VIL1 | (b) | Rambus CMOS Input Low Voltage | -0.3 | VCC1_8 / 2 – 0.25 | V | |
| VIH1 | (b) | Rambus CMOS Input High Voltage | VCC1_8 / 2 + 0.25 | VCC1_8 + 0.3 | V | |
| VOL1 | (c) | Rambus CMOS Output Low Voltage | -- | VCC1_8 / 2 – 0.65 | V | |
| VOH1 | (c) | Rambus CMOS Output High Voltage | VCC1_8 / 2 + 0.45 | -- | V | |
| | | | | | | |
| IOL1 | (c) | Rambus CMOS Output Low Current | -- | 1.0 | mA | |
| IOH1 | (c) | Rambus CMOS Output High Current | -0.25 | -- | mA | |
| RCLK_VMAX | | RSL Clock Max Input Voltage | | 2.2 | V | 3 |
| RCLK_VCIS | | RSL Clock Max Voltage Swing | | Vcis = 2 (Vmax – Vcm) | | 3 |
| IOL2 | (d),(e) | RSL Output Low Current | 30 | 90 | mA | |
| IOH2 | | RSL Output High Current at Vol = 0.9V | -10 | 10 | µA | |
| | | | | | | |
| IIL1 | | RSL Input Leakage Low Current | -10 | 10 | µA | |
| IIH1 | | RSL Input Leakage High Current | -10 | 10 | µA | |
| | | | | | | |
| IIL2 | (a),(b) | Rambus CMOS Input Leakage Current | -10.0 | 10.0 | µA | |
| $CIN_{rsl\ master}$ | | RSL Input Capacitance | 4 | 6 | pF | $F_C$ = 1 MHz |
| $CIN_{rsl\ slave}$ | | RSL Input Capacitance | 2.7 | 5 | pF | $F_C$ = 1 MHz |
| $CIN_{sck,cmd}$ | | Rambus CMOS Input Capacitance | 7 | 9 | pF | $F_C$ = 1 MHz |
| $CIN_{sio}$ | | Rambus CMOS Input Capacitance | 4 | 6 | pF | $F_C$ = 1 MHz |

**NOTES:**

1. Vterm provided externally of MRH-R. It carries a nominal value of 1.8 V.
2. Vref has a nominal value of 1.4 V
3. Vcis = 2(Vmax-Vcm), where: Vcis = Maximum clock input voltage swing, Vcm = Voltage common mode, Vmax = 2.2 V. See figure below.


RSL Clock Max Swing
RSL Clock
Vcm
Vcis
Vcis = 2(Vmax-Vcm)

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# Documentation Changes

## 1. 82803AA MRH-R ST—Stepping Register

**ST-Stepping Register, High Word**
Address: 24h
Default: 0002h
Access: Read Only
Size: 16 bits

| Bit | Description |
|---|---|
| 15:8 | **Reserved** |
| 7:4 | **Protocol Revision.** This field specifies the version of the Direct RDRAM channel implemented. |
| 3:0 | **Revision Identification Number.** This is a 4 bit field that identifies the revision identification number for the MRH-R. For A-2 stepping the value is 010h |

## 2. Ballout # D5 Changed from Reserved to VSS

The Ballout number D5 has changed from Reserved to VSS. Figure 20, "*MRH-R Ballout (Top View, Left Side)"* and Table 4, "*MRH-R Alphabetical Ball Assignment*" of the *Intel*® 82803AA *Memory Repeater Hub for RDRAM (MRH-R)* datasheet, Rev 002 is intended to be updated to reflect this change.