Intel® 850 Chipset Family: Intel® 82850/82850E Memory Controller Hub (MCH)

Specification Update

May 2002

Notice: The Intel® 82850/82850E MCH may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 298247-005

Contents

Revision History

Rev.	Draft/Changes	Date
-001	Initial Release	November 2000
-002	• Added A3 stepping information. • Formatting changes throughout	March 2001
-003	• Added Specification Change 1, Erratum 7, Specification Clarification 1.	May 2001
-004	• Added Documentation Change 1: Error Address Pointer Register	July 2001
-005	• Added 82850E to Component ID/Device Marking • Moved Specification Change 1, 288Mb Support for 16d Architecture, and Documentation Change 1, Error Address Pointer Register, to the public datasheet	May 2002

Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents/Related Documents

Document Title	Document Number
Intel® 850 Chipset Family: 82850/82850E Memory Controller Hub (MCH) Datasheet	290691-002

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the behavior of the Intel® 82850 MCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Identification via Programming Interface

The Intel® 82850 and 82850E MCH may be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
A2*	8086h	2530h	02h
A3	8086h	2530h	04h

NOTES:
1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00–01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15:0 of the Device ID Register located at offset 02–03h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

* A2/A3 Stepping for 82850. 82850E is available in A3 stepping only.

The Intel® 82850 or 82850E MCH may be identified by the following PCI Device 0 register contents:

Address Offset	Bit	Bit Contents - 850	Bit Contents – 850-E
Feh	9	0b	1b

Component Marking Information

The Intel 82850 MCH may be identified by the following component markings:

Stepping	Q-Spec	Top Marking	Notes
A2	QA49ES	SL4NG	
A3	QB77ES	SL5HA	

The Intel® 82850E MCH may be identified by the following component markings:

Stepping	Q-Spec	Top Marking	Notes
A3	QC90ES	SL64X	

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes which apply to the listed Intel 82850/82850E MCH steppings. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Erratum, Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status

Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
No Fix	There are no plans to fix this erratum.
Eval	Plans to fix this erratum are under evaluation.

Other

Shaded:	This item is either new or modified from the previous version of the document.

NO.	A2	A3	SPECIFICATION CHANGES
			There are no Specification Changes in this revision of the Specification Update

NO.	A2	A3	PLANS	ERRATA
1	X	X	NoFix	Suspend to RAM (S3) Entry
2	X	X	NoFix	Direct RDRAM* Device NAP Mode
3	X	X	NoFix	Invalid Graphic Aperture Access
4	X	X	NoFix	VDDQ Leakage
5	X	X	NoFix	Sustained PCI Bandwidth
6	X	X	NoFix	RDRAM* Device Interface Initialization Operation (IIO) Bit
7	X	X	NoFix	Simultaneous Clear/Set on Hub Interface Parity Error

NO.	A2	A3	SPECIFICATION CLARIFICATIONS
1	X	X	AGP Assertion of TRDY# before Throttle Point

NO.	A2	A3	DOCUMENTATION CHANGES
			There are no Documentation Changes in this revision of the Specification Update

Specification Changes

There are no Specification Changes in this revision of the Specification Update

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Errata

1. Suspend to RAM (S3) Entry

Problem: In the Intel 82850 MCH, a boundary condition between the “S3” (Suspend to RAM) state entry and a regularly scheduled refresh request causes the bank counter to miss an increment, leaving some banks in a non-precharged state. As a result, these banks are not refreshed during the S3 state.

Implication: This issue may cause data corruption and/or system hang upon resumption from a power-down state (S3/STR).

Workaround: System BIOS must ensure that all banks are closed before executing the memory power down sequence.

Status: There are no plans to fix this erratum.

2. Direct RDRAM* Device NAP Mode

Problem: With NAP mode enabled, the MCH may hang, causing an infinite number of random cycles to be issued to the memory interface.

Implication: NAP mode is not functional.

Workaround: None identified. The NAP feature should not be used.

Status: There are no plans to fix this erratum.

3. Invalid Graphic Aperture Access

Problem: Memory write accesses through the graphic aperture targeted above TOP memory or invalid memory location will cause the system to hang.

Implication: If an invalid graphic aperture access is executed, the system will hang. Below are two scenarios that could cause an invalid graphic aperture translation:

- Write to aperture entry is marked as "invalid"
- Write to aperture entry is marked as "valid," but does not point to physical memory

Workaround: None.

Status: There are no plans to fix this erratum.

4. VDDQ Leakage

Problem: If the 1.5 V supply for the MCH's VDDQ voltage is turned off (set to 0) and the 1.8 V supply for the MCH is on (set to 1.8 V), an internal diode within the MCH will be forward biased. This will cause leakage into the VDDQ power plane, approximately 1V.

Implication: During normal operations, this diode is not forward biased and has a leakage current of only 10 µA.

Workaround: Turn off and power on VCC1_8 and VDDQ at the same time. Follow the MCH power sequencing requirements documented in the platform design guide.

Status: There are no plans to fix this erratum.

5. Sustained PCI Bandwidth

Problem: During a memory read multiple operation, a PCI master will read more than one complete cache line from memory. In this situation, the MCH pre-fetches information from memory in order to provide optimal performance. However, the MCH cannot provide information to the PCI master fast enough. Therefore, the Intel® 82801BA terminates the read cycle early to free up the PCI bus for other PCI masters to claim.

Implication: The early termination limits the maximum bandwidth to ~90 MB/s.

Workaround: None

Status: There are no plans to fix this erratum.

6. RDRAM* Device Interface Initiate Initialization Operation (IIO) Bit

Problem: The Initiate Initialization Operation (IIO) bit in the RDRAM device initialization control management (RICM) register may be cleared by the MCH too early.

Implication: If the MCH clears the bit too early and BIOS immediately issues a new initialization op code (IOP), the MCH may incorrectly control the RDRAM device CMD signal causing an invalid cycle to write to the memory subsystem, and the IIO bit may not be cleared. This results in a system hang during the memory initialization process.

Workaround: BIOS must allow at least 1 µs delay between executing initialization opcodes (IOP).

Status: There are no plans to fix this erratum.

7. Simultaneous Clear/Set on Hub Interface Parity Error

Problem: If a Hub Interface error occurs, the MCH will set an error status flag for the offending Hub Interface. When the status flag transitions from a 0 to a 1, the MCH will generate an SERR (if enabled) and the ICH2 will generate an NMI to the processor. If an NMI handler clears the status flag on exactly the same clock as the MCH is trying to set the flag for a second NMI, the status flag will remain set at a 1 and a second NMI will not be generated.

Implication: This erratum was discovered using Intel test cards and has not been seen with real world applications. It is thought that most operating systems do not try to recover from an NMI.

Workaround: A specialized HAL can be written that clears the status flag and then checks to ensure that the status flag is indeed cleared before exiting the handler.

Status: There are no plans to fix this erratum.

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Specification Clarifications

1. AGP Assertion of TRDY# before Throttle Point

The AGP specification is ambiguous as to the state and protocol of TRDY# before the first throttling point during AGP Fast Writes. If an AGP master (acting as a PCI target) asserts TRDY# before the first throttling point, the system will hang. An ECR has been requested to clarify the AGP specification.

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Documentation Changes

There are no Documentation Changes in this revision of the Specification Update