# Intel® 815 Chipset Family: 82815 Graphics and Memory Controller Hub (GMCH)

## Specification Update

***May 2001***

**Notice:** The Intel® 82815 GMCH may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 298253-003

# Contents

# Revision History

| Rev. | Draft/Changes | Date |
|---|---|---|
| -001 | Initial Release: Specification Changes # 1– 2; Errata # 1 – 5; Specification Clarification # 1– 3. | August 2000 |
| -002 | Added Errata #6; Added Specification Clarification #4. | January 2001 |
| -003 | Added Specification Clarifications # 5 – 7;<br>Added Documentation Change #1 | May 2001 |

# Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

### Affected Documents/Related Documents

| Document Title | Document Number |
|---|---|
| *Intel® 815 Chipset Family: 82815 Graphics and Memory Controller Hub (GMCH)* datasheet | 290688-001 |

## Nomenclature

**Specification Changes** are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

**Errata** are design defects or errors. Errata may cause the Intel®815 chipset behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

**Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

**Documentation Changes** include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

# Component Identification via Programming Interface

The Intel® 82815 GMCH may be identified by the following register contents:

| Stepping | Device | Vendor ID[1] | Device ID[2] | Revision Number[3] |
|---|---|---|---|---|
| A0 | 0 | 8086h | 1130h | 00h |
| | 1 | 8086h | 1131h | 00h |
| | 2 | 8086h | 1132h | 00h |
| A1 | 0 | 8086h | 1130h | 01h |
| | 1 | 8086h | 1131h | 01h |
| | 2 | 8086h | 1132h | 01h |
| A2 | 0 | 8086h | 1130h | 02h |
| | 1 | 8086h | 1131h | 02h |
| | 2 | 8086h | 1132h | 02h |

**NOTES:**

1. The Vendor ID corresponds to bits 15-0 of the Vendor ID Register located at offset 00-01h in the PCI function 0 configuration space of Device 0, 1, 2.
2. The Device ID corresponds to bits 15-0 of the Device ID Register located at offset 02-03h in the PCI function 0 configuration space of Device 0, 1, 2.
3. The Revision Number corresponds to bits 7-0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space of Device 0, 1, 2.

# Component Marking Information

The Intel 82815 GMCH can be identified by the following component markings:

| Stepping | S-Spec | Top Marking | Notes |
|---|---|---|---|
| A0 | Q921 | FW82815 | |
| A1 | Q963 | FW82815 | |
| A1 | Q964 | FW82815 | |
| A2 | SL4DF | FW82815 | Production 82815 GMCH |

# Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed Intel® 815 chipset stepping. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

## Codes Used in Summary Table

### Stepping

| | |
|---|---|
| X: | Erratum, Specification Change or Clarification that applies to this stepping. |
| (No mark) or (Blank Box): | This erratum is fixed in listed stepping or specification change does not apply to listed stepping. |

### Status

| | |
|---|---|
| Doc: | Document change or update that will be implemented. |
| Fix: | This erratum is intended to be fixed in a future stepping of the component. |
| Fixed: | This erratum has been previously fixed. |
| No Fix | There are no plans to fix this erratum. |
| Eval | Plans to fix this erratum are under evaluation. |

### Other

| | |
|---|---|
| Shaded: | This item is either new or modified from the previous version of the document. |

| Number | SPECIFICATION CHANGES |
|---|---|
| 1 | SWE#, SCAS#, SRAS#, SMAA[11:8,3:0], and SBS[1:0] Signal Buffer Strength Programming |
| 2 | DRAMT – DRAM Timing Register (Device 0), Address Offset 53h, Bit 3 |

| Number | Steppings | | Plans | ERRATA |
|---|---|---|---|---|
| | A2 | | | |
| 1 | X | | Fix | Host Interface Buffer Noise |
| 2 | X | | No Fix | System Bus Snoop |
| 3 | X | | No Fix | Asynchronous Screen Flip |
| 4 | X | | No Fix | System Memory Data Line |
| 5 | X | | No Fix | System Memory Frequency |
| 6 | X | | No Fix | False Device 1 System Error Message |

| Number | SPECIFICATION CLARIFICATIONS |
|---|---|
| 1 | Section 1.5: System Memory Interface |
| 2 | Section 4.5: System Memory DRAM Interface |
| 3 | Section 4.5.2: DRAM Address Translation and Decoding |
| 4 | Only AGP4X Cards Which Use Differential Clocking Mode Are Supported |
| 5 | The 82815 Does Not Support Intel® Pentium® III Processors That Use 0.13 µ Technology |
| 6 | Chipsets in the Intel® 815 Chipset Family |
| 7 | The 82815 Does Not Support Intel® Pentium® III Processors That Use 0.13 µ Technology |

| Number | DOCUMENTATION CHANGES |
|---|---|
| 1 | 82815 544 BGA Ball-Out Package Dimensions Is Corrected |

# Specification Changes

## 1. SWE#, SCAS#, SRAS#, SMAA[11:8,3:0], and SBS[1:0] Signal Buffer Strength Programming

Regardless of system memory interface frequency, the SMAA [11:8, 3:0], SBS [1:0] SWE#, SCAS#, and SRAS# signal buffer strengths for all rows should be set accordingly to the DIMM loading which is defined in the table below. This affects the BUFF_SC – System Memory Buffer Strength Control Register, Device0, Reg92h [1:0].

Reference Section 3.4.24, *BUFF_SC—System Memory Buffer Strength Control Register*.

| | |
|---|---|
| 1:0 | **SWE#, SCAS#, SRAS#, SMAA[11:8, 3:0], SBS[1:0] Control Buffer Strengths (All Rows)**<br>00 = 1.7x > 32 loads<br>01 = 0.7x < 8 loads<br>10 = 1.0x 8-32 loads<br>11 = 1.0x 8-32 loads<br>The load on the Address and Control signals (other than SMA*[7:4] above) is simply the number of devices populated in ALL rows (range from 4 to 48 loads!).<br>Loads = (64 / Row 0 Device Width) + (64 / Row 1 Device Width) + (64 / Row 2 Device Width) +/ Row 3 Device Width) + (64 / Row 4 Device Width) + (64 / Row 5 Device Width) |

## 2. DRAMT – DRAM Timing Register (Device 0), Address Offset 53h, Bit 3

Reference the *Intel® 815 Chipset Family: 82815 Graphics and Memory Controller Hub (GMCH)* datasheet, Section 3.4.17, *DRAMT – DRAM Timing Register*. The description for bit 3 is changed from “Intel Reserved” to show the following:

| 7 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|
| SDRAM Mode Select | DRAM Cycle Time | Host Aperture Cycle Queue Slot | CAS# Latency | SDRAM RAS# to CAS# Dly | SDRAM RAS# Precharge |

| Bit | Description |
|---|---|
| 3 | **Host Aperture Cycle Queue Slot**<br>0 = Default value. No dedicated queue slot is reserved for host to aperture cycles.<br>1 = A dedicated queue slot is reserved for host to aperture cycles.<br>The BIOS should set this bit to ‘1’. |

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# Errata

## 1. Host Interface Buffer Noise

**Problem:** False assertions of H_ADS# signal observed on-die on the A-2 stepping of the Intel 815 chipset (GMCH).

**Implication:** System hangs or boot failures can occur with A-2 stepping of Intel 815 chipset based platforms.

**Workaround:** Increase spacing between nearest neighbor system memory and GTL+ buffers. Reduce System Memory buffer strength settings for 100/133.

**Status:** The Root Cause of this errata was found to be cross coupling of system memory signals onto nearest neighbor GTL+ signals (specifically H_ADS#) on the board, package, and die. The A-2 stepping of the Intel 815 chipset will include circuit changes to improve the noise immunity of GTL+ buffers.

## 2. System Bus Snoop Logic

**Problem:** Under specific sequence of bus cycles, data from the wrong address may be returned to the graphics controller. This can occur if the following three conditions align:

1. Back-to-back ADS# on the system bus
2. PHOLD (ISA Master) access on the hub interface

**Status:** External graphics AGP snoop OR internal graphics cacheable BLTs/Store DWORD.

**Implication:** If the data from the wrong address is returned to the graphics controller, either graphics corruption or system hang can occur.

**Workaround:** None

**Status:** This Issue has only been observed in a System Validation Environment with a specific focus test. This issue has not been observed with any real applications tested. There are no plans to fix this erratum.

### 3. Asynchronous Screen Flip

**Problem:** When the Intel 815 chipset A-2 step is configured for asynchronous screen flipping, under certain timing-dependent circumstances the display engine may temporarily read pixel data from a random memory location.

**Implication:** When changing display surfaces using the asynchronous screen flipping, subtle display corruption is seen in the form of short, somewhat random colored, horizontal lines along the left side of the screen.

**Workaround:** Driver version 4.1.1 does, and future versions will, disable asynchronous screen flipping for commonly used 3D resolutions.

**Status:** There are no plans to fix this erratum in silicon.

### 4. System Memory Data Line Noise

**Problem:** When the Intel 82815 A-2 step GMCH has multiple system memory data lines transition from low to high, a glitch can appear on non-switching data lines.

**Implication:** The erratum is amplified by trace impedance and discontinuities on the motherboard and DIMM. When measured at the SDRAM pin, it can violate the published $V_{IL}$ specification of SDRAM components in the valid timing window. In this case, incorrect data could be clocked into the SDRAM causing data corruption.

**Workaround:** To minimize amplification of the glitch on the board:

- Follow published design specifications detailed in the *Intel® 82815 Chipset Platform Design Guide*, dated June 2000, Order Number 298233-001, para 5.2 and 5.4. For the 82815E, follow published design specifications detailed in the *Intel® 82815E Chipset Platform Design Guide*, dated June 2000, Order Number 298234-001, para 5.2 and 5.4.
- Implement buffer strength and System Memory RCOMP.

**Status:** There are no plans to fix this erratum in silicon.

### 5. System Memory Frequency Select

**Problem:** Register 50h (GMCHCFG) bit 2 of the Intel 82815 A-2 step is set incorrectly when a 66 MHz Front Side Bus processor is plugged into the system.

**Implication:** When the Intel 82815 GMCH A-2 step sets this bit at reset with a 66 MHz Front Side Bus processor plugged into the system, this bit will be set incorrectly.

**Workaround:** BIOS must detect if a 66 MHz Front Side Bus processor is plugged into the system and set this bit to ‘0’ to indicate 100 MHz system memory.

**Status:** There are no plans to fix this erratum in silicon.

### 6. False Device 1 System Error Message

**Problem:** A false Signal System Error (SERR) is generated when Device 1 system error signaling is enabled. The false SERR results in the generation of a Non-Maskable Interrupt (NMI).

**Implication:** A false error is detected and the system may halt.

**Workaround:** Disable Device 1 SERR Message Enable by setting PCICMD1 - PCI-PCI Command Register (Device 1), address offset 04h-05h, bit [8] to “0”. This is the existing BIOS default setting for this bit.

**Status:** There are no plans to fix this erratum in silicon.

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# Specification Clarifications

## 1. Section 1.5: System Memory Interface

This section has been changed to correctly read, “The GMCH supports industry standard 64-bit wide DIMMs with SDRAM devices. The thirteen multiplexed address lines (SMAA[12:0]) along with the two bank select lines (SBS[1:0]) allow the GMCH to support 2M, 4M, 8M, 16M, and 32M x64 DIMMs.”

## 2. Section 4.5: System Memory DRAM Interface

This section has been changed to correctly read, “The 2 bank select lines (SBS[1:0]), the 13 address lines (SMAA[12:0]), and copies of 4 address lines (SMAB[7:4]# and SMAC[7:4]#) allow the GMCH to support 64-bit wide DIMMs using 16-Mb, 64-Mb, 128-Mb, or 256- Mb technology SDRAMs.”

## 3. Section 4.5.2: DRAM Address Translation and Decoding

This section has been changed to correctly read, “The GMCH supports 16-Mbit, 64-Mbit, 128-Mbit, and 256-Mbit SDRAM devices.”

## 4. Only AGP4X Cards Which Use Differential Clocking Mode Are Supported

Section 1.6.1, *AGP Interface*: The following line is added to the section:

“The Intel 82815 chipset only supports AGP4X cards that use differential clocking mode.”

## 5. The 82815 Does Not Support Intel® Pentium® III Processors That Use 0.13 µ Technology

*Intel® 815 Chipset Family: 82815 Graphics and Memory Controller Hub (GMCH)* datasheet *Features List*, Processor/Host Bus Support. Insert the following item in the list:

- Does not support Intel® Pentium® III processors that use 0.13 µ technology.

## 6. Chipsets in the Intel® 815 Chipset Family

Reference *Section 1, Overview*. Insert the following material to replace the paragraph beginning, “There are two chipsets…”

There are five chipsets in the Intel® 815 chipset family:

- Intel® 82815 chipset: This chipset contains the 82815 and the 82801AA ICH.
- Intel® 82815E chipset: This chipset contains the 82815E and the 82801BA ICH2.
- Intel® 82815EP chipset: This chipset contains the 82815EP and the 82801BA ICH2. There is no internal graphics capability. This GMCH uses an AGP port only.

- Intel® 82815G chipset: This chipset contains the 82815G GMCH and 82801AA ICH. There is no AGP port capability and no display cache capability. This GMCH uses internal graphics only.
- Intel® 82815EG chipset. This chipset contains the 82815EG GMCH and 82801BA ICH2. There is no AGP port capability and no display cache capability. This GMCH uses internal graphics only.

***Note:*** The only component difference between the Intel 82815 GMCH and the Intel 82815E GMCH is the I/O Controller Hub. The only component difference between the Intel 82815G GMCH and the Intel 82815EG GMCH is the I/O Controller Hub.

## 7. The 82815 Does Not Support Intel® Pentium® III Processors That Use 0.13 µ Technology

Reference Section 1.4, *Host Interface* in the datasheet. Add the following information to the first paragraph:

The 82815 GMCH will not support Intel Pentium III processors that use 0.13 µ technology. These processors should not be placed in platforms using the 82815 GMCH. Future versions of the Intel 815 chipset family will support Intel Pentium III processors that use 0.13 µ technology.

# Documentation Changes

## 1. 82815 544 BGA Ball-Out Package Dimensions Is Corrected

Reference Section 5.2,*Package Information*, in the datasheet. Replace Figure 13 with the following correct 544 BGA ball-out bottom view: