Intel® 915G/915GV/915GL/915P/ 915PL/910GL Express Chipset

Specification Update

For the Intel® 82915G / 82915GV / 82915GL / 82910GL Intel® Graphics and Memory Controller Hub (GMCH) and Intel® 82915P / 82915PL Memory Controller Hub (MCH)

July 2005

Notice: The Intel® 82915G / 82915GV / 82915GL / 82910GL GMCH and Intel® 82915P / 82915PL MCH may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 301468-006

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. Intel products are not intended for use in medical, life saving, or life sustaining applications.

Intel may make changes to specifications and product descriptions at any time, without notice.

Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

The Intel® 82915G / 82915GV / 82915GL / 82910GL GMCH and Intel® 82915P / 82915PL MCH may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Intel and the Intel logo are trademarks or registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.

*Other names and brands may be claimed as the property of others.

Copyright © 2004–2005, Intel Corporation. All rights reserved.

Contents

Revision History

Revision	Description	Date
-001	• Initial Release	June 2004
-002	• Corrected component marking information	July 2004
-003	• Added Errata items #13 - #18	January 2005
-004	• Added Errata item #19	February 2005
-005	• Added Errata items #20 – 24. • Updated the Component Marking table with Lead Free S-Specs	June 2005
-006	• Added Errata item #25.	July 2005

§

Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Note: The term (G)MCH refers to both the 82915G / 82915GV / 82915GL / 82910GL GMCH and 82915P / 82915PL MCH.

Affected Documents

Document Title	Document Link
Intel® 915G/915GV/915GL/915P/915PL/910GL Express Chipset Datasheet	http://developer.intel.com/design/chipsets/datashts/301467.htm

Nomenclature

Errata are design defects or errors. Errata may cause the *Intel® 82915G / 82915GV / 82915GL / 82910GL / 82915P / 82915PL Express* behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

§

Summary Tables of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes that apply to the listed component steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Erratum, Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status

Doc:	Document change or update that will be implemented.
PlanFix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This item is either new or modified from the previous version of the document.

NO.	B1	C2	PLANS	ERRATA
1	X	X	NoFix	Incorrect PCI Express* Lane Transition after Receiving Several TS1 Packets
2	X	X	NoFix	(G)MCH Does Not Ignore A PCI Express* Null Packet
3	X	X	NoFix	Data Payload Byte Count Supplied During An Unsupported Upstream Configuration Read Is Not 4 Bytes
4	X	X	NoFix	PCI Express* Replay Timer Register Default Setting Is Incorrect
5	X	X	NoFix	PCI Express* Common Mode Voltage Noise Immediately Following Receiver Detect sequence
6	X	X	NoFix	DMI Link Egress Port Address is Not Programmable

NO.	B1	C2	PLANS	ERRATA
7	X	X	NoFix	(G)MCH Does Not Send Minimum Number TS2 on PCI Express*
8	X	X	NoFix	DMI Traffic Ordering Violation
9	X	X	NoFix	I/O Bar Address Range Incorrectly Decoded as Memory Address by IGD
10	X	X	NoFix	E_SMERR Bit Set Incorrectly
11	X	X	NoFix	Desktop Icon Corruption When System Power Is Removed Ungracefully
12	X	X	NoFix	Booting to Certain Flat Panels with ADD2 Results in Lost Display Lines
13	X	X	NoFix	DDR2-533 Duty Cycle
14	X	X	Fixed	2GB DIMM Module Support in Asymmetric Mode
15	X	X	NoFix	PCI Express* DLLPs with Unknown Encoding Type
16	X		Fixed	DDC Slave Stall During Acknowledge Phase
17	X	X	No Fix	Advanced De-interlacing
18	X	X	NoFix	PCI Express* Scrambling
19	X	X	NoFix	PCI Express* SKP/InitFCx Contention
20	X	X	NoFix	LOCK to non-DRAM Memory Flag is Getting Asserted
21	X	X	NoFix	Packet Dropped When Replay Timer Expires and Replay is in Progress
22	X	X	NoFix	PCI Express* Skip Sequence is Not Transmitted When Entering Recovery State
23	X	X	NoFix	Malformed Upstream IO or Configuration Write Cycles Are Not Being Detected As Malformed
24	X	X	NoFix	The Transaction Layer Resets the Completion Timer Counter before Receiving a Passing CRC from the Link Layer on the PCI Express* Port
25	X	X	NoFix	Unintended SDVO Hot Plug Interrupt Events

NO.	SPECIFICATION CHANGES
	There are no specification changes.

NO.	SPECIFICATION CLARIFICATIONS
	There are no specification clarifications.

NO.	DOCUMENTATION CHANGES
	There are no documentation changes.

§

Identification Information

Component Identification Information

The Intel® 915G / 915GV / 915GL / 910GL / 915P / 915PL Express (G)MCH may be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
B1	8086h	2580h	04h
C2	8086h	2580h	0Eh

NOTES:
1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00–01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15:0 of the Device ID Register located at offset 02–03h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

The Intel® 82915G / 82915GV / 82915GL / 82910GL / 82915P / 82915PL (G)MCH may be identified by the following component markings:

Stepping	S-Spec	Top Marking	Notes
B1	SL7LX	NG82915G	82915G GMCH Production Samples
B1	SL7W5	NG82915GV	82915GV GMCH Production Samples
B1	SL74W	NG82910GL	82910GL GMCH Production Samples
B1	SL7LY	NG82915P	82915P MCH Production Samples
C2	SL8BW	NG82915P	82915P MCH Production Samples
C2	SL8AS	QG82915P	82915P MCH Production Samples (Lead Free)
C2	SL8BU	NG82915G	82915G GMCH Production Samples
C2	SL8AT	QG82915G	82915G GMCH Production Samples (Lead Free)
C2	SL8BT	NG82915GV	82915GV GMCH Production Samples
C2	SL8AU	QG82915GV	82915GV GMCH Production Samples (Lead Free)
C2	SL8BV	NG82910GL	82910GL GMCH Production Samples
C2	SL8AR	QG82910GL	82910GL GMCH Production Samples (Lead Free)
C2	SL8CK	NG82915GL	82915GL GMCH Production Samples
C2	SL8DC	QG82915GL	82915GL GMCH Production Samples (Lead Free)
C2	SL8D6	NG82915PL	82915PL MCH Production Samples
C2	SL8DD	QG82915PL	82915PL MCH Production Samples (Lead Free)

§

Errata

1. Incorrect PCI Express* Lane Transition after Receiving Several TS1 Packets

Problem: If (G)MCH receives several TS1 packets with Link and Lane numbers set to PAD, after 4 µs it will time out and transition into configuration state instead of going directly to the Detect state as it should. However, the link will still transition to the Detect state after timing out of Configuration.

Implication: The (G)MCH will experience longer latency when transitioning to Detect state.

Workaround: None at this time.

Status: NoFix. For steppings affected, see the *Summary Tables of Changes*.

2. (G)MCH Does Not Ignore A PCI Express* Null Packet

Problem: If the (G)MCH receives a PCI Express* Null packet, it should drop the packet and not perform sequence number checking or respond with any Ack or Nak DLLP. The issue is that the (G)MCH still performs sequence number checks for Null packets and may respond with an ACK or NAK depending on the result of the check.

Implication: (G)MCH may send ACK or NAK DLLPs in response to a Null packet. This may degrade link performance due to unnecessary retries.

Workaround: None at this time.

Status: NoFix. For steppings affected, see the *Summary Tables of Changes*.

3. Data Payload Byte Count Supplied During An Unsupported Upstream Configuration Read Is Not 4 Bytes

Problem: During configuration reads to unsupported PCI Express* configuration space, the byte count for data payload is not 4.

Implication: Data payload byte count is 5 and not the expected 4.

Workaround: Do not perform unsupported upstream PCI Express* configuration cycles.

Status: NoFix. For steppings affected, see the *Summary Tables of Changes*.

4. PCI Express* Replay Timer Register Default Setting Is Incorrect

Problem: Replay will occur 100 symbol times sooner than expected.

Implication: Retrain of the link may occur more often with devices that have slower ACK to packets from the (G)MCH.

Workaround: BIOS will need to reprogram the Replay Timer Register to reflect actual exit latency value. Contact your Intel Field Representative for the latest BIOS information.

Status: NoFix. For steppings affected, see the *Summary Tables of Changes*.

5. PCI Express* Common Mode Voltage Noise Immediately Following Receiver Detect sequence

Problem: The PCI Express Common Mode Voltage is not stable immediately after Receiver Detect Sequence when entering Polling.Active from Detect.Active states.

Implication: Common Mode Voltage noise may result in bit errors early in Polling.Active state. May result in additional training time before transitioning on to Polling.Configuration.

Workaround: None at this time.

Status: NoFix. For steppings affected, see the *Summary Tables of Changes*.

6. DMI Link Egress Port Address is Not Programmable

Problem: The PCI SIG approved ECR 04 to allow future system software (e.g., Operating System) to discover the link structure of the Root Complex. One of the registers in the (G)MCH that “points” from the DMI port to the ICH6 cannot be programmed correctly.

Implication: There is no impact on platform functionality. ECR’s do not retroactively apply to the current PCI Express 1.0a specification, and no existing software understands the Root Topology discovery structures. These structures are implemented in the (G)MCH only to aid future software development. Such software will need to comprehend the incorrect pointer.

Workaround: None at this time.

Status: NoFix. For steppings affected, see the *Summary Tables of Changes*.

7. (G)MCH Does Not Send Minimum Number TS2 on PCI Express*

Problem: On PCI express the (G)MCH transitions to Recovery. Idle after sending 9 TS2s after receiving the 1st TS2 from the endpoint. The PCI Express specification requires that a device send a minimum of 16 TS2s after detecting the first TS2.

Implication: If the endpoint is unable to consecutively receive 8 of the 9 transmitted TS2s, a 48 ms timeout will be incurred before the device transitions to Detect state and re-attempt training. All known production devices have been able to properly train after receiving 9 TS2s.

Workaround: None at this time.

Status: NoFix. For steppings affected, see the *Summary Tables of Changes*.

8. DMI Traffic Ordering Violation

Problem: Under certain traffic scenarios including AC97 and USB it is possible for upstream data on the DMI link to violate ordering rules. For example, a read completion to the CPU may be allowed to pass a prior write to memory.

Implication: The ordering violation may result in a system hang or unpredictable system behavior.

Workaround: A BIOS Workaround has been implemented. Contact your Intel Field Representative for the latest BIOS information.

Status: NoFix. For steppings affected, see the *Summary Tables of Changes*.

9. I/O Bar Address Range Incorrectly Decoded as Memory Address by IGD

Problem: When GMCH I/0 BAR Device 2, function 0 is programmed to certain address ranges. These address ranges can also incorrectly access graphics MMIO and internal configuration registers.

Implication: When this address decode conflict occurs, graphics display anomalies or system lock may occur.

Workaround: Restrict the values programmed into the PCI config space BAR to fall in one of the following safe ranges: 0x1000-1FF8, 0x3000-0x4FF8, 0x7000-0x9FF8, 0xB000-0xFFF8.

Status: NoFix. For steppings affected, see the *Summary Tables of Changes.*

10. E_SMERR Bit Set Incorrectly

Problem: The E_SMERR bit may be incorrectly set when performing valid accesses to SMM space

Implication: If this bit is used by the SMI handler to determine cache line flushes, unnecessary cache line flushes may occur when in SMM mode. A slight performance impact to the SMI handler may result from unnecessary cache line flushes.

Workaround: None.

Status: NoFix. For steppings affected, see the *Summary Tables of Changes*.

11. Desktop Icon Corruption When System Power Is Removed Ungracefully

Problem: If the system power cord is unplugged while the system is in active state, when power is restored and system restarted, the desktop icons may be corrupted or transparent.

Implication: Desktop icons may become corrupted or transparent.

Workaround: Fixed with next revision of driver.

Status: NoFix. For steppings affected, see the *Summary Tables of Changes*.

12. Booting to Certain Flat Panels with ADD2 Results in Lost Display Lines

Problem: When using an ADD2 or SDVO down device, and booting to DOS, line of information will not be displayed at bottom of screen.

Implication: It may not be possible to input data using a keyboard, as the cursor or input prompt will not be visible on the screen.

Workaround: BIOS workaround contained in latest VID BIOS.

Status: NoFix. For steppings affected, see the *Summary Tables of Changes*.

13. DDR2 Duty Cycle

Problem: When using internal graphics and system memory is DDR2-533, the differential clocks do not meet minimum period of 3.75 nsec and duty cycle of 45/55%, as specified by JEDEC. The measured duty cycle is 44/56%. The duty cycle is within specification when using external graphics or DDR2-400.

Implication: Intel has characterized the system memory clocks and shared the data with the major DRAM suppliers. Intel and the major DRAM suppliers agree that this system clock erratum should not cause system clock related timing issues providing all other DRAM related interface timing specifications are fulfilled according to Intel DDR2 specification addendum. Intel determined that the worst case minimum clock period of 3.55nsec does not occur on consecutive clock pulses.

Workaround: None.

Status: NoFix. For steppings affected, see the *Summary Tables of Changes.*

14. 2GB DIMM Module Support in Asymmetric Mode

Problem: 2GByte DIMM modules based upon 1Gbit memory technology are not supported when the total physical system memory is greater than 3.5GB and is configured for asymmetric mode. Addresses to physical memory are not properly decoded. Symmetric mode and single channel mode are not affected.

Implication: Memory may not be initialized correctly.

Workaround: The BIOS workaround is a memory initialization update contained in the latest BIOS specification update.

Status: Fixed. For steppings affected, see the *Summary Tables of Changes.*

15. PCI Express* DLLPs with Unknown Decode Type

Problem: If the GMCH receives a DLLP on PCI Express with an unknown encoding type, the GMCH may interpret the packet as an ACK or a NAK.

Implication: The GMCH may interpret the ACK as being from an outstanding TLP sent to the device, indicating that the device received the TLP. Or the GMCH may flag a DLLP protocol error in the sequence number is not appropriate. If the GMCH interprets the packet as a NAK, a needless replay may occur.

Workaround: None.

Status: NoFix. For steppings affected, see the *Summary Tables of Changes.*

16. DDC Slave Stall during Acknowledge Phase

Problem: Under specific conditions on the DDC interface, a slave stall during the the acknowledge phase may not be seen by the GMCH, resulting in incorrect DDC data read by the GMCH.

Implication: Information about the display is not available, resulting in the display device not being detected. The display device may not have any output.

Workaround: None.

Status: Fixed. For steppings affected, see the *Summary Tables of Changes.*

17. Advanced De-Interlacing

Problem: With certain video content, specifically the blending of still and full motion video, the advanced de-interlacing feature may not function properly.

Implication: Video artifacts may occur when using the advanced deinterlacing features.

Workaround: The advanced de-interlacing feature will be disabled in the latest Intel® graphics driver.

Status: NoFix. For steppings affected, see the *Summary Tables of Changes.*

18. PCI Express* Scrambling

Problem: While entering the Recovery state, the 91x (G)MCH stops scrambling two symbols before the first TS (training sequence).

Implication: When these non-scrambled symbols are received by the endpoint, the de-scrambler of the endpoint will observe two symbols of random data. The first symbol of TS1 will reset the endpoint's de-scrambler so that the endpoint should recognize the TS1 and TS2 ordered-sets being transmitted and move into the Recovery state as planned. There is no system level impact if the endpoint is * Express Specification 1.0a compliant in ignoring the random data.

Workaround: None.

Status: NoFix. For steppings affected, see the *Summary Tables of Changes.*

19. PCI Express* SKP/InitFCx Contention

Problem: During 91x (G)MCH PCI Express* initialization, if a SKP is being transmitted immediately before a InitFCx DLLP, then a partial InitFCx may be transmitted.

Implication: A slight delay (less than 100ns) may occur during link initialization. Device may report correctable error. InitFCx will automatically be repeated.

Workaround: None

Status: NoFix. For steppings affected, see the *Summary Table of Change.*

20. Lock to non-DRAM Memory Flag is Getting Asserted

Problem: A CPU lock cycle request is unintentionally being recognized as request to a non-system memory destination

Implication: The GMCH may incorrectly flag an error for a valid lock cycle that targets DRAM. A System Error (SERR) may be generated if enabled by System BIOS. Note: The default setting for ERRCMD[9] Bus 0 Device 0 Offset CAh is to disable this reporting.

Workaround: Do not enable or change default setting of ERRCMD[9] Bus 0 Device 0 Offset CAh (SERR reporting for Lock cycles to non-DRAM Memory)

Status: NoFix. For affected steppings, see the *Summary Table of Changes.*

21. Packet Dropped When Replay Timer Expires and Replay is in Progress

Problem: When a packet replay is in progress on the PCI Express* Port and the replay timer expires, the next packet in the replay buffer may be sent with an old sequence number. That packet is seen by receiver side as a duplicate and subsequently dropped. Note: This has only been reproduced in a synthetic test environment.

Implication: A fatal error may be registered by the GMCH and the system may hang.

Workaround: None.

Status: NoFix. For affected steppings, see the *Summary Table of Changes.*

22. PCI Express* Port Skip Sequence is Not Transmitted When Entering Recovery State

Problem: PCI Express* Port Skip Sequence in a non-common clock configuration is not transmitted when the skip latency counter expires exactly at the same time the GMCH is entering the recovery state. The GMCH sends the COM symbol (K28.5) followed by idles instead of skip sequence symbols.
Note: This has only been reproduced in a synthetic test environment and only applies to systems that use a non-common clock configuration.

Implication: None. Skip Sequence Symbol generation is not a requirement for proper operation in systems that implement common clock configurations.

Workaround: None

Status: NoFix. For affected steppings, see the *Summary Table of Changes.*

23. Malformed Upstream IO or Configuration Write Cycles Are Not Being Detected As Malformed

Problem: Malformed upstream IO or configuration write cycles are not being properly detected. The IO or configuration write cycles are put in the upstream non-posted queue as an invalid cycle and an unsupported request completion is returned instead of a fatal error.
Note: This has only been reproduced in a synthetic test environment.

Implication: None. PCI Express* 1.0a compliant devices are not allowed to send I/O or Configuration cycles upstream.

Workaround: None.

Status: NoFix. For affected steppings, see the *Summary Table of Change.*

24. The Transaction Layer Resets the Completion Timer Counter before Receiving a Passing CRC from the Link Layer on the PCI Express* Port

Problem: The PCI Express* Port is resetting the completion timer before receiving a Transaction Layer Packet (TLP) with a passing Cyclic Redundancy Check (CRC) indicator from the Link Layer. The completion timer should only be resetting when there is a passing CRC indicator from the Link Layer.
Note: This has only been reproduced in a synthetic test environment.

Implication: None.

Workaround: None.

Status: NoFix. For affected steppings, see the *Summary Table of Changes.*

25. Unintended SDVO Hot Plug Interrupt Events

Problem: When the SDVO_INT/INT# lines are routed adjacent to the SDVO CTRL Bus, the falling edge of the SDVO CTRL Bus may induce noise onto the SDVO_INT/INT# lines which may cause an unintended SDVO display hot plug interrupt at the GMCH.

Implication: Unintended SDVO display hot plug interrupts may be detected by the GMCH. This may result in performance degradation.

Workaround: Option A – Use 14.11 PV Driver. Option B. – Disable SDVO hot plug via VBIOS

Status: NoFix. For affected steppings, see the *Summary Table of Changes*.

§

Specification Changes

There are no specification clarifications in this Specification Update revision.

§

Specification Clarifications

There are no specification clarifications in this Specification Update revision.

§

Documentation Changes

There are no documentation changes in this Specification Update revision.

§