Intel® 440BX Scalable Performance Board

Development Kit Manual

July 2001

Order Number: 273318-007

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Revision History

Revision	Date	Description
007	7/01	Added power management section and replaced BIOS information.
006	4/01	Kits upgraded to ship with 850 MHz Celeron processor (replacing 566 MHz processor).
005	3/20/01	Expanded the Key Components BOM to include all kit contents other than packaging, documentation, cables, mounting hardware, etc. Changed baseboard part FB1-FB4, FB9 to BLM41P750S, 75 Ω/100 MHz/3 A (schematic and BOM change). Removed processor core voltages; see processor datasheets. BOM was reformatted.
004	01/01	Updated processor support.
003	8/00	Added support for the 850 MHz Pentium® III processor.
002	5/00	Added support for the 700 MHz Pentium® III processor and the 566 MHz Celeron™ processor. Changed document name. Removed references to specific video adapter card.
001	1/00	First publication of this document.

About this Manual 1

This manual tells you how to set up and use the evaluation board and processor assembly included in your Intel® 440BX Scalable Performance Board Development Kit.

1.1 Content Overview

Chapter 1, “About This Manual” - This chapter contains a description of conventions used in this manual. The last few sections tell you how to obtain literature and contact customer support.

Chapter 2, “Getting Started” - Provides complete instructions on how to configure the evaluation board and processor assembly by setting jumpers, connecting peripherals, providing power, and configuring the BIOS.

Chapter 3, “Theory of Operation” - This chapter provides information on the system design.

Chapter 4, “Hardware Reference” - This chapter provides a description of jumper settings and functions, and pinout information for each connector.

Chapter 5, “BIOS Quick Reference” - This chapter describes how to configure the BIOS for your system configuration. A summary of all BIOS menu options is provided.

Appendix A, “PLD Code Listing” - This appendix includes a sample code listing for the Post Code Debugger.

Appendix B, “Bill of Materials” - This appendix contains the bill of materials for the evaluation board.

Appendix C, “Schematics” - This appendix contains schematics for selected connectors and subsystems for the evaluation board.

1.2 Text Conventions

The following notations may be used throughout this manual.

#	The pound symbol (#) appended to a signal name indicates that the signal is active low.
Variables	Variables are shown in italics. Variables must be replaced with correct values.
Instructions	Instruction mnemonics are shown in uppercase. When you are programming, instructions are not case-sensitive. You may use either uppercase or lowercase.
Numbers	Hexadecimal numbers are represented by a string of hexadecimal digits followed by the character *H*. A zero prefix is added to numbers that begin with *A* through *F*. (For example, *FF* is shown as *0FFH*.) Decimal and binary numbers are represented by their customary notations. (That is, 255 is a decimal number and 1111 1111 is a binary number. In some cases, the letter *B* is added for clarity.)
Units of Measure	The following abbreviations are used to represent units of measure:

A	amps, amperes
Gbyte	gigabytes
Kbyte	kilobytes
KΩ	kilo-ohms
mA	milliamps, milliamperes
Mbyte	megabytes
MHz	megahertz
ms	milliseconds
mW	milliwatts
ns	nanoseconds
pF	picofarads
W	watts
V	volts
µA	microamps, microamperes
µF	microfarads
µs	microseconds
µW	microwatts

Signal Names	Signal names are shown in uppercase. When several signals share a common name, an individual signal is represented by the signal name followed by a number, while the group is represented by the signal name followed by a variable (*n*). For example, the lower chip-select signals are named CS0#, CS1#, CS2#, and so on; they are collectively called CS*n*#. A pound symbol (#) appended to a signal name identifies an active-low signal. Port pins are represented by the port abbreviation, a period, and the pin number (e.g., P1.0).

1.3 Technical Support

1.3.1 Electronic Support Systems

Intel's site on the World Wide Web (http://www.intel.com/) provides up-to-date technical information and product support. This information is available 24 hours per day, 7 days per week, providing technical information whenever you need it.

Product documentation is provided online in a variety of web-friendly formats at:

http://developer.intel.com/design/litcentr/index.htm

1.3.2 Telephone Technical Support

In the U.S. and Canada, technical support representatives are available to answer your questions between 5 a.m. and 5 p.m. PST. You can also fax your questions to us. (Please include your voice telephone number and indicate whether you prefer a response by phone or by fax). Outside the U.S. and Canada, please contact your local distributor.

1-800-628-8686	U.S. and Canada
916-356-7599	U.S. and Canada
916-356-6100 (fax)	U.S. and Canada

1.4 Product Literature

You can order product literature from the following Intel literature centers.

1-800-548-4725	U.S. and Canada
708-296-9333	U.S. (from overseas)
44(0)1793-431155	Europe (U.K.)
44(0)1793-421333	Germany
44(0)1793-421777	France
81(0)120-47-88-32	Japan (fax only)

1.5 Related Documents

Table 1. Related Documents

Document Title	Order Number
Intel® Pentium® III Processor for the PGA370 Socket at 500 MHz to 1 GHz datasheet	245264
Intel® Pentium® III Processor Specification Update	244453
P6 Family of Processors Hardware Developer's Manual	244001
Intel® Celeron™ Processor up to 850 MHz datasheet	243658
Intel® Celeron™ Processor Specification Update	243748
Intel® 440BX AGPset / PGA370 Scalable Performance Board Design Guide	273296
Intel Architecture Software Developer's Manual, Volume 1: Basic Architecture	243190
Intel Architecture Software Developer's Manual, Volume 2: Instruction Set Reference	243191
Intel Architecture Software Developer's Manual, Volume 3: System Programming Guide	243192
Intel® 440BX AGPset: 82443BX Host Bridge/Controller datasheet	290633
Intel® 440BX AGPset: 82443BX Host Bridge/Controller Specification Update	290639
Intel® 440BX AGPset: 82443BX Host Bridge/Controller Timing Specification	273218
82371AB (PIIX4) and 82371EB (PIIX4E) PCI-TO-ISA/IDE Xcelerator datasheet	290562
Intel 82371EB (PIIX4E) Specification Update	290635
Intel 82371AB PCI ISA IDE Xcelerator (PIIX4) Timing Specification	273135
CK97 Clock Synthesizer/Driver Design Guidelines	243867

Getting Started 2

This chapter identifies the Intel® 440BX Scalable Performance Board Development Kit's key components, features and specifications, and tells you how to set up the board for operation.

2.1 Overview

The evaluation board provided in your kit is a scalable board design. It supports 440BX AGPset-based designs with several different Intel processors and core voltages[1]:

- Intel® Pentium® III Processor at 600 MHz, 700 MHz and 850 MHz (FC-PGA package, 100 MHz processor system bus)
- Intel® Celeron™ Processor at 300A MHz, 366 MHz and 433 MHz (PPGA package, 66 MHz processor system bus)
- Intel® Celeron™ Processor at 566 MHz and 733 MHz (FC-PGA package, 66 MHz processor system bus)
- Intel® Celeron™ Processor at 850 MHz (FC-PGA package, 100 MHz processor system bus)
- All future PGA370-socketed Intel® Pentium® III and Celeron™ processors (.18µ and .25µ technologies)

This scalable board design provides an example of a single-platform solution that supports multiple processors. Following this example, OEMs can design products that are scalable over a broad range of Intel Pentium III and Celeron processors.

The evaluation board consists of a baseboard and a processor assembly.

- The processor assembly contains an 850 MHz Intel® Pentium® III Processor, an 82443BX Host Bridge/Controller and the supporting circuitry.
- The baseboard contains the 82371EB PCI ISA IDE Xcelerator (PIIX4E) and other system board components and peripheral connectors.

Warning: The processor assembly is attached to the baseboard at the factory. Do *not* remove the processor assembly from the baseboard. Intel will not support the processor assembly or the baseboard if any portion of the assembly is removed by the customer.

2.1.1 Processor Assembly Features

The processor assembly features are summarized below.

- Pentium III Processor in a FC-PGA package (PGA370) with 100-MHz system bus frequency
- Intel 440BX AGPset: 82443BX Host Bridge/Controller

1. Core voltages are specified in the Intel® Pentium® III and Celeron™ processor datasheets. See "Related Documents" on page 10. No jumpers are required to switch between voltages; the core voltage is automatically sensed by the regulation circuitry.

  - 100/66 MHz memory interface:
  - 64-bit memory data interface plus 8 ECC bits and hardware scrubbing
  - 60 ns EDO DRAM and 100/66 MHz SDRAM support
  - 16 Mbit and 64 Mbit DRAM technologies
- Five PCI masters
  - PCI Specification Rev 2.1 Compliant
- Accelerated Graphics Port (AGP) Support:
  - AGP Interface Specification Revision 1.0 compliant
  - 66/133 MHz, 3.3-V, AGP device support
- Integrated System Power Management support

2.1.2 Baseboard Features

- Flash system BIOS ROM
  - General Software system BIOS
  - In-circuit BIOS upgradability
- 32-Mbyte SDRAM DIMM included
  - 4 Mbyte x64, 3.3 V, 100 MHz with a CAS latency of 2
- User-accessible on-board connectors include:
  - Two SDRAM DIMM connectors
  - Two serial RS-232 ports; COM1, COM2
  - One EPP/ECP parallel port
  - PS/2 keyboard and PS/2 mouse (6-pin mini-DIN connectors)
  - Two USB ports
  - Two IDE bus connectors
  - One floppy connector
  - Three PCI expansion slots and two ISA expansion slots. There are no shared slots; all slots are usable.
  - One AGP connector
  - Standard ATX power supply connector
- Miscellaneous features include:
  - On-board post-code debugger (Port 80)
  - Reset push button
  - Stand-off feet for table-top operation

2.2 Included Hardware

- Evaluation board (baseboard and processor assembly combination)
- 4.3-Gbyte hard disk drive pre-loaded with the QNX Real Time Operating System*
- 32-Mbyte, 100-MHz SDRAM DIMM
- Attached heatsink and fan
- PCI video graphics adapter
- Intel® PRO/100+ Adapter - 82559-based Ethernet network adapter
- Mounting hardware
- IDE cable for the hard disk drive

2.3 Software Key Features

The software in the kit is included to facilitate development of real-time applications based on the components used in the evaluation board. The software tools included in your kit are described in this section.

Refer to the letter included in your kit for up to date information about other vendors offering development software for this kit.

Note: Software in the kit is provided free by the vendor and is only licensed for evaluation purposes. Customers using the tools that work with Microsoft products must have licensed those products. Any targets created by those tools should also have appropriate licenses. Software included in the kit is subject to change.

2.3.1 General Software, Inc.

General Software's Embedded BIOS* is a full-featured BIOS for x86-based handheld, applied computing, and volume consumer electronics applications. This product offers a winning combination of superior OEM configurability and superior embedded features.

Intel selected Embedded BIOS as the standard pre-installed pre-boot firmware for this design. The following features of Embedded BIOS have been enabled in this Intel development kit:

- SDRAM detection, configuration and initialization
- L2 cache configuration and initialization
- Intel 440BX Northbridge configuration and initialization
- PIIX4E Southbridge configuration and initialization
- POST codes displayed to POST code monitor
- Two serial ports, one EPP/ECP parallel port
- PCI bus and device enumeration and configuration
- AGP configuration and initialization
- SMC FDC37B787 Super I/O programming
- Integrated debugger

- Burn-in diagnostics
- Console redirection
- Manufacturing mode

2.3.2 QNX Software Systems, Ltd.

The QNX Real Time Operating System for Intel Architecture comes pre-loaded on the hard disk included in your kit.

- Small memory footprint of the QNX operating system with microGUI
- QNX microGUI is a full featured graphical user interface (GUI) and windowing system
- Photon Application Builder
- QNX Development kit provides the basic utilities to build and program Intel Flash
- Watcom C/C++ Development Suite*: is a full featured development suite
- Includes compiler, assembler and debugger with full support for the QNX microGUI function library
- Makes development of the QNX executables fast, easy and optimized

To use the QNX software, use the following password and username:

Username: Inteldemo
Password: QNX

Caution: Use the shutdown button to exit from QNX. Improper shutdown may result in the loss of the file system.

2.4 Before You Begin

Before you set up and configure your evaluation board, you may want to gather some additional hardware and software.

VGA Monitor	You can use any standard VGA or multi-resolution monitor. The setup instructions in this chapter assume that you are using a standard VGA monitor.
Power Supply	You must use an ATX-type PC power supply.
Keyboard	You need a keyboard with a PS/2-style connector or adapter.
Mouse	Optional. You can use a mouse with a PS/2-style connector or adapter.
Additional Drives	You can connect up to four IDE drives and two floppy drives to the evaluation board. Two devices (master and slave) can be attached to each IDE connector. You must provide the cables for these drives. You may have all these storage devices attached to the evaluation board at the same time.
Video Adapter	You can use the video adapter supplied with your kit, or you can use any other adapter. The evaluation board supports AGP, PCI and ISA video cards. You will have to install the correct drivers for video adapters other than the one provided.
Network Adapter	An Intel Pro 100+ Adapter network adapter is supplied with your kit. Drivers for this adapter are also provided. The evaluation board supports all standard PCI and ISA compatible network cards. You will have to install the correct drivers to use adapters not included in your kit.
Other Devices and Adapters	The evaluation board behaves much like a standard desktop computer motherboard. Most PC compatible peripherals can be attached and configured to work with the evaluation board. For example, you may want to install a sound card or AGP graphics card.

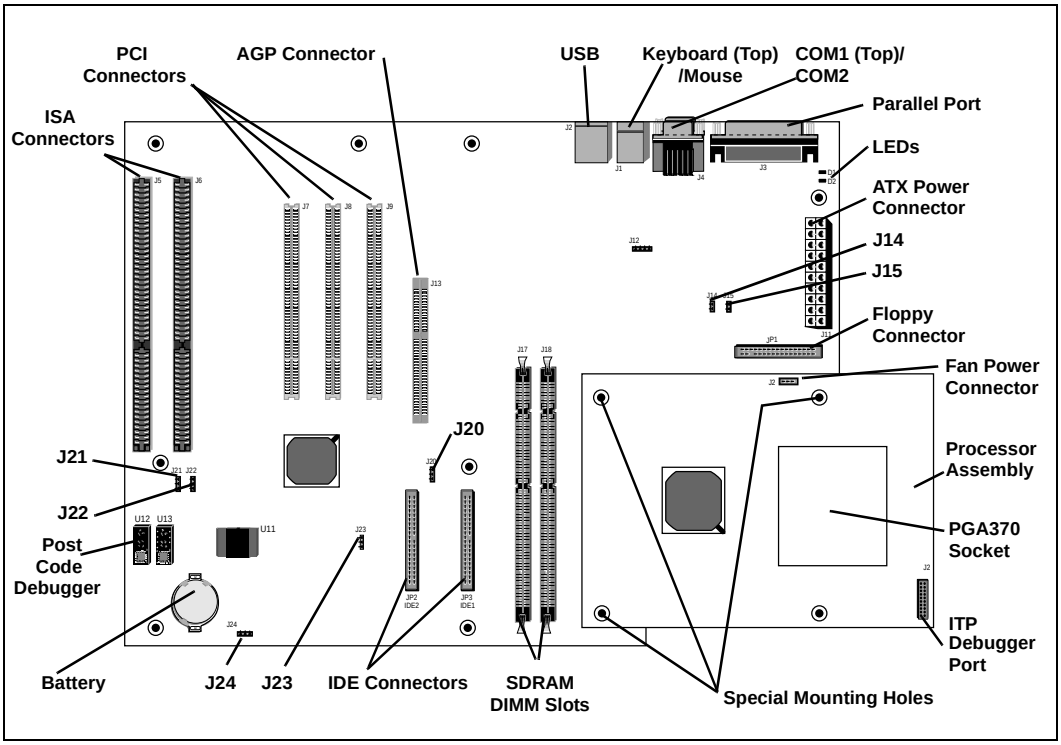
2.5 Setting up the Evaluation Board

Once you have gathered the hardware described in the last section, follow the steps below to set up your evaluation board. This manual assumes you are familiar with the basic concepts involved with installing and configuring hardware for a personal computer system. Refer to Figure 1 for the location of connectors, jumpers, etc.

1. Make sure you are in a static-free environment before removing any components from their anti-static packaging. The evaluation board is susceptible to electro-static discharge damage; such damage may cause product failure or unpredictable operation.
2. Inspect the contents of your kit. Check for damage that may have occurred during shipment. Contact your sales representative if any items are missing or damaged.

Caution: Connecting the wrong cable or reversing the cable can damage the evaluation board and may damage the device being connected. Since the evaluation board is not in a protective chassis, use caution when connecting cables to this product.

Figure 1. Evaluation Board Jumpers and Connectors



3. Make sure the evaluation board's jumpers are set to the following default locations.
   - J14 - Not installed
   - J15 - Not Installed
   - J20 - Jumper pins 2-3
   - J21 - Jumper pins 2-3
   - J22 - Jumper pins 2-3
   - J23 - Jumper pins 2-3
   - J24 - Jumper pins 1-2
4. Mount the hardware:
   - Table-top operation: The evaluation board is shipped with standoff "feet" for use in a table-top environment. These feet are installed on the evaluation board to raise it off the table surface.Your kit contains two bags of mounting hardware. One bag contains eight standoff feet, eight mounting screws, and eight washers. Another bag has three *shorter* feet that must be attached slightly differently.
     — To mount the eight standard feet, insert a washer onto a screw, then push the screw through the top of the board. From below the board, thread one of the longer feet onto the screw.
     — To mount the three special feet, screw the three *shorter* feet onto the existing screws. See Figure 1 for the location of the three special holes.

Warning: Do not remove the nuts from these three holes! This will detach the processor assembly from the baseboard, and Intel will no longer support the evaluation board.

Note: The evaluation board is not an ATX form factor.

5. Connect desired storage devices to the evaluation board:

   The evaluation board supports Primary and Secondary IDE interfaces that can each host one or two devices (master/slave). When you are using multiple devices, such as a hard disk and a CD-ROM drive, make sure the hard disk drive has a jumper in the master position and the CD-ROM has a jumper in the slave position. When you are using a single IDE device with the evaluation board, make sure that the jumper is set correctly for single master operation. For jumper settings for other configurations, consult the drive's documentation.

Note: The evaluation board BIOS only supports hard drives of 16 Gbytes or less.

- Installing the IDE hard disk drive included in your kit:
  — Connect the hard drive's IDE connector to the JP4 connector on the evaluation board. Be sure to align Pin 1 of the cable connector with pin 1 of JP4.
  — Connect the other end to the hard disk drive.

Caution: Make sure the tracer on the ribbon cable is aligned with pin 1 on both the hard disk and the IDE connector header. Connecting the cable backwards can damage the evaluation board or the hard disk.

— Connect the power supply to the hard drive.

Note: The hard disk is already formatted and is pre-loaded with the QNX Real-Time Operating System for Intel Architecture.

— You may have to make changes to the system BIOS to enable this hard disk. See Chapter 5, “BIOS Quick Reference” for more information.

- Floppy drive: A floppy disk drive connected to the evaluation board is the most direct method for loading software.
  - — Insert the floppy drive cable into JP1 (be sure to orient Pin 1 correctly).
  - — Connect the other end of the ribbon cable to the floppy drive.
  - — Connect a power cable to the floppy drive.
  - — You must make changes to the system BIOS to enable this floppy disk. See Chapter 5, “BIOS Quick Reference” for more information.

6. Make sure the SDRAM DIMM is installed in the socket labeled J18.
7. Connect a PS/2 mouse and keyboard (see Figure 1 for connector locations).

Note: J1 (on the baseboard) is a stacked PS/2 connector. The *bottom* connector is for the mouse and the *top* is for the keyboard.

8. Install the supplied PCI video adapter into one of the available PCI slots. Connect the monitor cable to the VGA port on the card.
9. Connect the power supply:
   - You’ll need a standard ATX PC power supply. Make sure the power supply is unplugged (or turned off), then connect the power supply cable to the power header (J11).

Note: Some ATX power supplies do not have an on/off switch. In this case remove jumper J20 before plugging in the ATX power connector. J20 controls an internal power supply on/off switch. When you are ready to apply power, insert the jumper on pins 2-3. You may want to wire this header up to a toggle switch for convenience.

10. Make sure the thermal solution is attached to the processor. Make sure the fan is plugged into the fan power connector (J2) on the processor assembly (see Figure 1 for connector location).

Turn on the power to the monitor and evaluation board. When the power is on you should see two power-indicator LEDs light up (located next to the ATX power connector in the upper right corner of the board; see Figure 1). Check to see that the fan on the processor is operating.

2.6 Configuring the BIOS

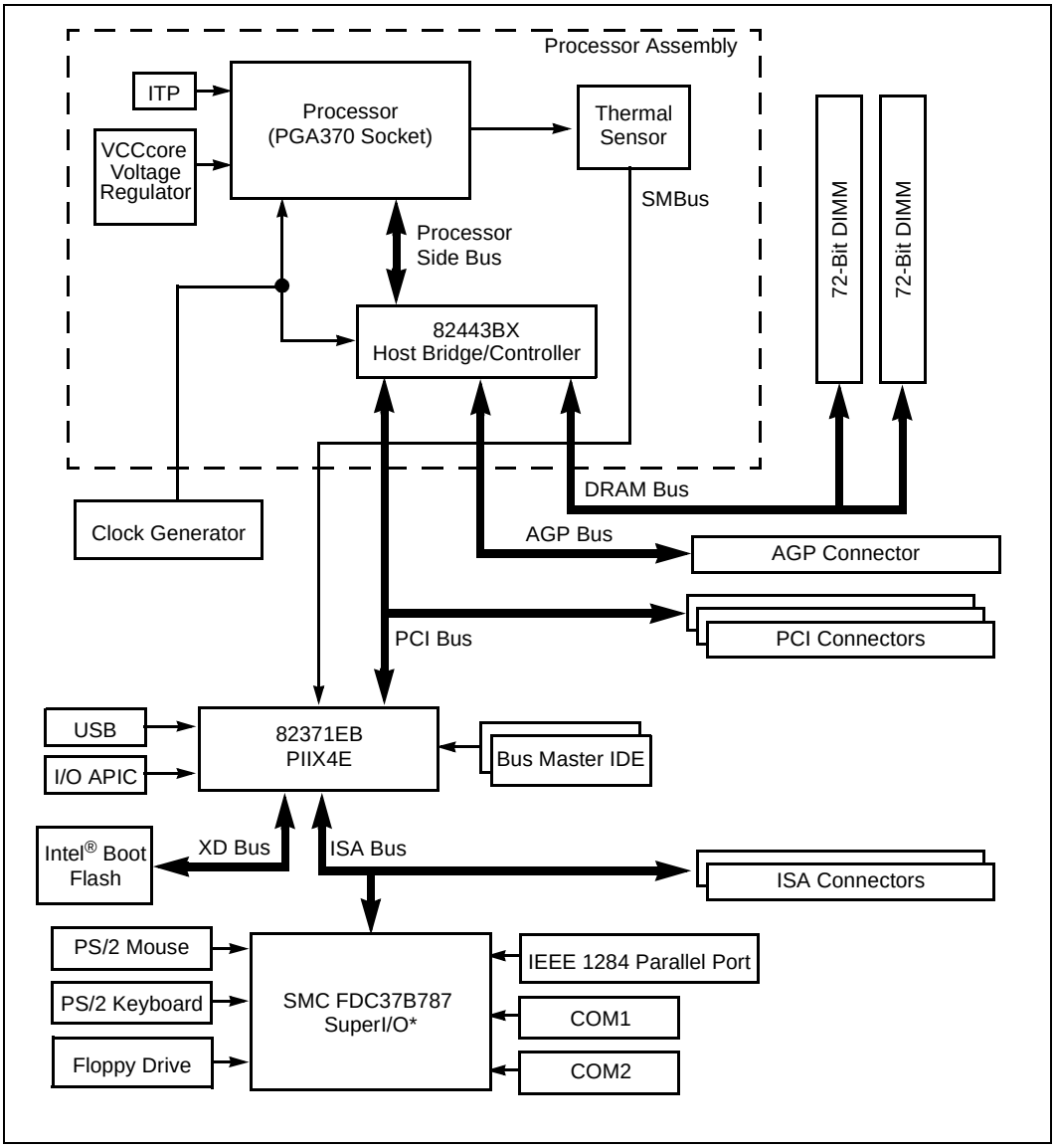
General Software’s BIOS software is pre-loaded on the evaluation board. You will have to make changes to the BIOS to enable hard disks, floppy disks and other supported features You can use the Setup program to modify BIOS settings and control the special features of the system. Setup options are configured through a menu-driven user interface. Chapter 5, “BIOS Quick Reference” contains a description of BIOS options.

BIOS updates may periodically be posted to Intel’s Developers’ web site at http://developer.intel.com/.

Theory of Operation 3

3.1 Block Diagram

Figure 2. Evaluation Board Block Diagram



3.2 System Operation

The evaluation board is a full-featured system board and processor assembly. The processor assembly includes an 850 MHz Pentium® III processor with 256 Kbytes of integrated L2 cache and the Intel 82443BX Host Bridge/Controller. The evaluation board contains the Intel 82371EB PCI-to-ISA/IDE Xcelerator (PIIX4E) and other system and I/O peripherals.

The evaluation board and processor assembly support other PGA370 socket processors. The customer may remove the Pentium III processor from the processor *socket* and replace it with another *supported* processor. The evaluation board automatically detects which processor is installed in the socket.

Warning: The processor assembly is attached to the baseboard at the factory. Do *not* remove the processor assembly from the baseboard. Intel will not support the processor assembly or the baseboard if any portion of the assembly is removed by the customer.

3.2.1 Supported Processors

An 850 MHz Pentium III processor is supplied in your kit. You may replace the supplied processor with one of the following:

- **600 and 700 MHz Pentium® III processor**. These processors have a 256-Kbyte integrated L2 cache, and support a 100-MHz processor system bus.
- **300A, 366 and 433, 566, 733 and 850 MHz Celeron™ processor**. These processors have a 128-Kbyte integrated L2 cache, and support a 66 MHz processor system bus (except for the 850 MHz Celeron processor, which has a 100 MHz processor system bus).
- Future PGA370-socketed Intel processors (.18µ and .25µ technologies) that support a 66 or 100 MHz processor system bus

3.2.1.1 Intel® Pentium® III Processor

The Pentium III processor for applied computing is offered at 600, 700 and 850 MHz with a processor system bus speed of 100 MHz. Refer to the processor datasheet for processor core voltage data (see “Related Documents” on page 10). The processor has an on-die second level cache bus that allows a high-performance 64-bit wide cache subsystem to be integrated on the same die as the processor. The processor can cache up to 4 Gbytes of memory using 128 Kbytes of L2 cache, 16 Kbytes of L1 data cache and 16 Kbytes of L1 code cache. The on-die first and second level cache operate at the same frequency and voltage as the processor core to improve performance and reduce total system power consumption.

3.2.1.2 Intel® Celeron™ Processor

The Intel Celeron Processor is offered at 300A, 366, 433, 566, 733 and 850 MHz. All processors have a processor system bus speed of 66 MHz, except for the 850 MHz version, which runs at 100 MHz. Refer to the processor datasheet for processor core voltage data (see “Related Documents” on page 10). The processor has an on-die second level cache bus that allows a high-performance 64-bit wide cache subsystem to be integrated on the same die as the processor. The processor can cache up to 4 Gbytes of memory using 128 Kbytes of L2 cache, 16 Kbytes of L1 data cache and 16 Kbytes of L1 code cache. The on-die first and second level cache operate at the same frequency and voltage as the processor core to improve performance and reduce total system power consumption. Additional features include: dynamic execution technology, Intel’s MMX™ media enhancement technology, Intel streaming SIMD extensions. At 566 MHz and higher, the processer is available in the FC-PGA package. 433 MHz and slower Celeron processors are offered in the PPGA package. Both packages are compatible with the 370-pin socket.

3.2.2 82443BX Host Bridge/Controller

The Intel® 440BX AGPset supports the Pentium III processor architecture. It interfaces with the processor system bus at 66 or 100 MHz. Along with its Host-to-PCI bridge interface, the 82443BX Host Bridge/Controller has been optimized with a 100/66 MHz SDRAM memory controller and data path unit. The 82443BX also features the Accelerated Graphics Port (AGP) interface. The 82443BX component includes the following functions and capabilities:

- 64-bit GTL+ based system data bus interface
- 32-bit system address bus support
- 64/72-bit main memory interface with optimized support for SDRAM
- 32-bit PCI bus interface with integrated PCI arbiter
- AGP interface with up to 133 MHz data transfer capability
- Extensive data buffering between all interfaces for high throughput and concurrent operations

3.2.2.1 System Bus Interface

The 82443BX supports a maximum of 4 Gbytes of memory address space from the processor perspective. The largest address size is 32 bits. The 82443BX provides bus control signals and address paths for transfers between the processor bus, PCI bus, Accelerated Graphics Port and main memory. The 82443BX supports a 4-deep-in-order queue, which provides support for pipelining of up to four outstanding transaction requests on the system bus.

For system bus-to-PCI transfers, the addresses are either translated or directly forwarded on the PCI bus, depending on the PCI address space being accessed. When the access is to a PCI configuration space, the processor I/O cycle is mapped to a PCI configuration space cycle. When the access is to a PCI I/O or memory space, the processor address is passed without modification to the PCI bus. Certain memory address ranges are dedicated for a graphics memory address space. When this space or a portion of it is mapped to main DRAM, the address is translated by the AGP address remapping mechanism and the request is forwarded to the DRAM subsystem. A portion of the graphics aperture can be mapped on the AGP, and the corresponding system bus cycles accessing that range are forwarded to the AGP without any translation. The AGP address map defines other system bus cycles that are forwarded to the AGP.

3.2.2.2 Accelerated Graphics Port (AGP) Interface

The 82443BX supports an AGP interface. The AGP interface has a maximum theoretical transfer rate of ~532 Mbytes/s.

3.2.2.3 System Clocking

The 82443BX operates the system bus interface at 66 or 100 MHz, the PCI bus at 33 MHz and the AGP at a transfer rate of 66/133 MHz. The 82443BX clocking scheme uses an external clock synthesizer that produces reference clocks for the system bus and PCI interfaces. The 82443BX generates the AGP and DRAM clock signals. Please refer to the *CK97 Clock Synthesizer/Driver Design Guidelines* (order number 243867).

3.2.3 In-Target Probe

The evaluation board is populated with a 2.5 V or 1.5 V In-Target Probe (ITP) debugger port. The ITP port provides a path for debugger tools like emulators, in-target probes, and logic analyzers to gain access to the processor registers and signals without affecting high speed operation. This allows the system to operate at full speed with the debugger attached.

Caution: When using a 300A, 366 or 433 MHz Celeron processor, you need to use a 2.5 V ITP plug. When using a 566 MHz or faster Celeron processor, or a Pentium III processor, you need to use a 1.5 V ITP plug. Using the wrong ITP voltage can damage the processor.

3.2.4 82371EB PCI to ISA/IDE Xcelerator (PIIX4E)

The 82443BX is designed to support the PIIX4E I/O bridge. The PIIX4E is a highly-integrated multifunctional component that supports the following:

- PCI Revision 2.1 compliant PCI-to-ISA bridge with support for 33-MHz PCI operations
- ACPI Power Management support
- Enhanced DMA controller, interrupt controller and timer functions
- Integrated IDE controller with Ultra DMA/33 support
- USB host interface with support for two USB ports
- System Management Bus (SMB) with support for DIMM Serial Presence Detect

3.2.5 DRAM

The evaluation board provides two 168-pin DIMM module connectors. The DRAM interface is a 64-bit data path that supports Synchronous DRAM (SDRAM). The DRAM interface supports 4 Mbytes to 256 Mbytes of 4-Mbit, 16-Mbit and 64-Mbit DRAM and SRAM technology (both symmetrical and asymmetrical). Parity is not supported. One 100 MHz, 32-Mbyte SDRAM DIMM is included in the kit.

3.2.6 Power

The evaluation board uses an industry standard ATX-style power supply with a 20-pin connector. A 230-watt (minimum) supply is recommended. Note that the ATX power connector is keyed to prevent incorrect insertion. See “ATX Power Connector” on page 29 for a detailed description of the power connector.

Make sure that the ATX power supply is *not* plugged into the wall when connecting or disconnecting it from the evaluation board.

3.2.7 Power Management

Some hardware in the kit may support power management, but the Intel® 440BX Scalable Performance Board Development Kit as a whole does not support power management. Also note that power management has not been tested on the kit.

3.2.8 Boot ROM

The system boot ROM installed at U11 is a 2-Mbit (28F002BC) or 4-Mbit (E28F004B5T60) flash device. The system is set up for in-circuit reprogramming of the BIOS, but the flash device is also socketed. This device is addressable on the XD bus extension of the ISA bus.

3.2.9 RTC/NVRAM

The RTC and NVRAM are contained within the 82371EB PIIX4E device. CMOS NVRAM backup is provided by a 3-V lithium-ion battery.

3.2.10 Legacy I/O

Support for legacy I/O functions is provided by the Intel 82371EB PIIX4E and the SMC FDC37B787 SuperI/O* device.

3.2.11 IDE Support

The evaluation board supports both a primary and secondary IDE interface via two 40-pin IDE connectors. The connector labeled IDE1 is the primary interface. IDE2 is the secondary interface.

3.2.12 Floppy Disk Support

Floppy disk support is provided by the SMC FDC37B787 SuperI/O device. One 34-pin floppy connector is provided on the evaluation board.

3.2.13 Keyboard/Mouse

Keyboard and mouse support are provided by the SMC FDC37B787 SuperI/O device. The keyboard and mouse connectors (J1) are PS/2-style, 6-pin stacked miniature DIN connectors. The top connector is for the keyboard and the bottom connector is for the mouse.

3.2.14 USB

USB support is provided through the 82371EB PCI-to-ISA/IDE Xcelerator (PIIX4E) and can be used through connector J2.

3.2.15 RS232 Ports

Two serial I/O ports provided by the SMC FDC37B787 SuperI/O device. Two 9-pin RS232 connectors are provided on a single stacked connector (J4).

3.2.16 IEEE 1284 Parallel Port

One 25-pin IEEE 1284 parallel port connector controlled by the SMC FDC37B787 SuperI/O device is provided (J3).

3.2.17 PCI Connectors

Three industry standard 32-bit, 5-V PCI connectors are provided on the evaluation board. The connectors are designed to handle either a 5-V only card or a universal card. 3.3-V cards are not supported.

3.2.18 ISA Connectors

Two 16-bit ISA connectors are provided on the evaluation board.

3.2.19 AGP Connector

AGP support is provided through the 82443BX Host Bridge/Controller. One industry standard AGP connector (J13) is provided on the evaluation board.

3.2.20 Post Code Debugger

The evaluation board has an on-board Post Code Debugger. Data from any program that does an I/O write to 0080H is latched and displayed on the two LEDs (U12 and U13). During BIOS startup, codes are posted to these LEDs to indicate what the BIOS is doing. Application programs can post their own data to these LEDs by writing to I/O address 0080H.

3.2.21 Clock Generation

There are two devices on the baseboard which generate and distribute the clocks used by the entire system. These are the CY2280 clock synthesizer and the CY2318NZ clock buffer.

The CY2280 generates the clocks for the PGA370 processor, Host Bridge/Controller, cache, PCI, USB and ISA bus. The processor side bus clock runs at 66 or 100 MHz. The PCI clocks run at 33 MHz. This device is capable of spread spectrum clocking. If spread spectrum clocking is enabled, a 0.5% down spread will be introduced in the processor and PCI clocks.

The CY2318NZ clock buffer is used to buffer the clock signals sent to the SDRAM DIMMS. The SDRAM interface operates at 66 or 100 MHz.

3.2.22 Interrupt Map

Table 2. Interrupts

IRQ	System Resources
NMI	I/O Channel Check
0	Reserved, Interval Timer
1	Reserved, Keyboard buffer full
2	Reserved, Cascade interrupt from slave PIC
3	Serial Port 2
4	Serial Port 1
5	Parallel Port (PNP0 option)
6	Floppy
7	Parallel Port 1
8	Real Time Clock
9	IRQ2 Redirect
10	Reserved. Not supported.
11	Reserved. Not supported.
12	Onboard Mouse Port if present, else user available
13	Reserved, Math coprocessor
14	Primary IDE if present, else user available
15	Reserved. Not supported.

3.2.23 Memory Map

Table 3. Memory Map

Address Range (Hex)	Size	Description
100000-8000000	127.25M	Extended Memory
E0000-FFFFF	128K	BIOS
C8000-DFFFF		Available expansion BIOS area (Flash disk memory window)
A0000-C7FFF		Off-board video memory and BIOS
9FC00-9FFFF	1K	Extended BIOS Data (movable by QEMM, 386MAX)
80000-9FBFF	127K	Extended conventional
00000-7FFFF	512K	Conventional

Hardware Reference 4

This section provides reference information on the system design. Included in this section is connector pinout information, jumper settings, and other system design information.

4.1 Processor Assembly

The processor assembly contains the Pentium® III processor, the 82443BX Host Bridge/Controller, a voltage regulator and an ITP debugger connector. The assembly connects to the baseboard via a 400-pin connector.

Warning: The processor assembly is attached to the baseboard at the factory. Do *not* remove the processor assembly from the baseboard. Intel will not support the processor assembly or the baseboard if any portion of the assembly is removed by the customer.

4.1.1 Thermal Management

The objective of thermal management is to ensure that the temperature of each component is maintained within specified functional limits. The functional temperature limit is the range within which the electrical circuits can be expected to meet their specified performance requirements. Operation outside the functional limit can degrade system performance and cause reliability problems.

Important: The evaluation kit contains a heatsink and fan attached to the top of the processor. This thermal solution has been tested in an open air environment at room temperature and is sufficient for *evaluation purposes only.* It is up to the designer to provide adequate thermal management for any designs derived from the schematics provided in your kit.

4.1.2 In-Target Probe Debugger Port

The evaluation platform is populated with a 1.5 V/2.5 V ITP debugger port. The ITP port provides a path for debugger tools like emulators, in-target probes, and logic analyzers to gain access to the processor's registers and signals without affecting high speed operation. This allows the system to operate at full speed with the debugger attached.

Caution: When using a 300A, 366 or 433 MHz Celeron™ processor, you need to use a 2.5 V ITP plug. When using a 566 MHz or faster Celeron processor, or a Pentium III processor, you need to use a 1.5 V ITP plug. Using the wrong ITP voltage can damage the processor.

4.2 Post Code Debugger

The evaluation board has an on-board Post Code Debugger. Data from any code that does an I/O write to 80H is latched on the two led displays (U12/U13). During BIOS startup, code is posted to these LEDs to indicate what the BIOS is doing. Application code can post its own data to these LEDs by doing an I/O write to address 80H. The 22V10 PLD code used to implement this function is included in Appendix A, “PLD Code Listing.”

4.3 ISA and PCI Expansion Slots

The evaluation platform has three PCI expansion slots and two ISA slots.

4.4 PCI Device Mapping

On the evaluation platform the PCI devices are mapped to PCI device numbers by connecting an address line to the IDSEL signal of each PCI device. Table 4 shows the mapping of PCI devices.

Table 4. PCI Device Mapping

Device	Address Line	PCI Device Number
PIIX4E	AD18	7
PCI Slot 0 (J7)	AD28	17
PCI Slot 1 (J8)	AD29	18
PCI Slot 2 (J9)	AD30	19

4.5 Connector Pinouts

4.5.1 ATX Power Connector

Table 5 shows the signals assigned to the ATX style power connector.

Table 5. Primary Power Connector (J11)

Pin	Name	Function
1	3.3 V	3.3 V
2	3.3 V	3.3 V
3	GND	Ground
4	+5V	+5 V VCC
5	GND	Ground
6	+5V	+5 V VCC
7	GND	Ground
8	PWRGD	Power Good
9	5VSB	Standby 5 V
10	+12 V	+12 V
11	3.3 V	3.3 V
12	–12 V	–12 V
13	GND	Ground
14	PS_ON#	Soft-off control
15	GND	Ground
16	GND	Ground
17	GND	Ground
18	–5 V	–5 Volts
19	+5 V	+5 V VCC
20	+5 V	+5 V VCC

4.5.2 ITP Debugger Connector

Table 6. ITP 1.5 V Receptacle Connector Pin Assignment (J2 on the Processor Assembly)

Pin	Signal	Pin	Signal
1	GND	16	GND
2	RESET#	17	PRDY0#
3	GND	18	GND
4	DBRESET#	19	PREQ1#
5	GND	20	GND
6	TCK	21	PRDY1#
7	TDI	22	GND
8	TMS	23	PREQ2#
9	TDO	24	GND
10	POWERON	25	PRDY2#
11	TRST#	26	GND
12	DBINST#	27	PREQ3#
13	BSEN#	28	GND
14	GND	29	PRDY3#
15	PREQ0#	30	BCLK

4.5.3 Stacked USB

P0 is the bottom connector. P1 is on top.

Table 7. USB Connector Pinout (J2)

Pin	P0 Signals	P1 Signals
1	VCC0	VCC1
2	D0-	D1-
3	D0+	D1+
4	GND0	GND1

4.5.4 Mouse and Keyboard Connectors

The keyboard port is on top. The mouse port is on the bottom.

Table 8. Keyboard and Mouse Connector Pinouts (J1 on the Baseboard)

Pin	Signal Name
1	Data
2	No Connect
3	Ground
4	+5 V (fused)
5	Clock
6	No Connect

4.5.5 Parallel Port

Table 9. DB25 Parallel Port Connector Pinout (J3)

Pin	Signal Name	Pin	Signal Name
1	Strobe#	14	Auto Feed#
2	Data Bit 0	15	Fault#
3	Data Bit 1	16	INIT#
4	Data Bit 2	17	SLCT IN#
5	Data Bit 3	18	Ground
6	Data Bit 4	19	Ground
7	Data Bit 5	20	Ground
8	Data Bit 6	21	Ground
9	Data Bit 7	22	Ground
10	ACK#	23	Ground
11	Busy	24	Ground
12	Paper end	25	Ground
13	SLCT		

4.5.6 Serial Ports

COM1 is the top connector. COM2 is the bottom connector.

Table 10. Serial Port Connector Pinout (J4)

Pin	Signal Name
1	DCD
2	Serial In (SIN)
3	Serial Out (SOUT)
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI

4.5.7 IDE Connector

Table 11. PCI IDE1 (JP3) and IDE2 (JP4) Connector

Pin	Signal Name	Pin	Signal Name
1	Reset IDE	2	Ground
3	Host Data 7	4	Host Data 8
5	Host Data 6	6	Host Data 9
7	Host Data 5	8	Host Data 10
9	Host Data 4	10	Host Data 11
11	Host Data 3	12	Host Data 12
13	Host Data 2	14	Host Data 13
15	Host Data 1	16	Host Data 14
17	Host Data 0	18	Host Data 15
19	Ground	20	Key
21	DRQ3	22	Ground
23	I/O Write#	24	Ground
25	I/O Read#	26	Ground
27	IOCHRDY	28	BALE
29	DACK3#	30	Ground
31	IRQ14	32	IOCS16#
33	Addr 1	34	Ground
35	Addr 0	36	Addr 2
37	Chip Select 0#	38	Chip Select 1#
39	Activity	40	Ground

4.5.8 Floppy Drive Connector

Table 12. Diskette Drive Header Connector (JP1)

Pin	Signal Name	Pin	Signal Name
1	Ground	2	FDHDIN
3	Ground	4	Reserved
5	Key	6	FDEDIN
7	Ground	8	Index
9	Ground	10	Motor Enable A#
11	Ground	12	Drive Select B#
13	Ground	14	Drive Select A#
15	Ground	16	Motor Enable B#
17	Ground	18	DIR#
19	Ground	20	STEP#
21	Ground	22	Write Data#
23	Ground	24	Write Gate#
25	Ground	26	Track 00#
27	Ground	28	Write Protect#
29	Ground	30	Read Data#
31	Ground	32	Side 1 Select#
33	Ground	34	Diskette Change#

4.5.9 PCI Slot Connector

Table 13. PCI Slots (J7, J8, J9)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	VCC	B1	- 12V	A32	AD16	B32	AD17
A2	+ 12V	B2	GND	A33	3.3V	B33	CBE2#
A3	VCC	B3	GND	A34	FRAME#	B34	GND
A4	VCC	B4	No Connect	A35	GND	B35	IRDY#
A5	VCC	B5	VCC	A36	TRDY#	B36	3.3 V
A6	PIRQ1#	B6	VCC	A37	GND	B37	DEVSEL#
A7	PIRQ3#	B7	PIRQ2#	A38	STOP#	B38	GND
A8	VCC	B8	PIRQ0	A39	3.3 V	B39	LOCK#
A9	No Connect	B9	PRSNT1B#	A40	SDONE	B40	PERR#
A10	VCC	B10	No Connect	A41	SBO#	B41	3.3 V
A11	No Connect	B11	PRSNT2B#	A42	GND	B42	SERR#
A12	GND	B12	GND	A43	PAR	B43	3.3V
A13	GND	B13	GND	A44	AD15	B44	CBE1#
A14	No Connect	B14	No Connect	A45	3.3V	B45	AD14
A15	RST#	B15	GND	A46	AD13	B46	GND
A16	VCC	B16	PCLK3	A47	AD11	B47	AD12
A17	GNT1#	B17	GND	A48	GND	B48	AD10
A18	GND	B18	REQ#	A49	AD9	B49	GND
A19	Reserved	B19	VCC	A50	KEY	B50	KEY
A20	AD30	B20	AD31	A51	KEY	B51	KEY
A21	3.3V	B21	AD29	A52	CBEO#	B52	AD8
A22	AD28	B22	GND	A53	3.3 V	B53	AD7
A23	AD26	B23	AD27	A54	AD6	B54	3.3 V
A24	GND	B24	AD25	A55	AD4	B55	AD5
A25	AD24	B25	3.3 V	A56	GND	B56	AD3
A26	IDSEL	B26	CBE3#	A57	AD2	B57	GND
A27	3.3V	B27	AD23	A58	AD0	B58	AD1
A28	AD22	B28	GND	A59	VCC	B59	VCC
A29	AD20	B29	AD21	A60	REQ64#	B60	ACK64#
A30	GND	B30	AD19	A61	VCC	B61	VCC
A31	AD18	B31	3.3 V	A62	VCC	B62	VCC

4.5.10 ISA Slot Connector

Table 14. ISA Slots (J5, J6)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	IOCHK#	B1	GND	A26	SA5	B26	DACK2#
A2	SD7	B2	RSTSLOT	A27	SA4	B27	TC
A3	SD6	B3	VCC	A28	SA3	B28	BALE
A4	SD5	B4	IRQB9	A29	SA2	B29	VCC
A5	SD4	B5	–5V	A30	SA1	B30	OSC
A6	SD3	B6	DREQ2	A31	SA0	B31	GND
A7	SD2	B7	–12V	C1	SBHE#	D1	MEMCS16#
A8	SD1	B8	ZEROWS#	C2	LA23	D2	IOCS16#
A9	SD0	B9	+12V	C3	LA22	D3	IRQB10
A10	IOCHRDY	B10	GND	C4	LA21	D4	IRQB11
A11	AEN	B11	SMEMW#	C5	LA20	D5	IRQB11
A12	SA19	B12	SMEMR#	C6	LA19	D6	IRQ15
A13	SA18	B13	IOW#	C7	LA18	D7	IRQ14
A14	SA17	B14	IOR#	C8	LA17	D8	DACK0
A15	SA16	B15	DACK3#	C9	MEMR#	D9	DREQ0
A16	SA15	B16	DREQ3	C10	MEMW#	D10	DACK5
A17	SA14	B17	DACK1#	C11	SD8	D11	DREQ5
A18	SA13	B18	DREQ1	C12	SD9	D12	DACK6#
A19	SA12	B19	REFRESH#	C13	SD10	D13	DREQ6
A20	SA11	B20	SYSCLK	C14	SD11	D14	DACK7#
A21	SA10	B21	IRQA7	C15	SD12	D15	DREQ7#
A22	SA9	B22	IRQA6	C16	SD13	D16	VCC
A23	SA8	B23	IRQA5	C17	SD14	D17	MASTER#
A24	SA7	B24	IRQA4	C18	SD15	D18	GND
A25	SA6	B25	IRQA3				

4.6 AGP Connector

Table 15. AGP Slot (J13)

Pin#	B	A	Pin#	B	A
1	OVRCNT#	12V	34	Vddq3.3	Vddq3.3
2	5.0V	TYPEDET#	35	AD21	AD22
3	5.0V	Reserved	36	AD19	AD20
4	USB+	USB-	37	GND	GND
5	GND	GND	38	AD17	AD18
6	INTB#	INTA#	39	C/BE2#	AD16
7	CLK	RST#	40	Vddq3.3	Vddq3.3
8	REQ#	GNT#	41	IRDY#	FRAME#
9	VCC3.3	VCC3.3	42	3.3Vaux	Reserved
10	ST0	ST1	43	GND	GND
11	ST2	Reserved	44	Reserved	Reserved
12	RBF#	PIPE#	45	VCC3.3	VCC3.3
13	GND	GND	46	DEVSEL#	TRDY#
14	Reserved	Reserved	47	Vddq3.3	STOP#
15	SBA0	SBA1	48	PERR#	PME#
16	VCC3.3	VCC3.3	49	GND	GND
17	SBA2	SBA3	50	SERR#	PAR
18	SB_STB	Reserved	51	C/BE1#	AD15
19	GND	GND	52	Vddq3.3	Vddq3.3
20	SBA4	SBA5	53	AD14	AD13
21	SBA6	SBA7	54	AD12	AD11
22	KEY	KEY	55	GND	GND
23	KEY	KEY	56	AD10	AD9
24	KEY	KEY	57	AD8	C/BE0#
25	KEY	KEY	58	Vddq3.3	Vddq3.3
26	AD31	AD30	59	AD_STB0	Reserved
27	AD29	AD28	60	AD7	AD6
28	VCC3.3	VCC3.3	61	GND	GND
29	AD27	AD26	62	AD5	AD4
30	AD25	AD24	63	AD3	AD2
31	GND	GND	64	Vddq3.3	Vddq3.3
32	AD_STB1	Reserved	65	AD1	AD0
33	AD23	C/BE3#	66	Reserved	Reserved

NOTES:
1. Reserved pins are only for future use by the AGP interface specification.
2. IDSEL# is not a pin on the AGP connector. AGP graphics components should connect the AD16 signal to the 3. 3 volt IDSEL# function internal to the component.
3. All 3.3 volt cards leave the TYPEDET signal open. All 1.5 volt cards tie this signal hard to ground.

4.7 Jumpers

Table 16 shows default Jumper settings.

Table 16. Default Jumper Settings

Jumper	Function	Settings
J14	Enable Spread Spectrum Clocking	In – Enable Spread Spectrum Out – Disable Spread Spectrum (Default)
J15	Clock Frequency Selection	In – Reserved Out – Autodetects the processor side bus frequency (Default)
J20	On/Off	1–2 Reserved 2–3 On (Default) No Jumper Installed – Off
J21	Flash BIOS VPP Select	1–2 12 V 2–3 5 V (Default)
J22	Flash BIOS boot block control	1–2 12 V 2–3 5 V (Default)
J23	SMI# Source	1–2 Reserved 2–3 SMI# controlled by PIIX4E (Default)
J24	CMOS RAM Clear	1–2 Normal Operation (Default) 2–3 Clear CMOS RAM

4.7.1 Enable Spread Spectrum Clocking (J14)

This jumper is used to enable or disable spread spectrum clocking on the clock synthesizer. When this jumper is in, a 0.5% down spread will be introduced into the PCI and processor clocks. The default setting is no jumper installed, which disables spread spectrum clocking.

4.7.2 Clock Frequency Selection (J15)

This jumper controls the frequency of the processor clock. When the jumper is out, the processor side bus is automatically configured. This is the default setting.

4.7.3 On/Off (J20)

This jumper is used to control the state of the ATX power supply. When this jumper is removed, the power supply will be turned off. Placing the jumper in the 2-3 position will turn the power supply on.

The 1-2 position is reserved and should not be used.

4.7.4 Flash BIOS VPP Select (J21)

This jumper controls the voltage presented to the flash BIOS VPP pin. The 2-3 position supplies 5 V and is the default for normal operation. This position inhibits programming or erasing the flash BIOS.

The 1-2 position supplies 12 V and should only be used if directed to do so by a utility that is used to reprogram the BIOS.

4.7.5 Flash BIOS Boot Block Control (J22)

This jumper controls the Boot Block protection of the flash BIOS. When this jumper is in the 2-3 position, the boot block is locked and cannot be programmed. This is the default position of this jumper.

The 1-2 position unlocks the boot block so that it can be erased and reprogrammed. This position should only be used under the direction of a utility that is designed to reprogram the boot block of the flash device.

4.7.6 SMI# Source Control (J23)

This jumper selects the source of the SMI# interrupt to the processor. Only the 2-3 position which selects the PIIX4E is supported. The 1-2 position is reserved for future use.

4.7.7 CMOS RAM Clear (J24)

This jumper controls power to the battery backed-up CMOS RAM. This RAM is used to store information about the system configuration that is required by the BIOS. The 1-2 position is for normal operation. The 2-3 position allows for the RAM to be cleared.

To clear the RAM perform the following steps:

1. Remove power from the evaluation platform by removing jumper J20.
2. Move J24 to the 2-3 position.
3. Disconnect the power supply (J11).
4. Install J24 in the 1-2 position.
5. Reconnect the power supply (J11).
6. Reboot the system and enter the BIOS setup screen to configure the system.

4.7.8 Push Button Switches

There are two push button switches on the evaluation board labeled S1 and S2.

- S1 is non-functional and reserved for future use.
- S2 is the reset button. Press S2 to force a hardware reset of the system.

4.8 In-Circuit BIOS Update

The BIOS can be upgraded in-circuit. BIOS updates may periodically be posted to Intel's Developers' site at http://www.intel.com/design/.

To reprogram the BIOS:

1. Set Jumper J21 and Jumper J22 to the 1-2 position on the evaluation platform.
2. Download the new BIOS upgrade file from Intel's Developers' web site.
3. Extract the BIOS upgrade zip file onto a bootable floppy.
4. Insert the floppy disk into the floppy drive attached to the evaluation board.
5. Reboot the evaluation board so that it boots from the floppy.
6. Follow the on-screen instructions.
7. When the BIOS update program is finished, power down the board and reset the jumpers at J21 and J22 to the 2-3 position.

BIOS Quick Reference 5

The evaluation board is licensed with a single copy of Embedded BIOS and Embedded DOS software from General Software, Inc.[1] This software is provided for demonstration purposes only and must be licensed directly from General Software, Inc. for integration with new designs. General Software may be reached at (800) 850-5755, on the web at http://www.gensw.com, or via email at sales@gensw.com.

BIOS updates may periodically be posted to the Intel Developers' web site at http://developer.intel.com/.

5.1 BIOS and Pre-Boot Features

The system's pre-boot environment is managed with an adaptation of Embedded BIOS from General Software. The pre-boot environment includes POST, Setup Screen System, Manufacturing Mode, Console Redirection, Windows CE Loader (CE Ready), and Integrated BIOS Debugger. A REFLASH tool is also available to update the BIOS image with new builds of Embedded BIOS that may be obtained from General Software.

Before using the system, please read the following to properly configure CMOS settings, and learn how to use the embedded features of the pre-boot firmware, Embedded BIOS.

The last two sections of this chapter provide the BIOS POST Codes and Beep codes.

5.2 Power-On Self-Test (POST)

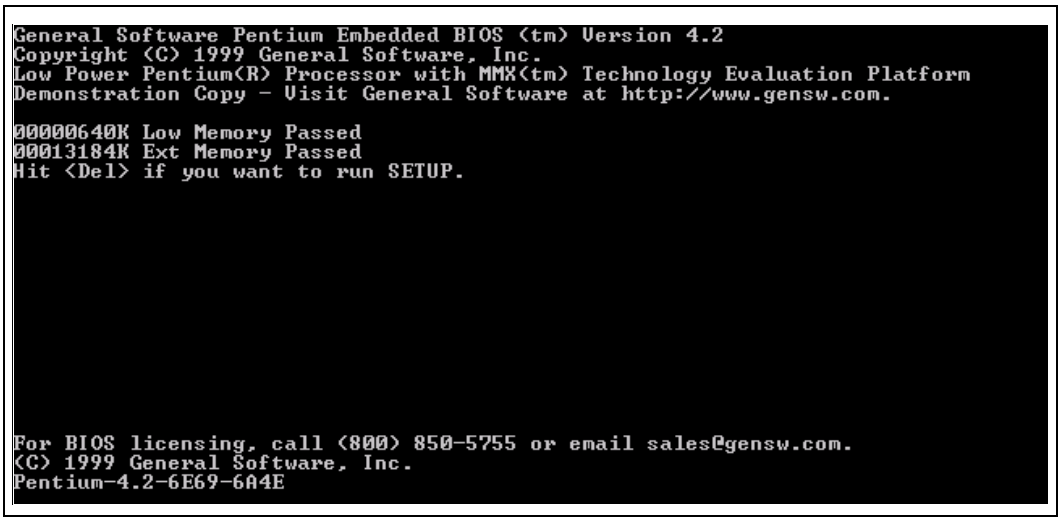
When the system is powered on, Embedded BIOS tests and initializes the hardware and programs the chipset and other peripheral components. During this time, POST progress codes are written by the system BIOS to I/O port 80H, allowing the user to monitor the progress with a special monitor. "Embedded BIOS POST Codes" on page 52 lists the POST codes and their meanings.

During early POST, no video is available to display error messages should a critical error be encountered; therefore, POST uses beeps on the speaker to indicate the failure of a critical system component during this time. Consult "Embedded BIOS Beep Codes" on page 55 for a list of Beep codes used by the system's BIOS.

POST displays its progress on the system video device, which may be the video screen if a VGA card is used, or on a terminal emulation program's screen if output is redirected over a serial port.

1. General Software™, the GS Logo, Embedded BIOS™, BIOStart™, CE-Ready™, and Embedded DOS™ are trademarks or registered trademarks of General Software, Inc.

Figure 3. BIOS POST Pre-Boot Environment



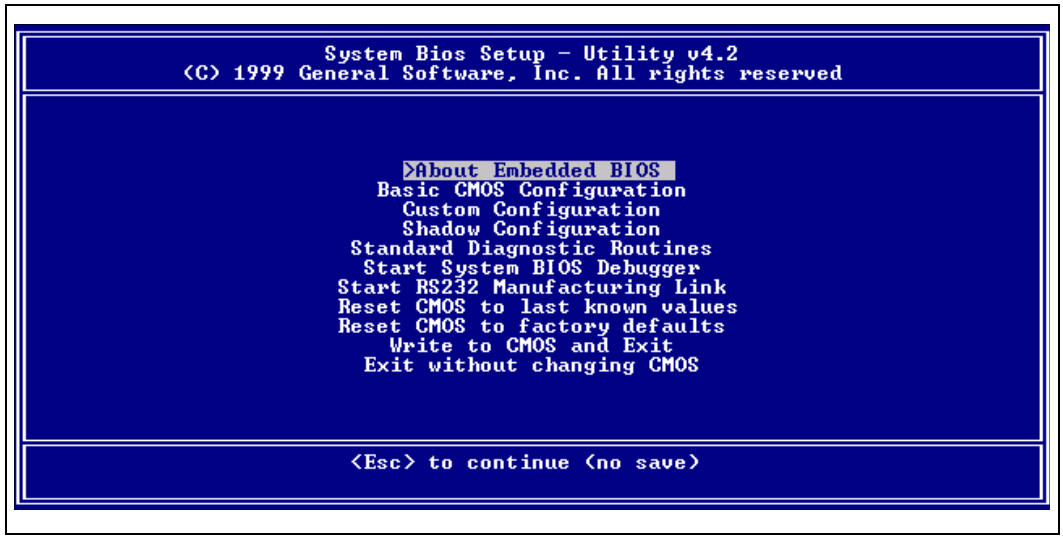
When the system is powered on for the first time, you'll need to configure the system through the Setup Screen System (described later) before peripherals, such as disk drives, are recognized by the BIOS. The information is written to battery-backed CMOS RAM on the board's Real Time Clock. Should the board's battery fail, this information will be lost and the board will need to be reconfigured.

OEMs can modify the look-and-feel of POST with the Embedded BIOS adaptation kit. While the demonstration BIOS looks and feels like a desktop PC, it is possible to eliminate messages, sounds, delays, to make the POST effectively invisible.

5.3 Setup Screen System

The system is configured from within the Setup Screen System, which is a series of menus that can be invoked from POST by pressing the <DEL> key if the main keyboard is being used, or by pressing ^C if the console is being redirected to a terminal program.

Figure 4. Embedded BIOS Setup Screen Menu

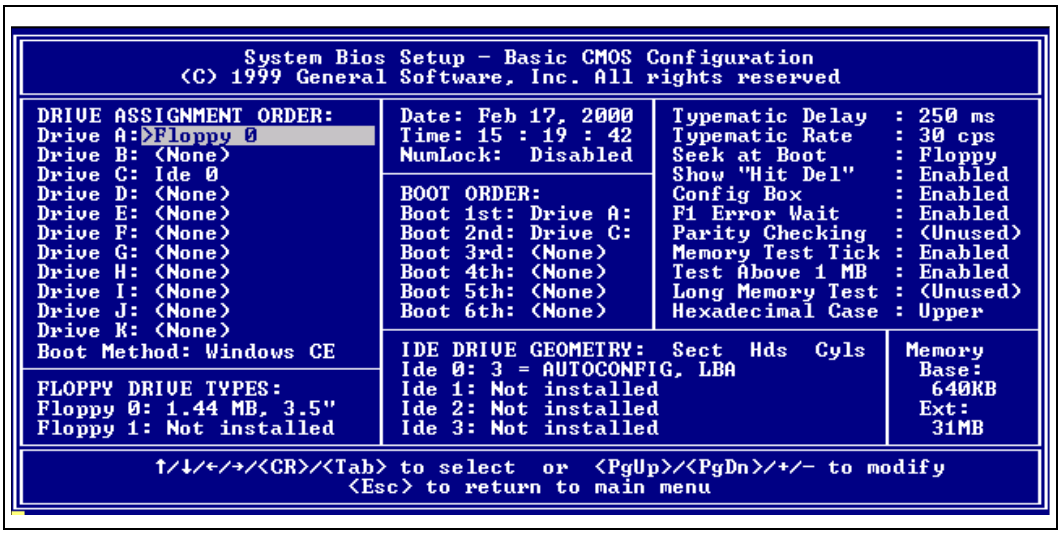


Once in the Setup Screen System (Figure 4), the user can navigate with the UP and DOWN arrow keys from the main console, or use the ^E and ^X keys from the remote terminal program to accomplish the same thing. TAB and ENTER are used to advance to the next field, and '+' and '-' keys cycle through values, such as those in the Basic Setup Screen, or the Diagnostics Setup Screen.

5.3.1 Basic CMOS Configuration Screen

The system's drive types, boot activities, and POST optimizations are configured from the Basic Setup Screen (Figure 5). In order to use disk drives with your system, you must select appropriate assignments of drive types in the left-hand column. Then, if you are using true floppy and IDE drives (not memory disks that emulate these drives), you need to configure the drive types themselves in the Floppy Drive Types and IDE Drive Geometry sections. Finally, you'll need to configure the boot sequence in the middle of the screen. Once these selections have been made, your system is ready to use.

Figure 5. Embedded BIOS Basic Setup Screen



5.3.2 Configuring Drive Assignments

Embedded BIOS allows the user to map a different file system to each drive letter. The BIOS allows file systems for each floppy (Floppy0 and Floppy1), each IDE drive (Ide0, Ide1, Ide2, and Ide3), and memory disks when configured (Flash0, ROM0, RAM0, etc.) Figure 5 shows how the first floppy drive (Floppy0) is assigned to drive A: in the system, and then how the first IDE drive (Ide0) is assigned to drive C: in the system.

To switch two floppy disks around or two hard disks around, just map Floppy0 to B: and Floppy1 to A:, and for hard disks map Ide0 to D: and Ide1 to C:.

Caution: Take care to not skip drive A: when making floppy disk assignments, as well as drive C: when making hard disk assignments. The first floppy should be A:, and the first hard drive should be C:. Also, do not assign the same file system to more than one drive letter. Thus, Floppy0 should not be used for both A: and B:. The BIOS permits this to allow embedded devices to alias drives, but desktop operating systems may not be able to maintain cache coherency with such a mapping in place.

A special field in this section entitled “Boot Method: (Windows CE/Boot Sector)” is used to configure the CE Ready feature of the BIOS. For normal booting (DOS, Windows NT, etc.), select “Boot Sector” or “Unused”.

5.3.2.1 Configuring Floppy Drive Types

If true floppy drive file systems (and not their emulators, such as ROM, RAM, or flash disks) are mapped to drive letters, then the floppy drives themselves must be configured in this section. Floppy0 refers to the first floppy disk drive on the drive ribbon cable (normally drive A:), and Floppy1 refers to the second drive (drive B:).

5.3.3 Configuring IDE Drive Types

If true IDE disk file systems (and not their emulators, such as ROM, RAM, or flash disks) are mapped to drive letters, then the IDE drives themselves must be configured in this section. The following table shows the drive assignments for Ide0-Ide3:

Table 17. IDE0-IDE3 Drive Assignments

File System Name	Controller	Master/Slave
Ide0	Primary (1f0h)	Master
Ide1	Primary (1f0h)	Slave
Ide2	Secondary (170h)	Master
Ide3	Secondary (170h)	Slave

To use the primary master IDE drive in your system (the typical case), just configure Ide0 in this section, and map Ide0 to drive C: in the Configuring Drive Assignments section.

The IDE Drive Types section lets you select the type for each of the four IDE drives: None, User, Physical, LBA, or CHS.

User This type allows the user to select the maximum cylinders, heads, and sectors per track associated with the IDE drive. This method is now rarely used since LBA is now in common use.

Physical This type instructs the BIOS to query the drive's geometry from the controller on each POST. No translation on the drive's geometry is performed, so this type is limited to drives of 512 Mbytes or less. Commonly, this is used with embedded ATA PC Cards.

LBA This type instructs the BIOS to query the drive's geometry from the controller on each POST, but then translate the geometry according to the industry-standard LBA convention. This supports up to 16-Gbyte drives. *Use this method for all new drives.*

CHS This type instructs the BIOS to query the drive's geometry from the controller on each POST, but then translate the geometry according to the Phoenix CHS convention. Using this type on a drive previously formatted with LBA or Physical geometry might show data as being missing or corrupted.

5.4 Configuring Boot Actions

Embedded BIOS supports up to six different user-defined steps in the boot sequence. When the entire system has been initialized, POST executes these steps in order until an operating system successfully loads. In addition, other pre-boot features can be run before, after, or between operating system load attempts. The following actions can be used:

Drive A: - K: Boot operating system from specified drive. If “Loader” is set to “BootRecord” or “Unused”, then the standard boot record will be invoked, causing DOS, Windows95/98, Windows NT, or other industry-standard operating systems to load. If “Boot Method” is set to “Windows CE”, then the boot drive’s boot record will not be used, and instead the BIOS will attempt to load and execute the Windows CE Kernel file, NK.BIN, from the root directory of each boot device.

Debugger Launch the Integrated BIOS Debugger. To return to the boot process from the debugger environment, type “G” at the debugger prompt and press ENTER.

MFGMODE Initiate Manufacturing Mode, allowing the system to be configured remotely via an RS232 connect to a host computer.

WindowsCE Execute a ROM-resident copy of Windows CE, if available. This feature is not applicable unless properly configured by the OEM in the BIOS adaptation.

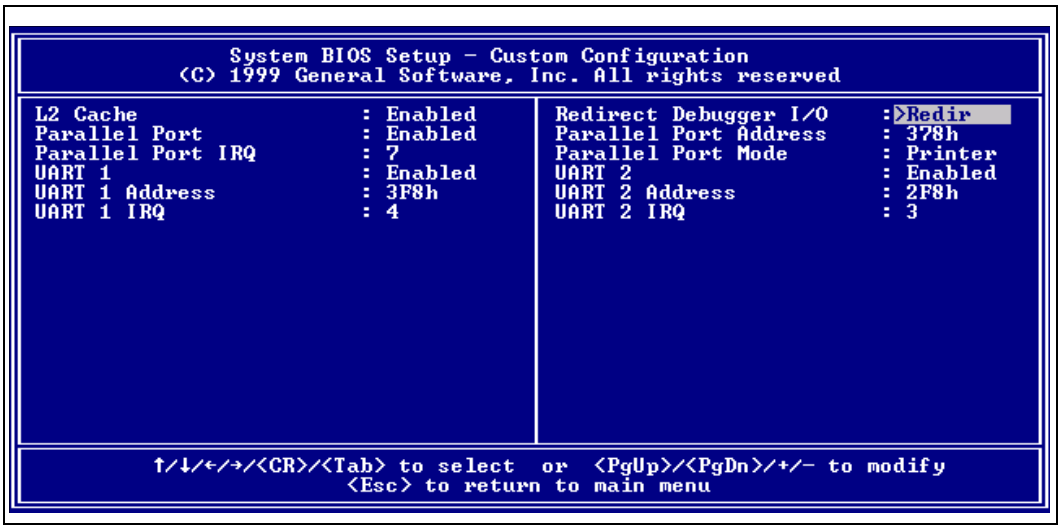
DOS in ROM Execute a ROM-resident copy of DOS, if available. This feature is not applicable unless an XIP copy of DOS, such as Embedded DOS-ROM, has been stored in the BIOS boot ROM. Copies of Embedded DOS-ROM may be obtained from General Software.

None No action; POST proceeds to the next activity in the sequence.

5.5 Custom Configuration Setup Screen

The system’s hardware-specific features are configured with the Custom Setup Screen (Figure 6). All features are straightforward except for the Redirect Debugger I/O option, which is an extra embedded feature that allows the user to select whether the Integrated BIOS Debugger should use standard keyboard and video or RS232 console redirection for interaction with the user. If no video is available, the debugger is always redirected.

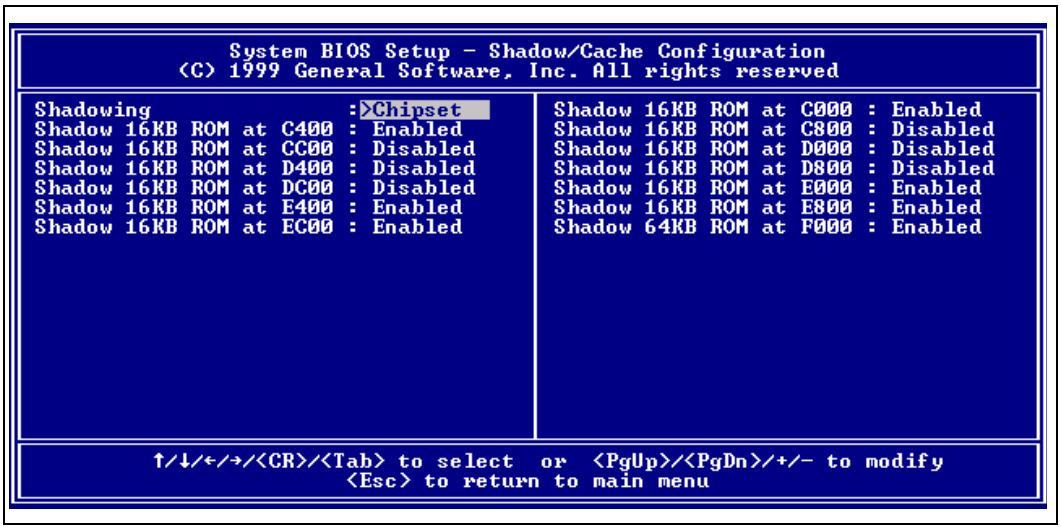
Figure 6. Embedded BIOS Custom Setup Screen



5.6 Shadow Configuration Setup Screen

The system's Shadow Configuration Setup Screen (Figure 7) allows the selective enabling and disabling of shadowing in 16 Kbyte sections, except for the top 64 Kbytes of the BIOS ROM, which is shadowed as a unit. Normally, shadowing should be enabled at C000/C400 (to enhance VGA ROM BIOS performance), and then E000-F000 should be shadowed to maximize system ROM BIOS performance.

Figure 7. Embedded BIOS Shadow Setup Screen



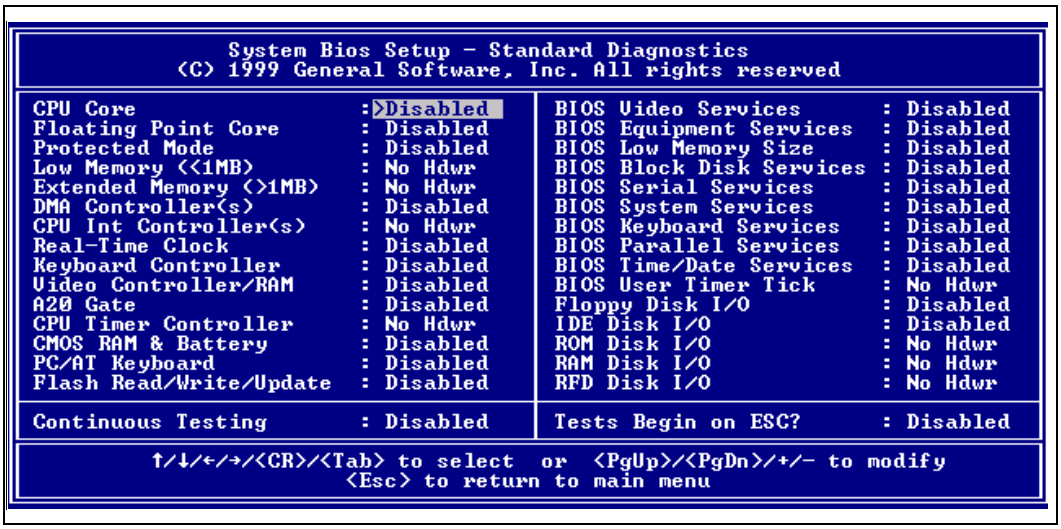
5.7 Standard Diagnostics Routines Setup Screen

Embedded systems may require automated burn-in testing in the development cycle. This facility is provided directly in the system's system BIOS through the Standard Diagnostics Routines Setup Screen (Figure 8). To use the system, selectively enable or disable features to be tested, and then enable the "Tests Begin on ESC?" option to cause the system test suite to be invoked. To repeat the system test battery continuously, you should also enable the "Continuous Testing" option. When continuous testing is started, the system will continue until an error is encountered.

Caution: The disk I/O diagnostics perform write operations on those drives; therefore, only spare drives should be used which do not contain data that could be harmed by the test.

Caution: The keyboard test may fail when in fact the hardware is operating within reasonable limits. This is because although the device may produce occasional errors, the BIOS retries operations when failures occur during normal operation of the system.

Figure 8. Standard Diagnostic Routines Setup Screen



5.8 Start System BIOS Debugger Setup Screen

The Embedded BIOS Integrated Debugger may be invoked from the Setup Screen main menu, as well as a boot activity. Once invoked, the debugger will display the debugger prompt:

EB42DBG:

and await debugger commands. To resume back to the Setup Screen main menu, type the following command, which instructs the debugger to "go":

EB42DBG: **G** <ENTER>

5.9 Start RS232 Manufacturing Link Setup Screen

The Embedded BIOS Manufacturing Mode may be invoked from the Setup Screen main menu, as well as a boot activity. Once invoked, Manufacturing Mode takes over the system and freezes the console of the system (Figure 9). The host can resume operation of the system and give control back to the system Setup Screen system with special control software.

Figure 9. Start RS232 Manufacturing Link Setup Screen

5.10 Manufacturing Mode

The system's BIOS provides a special mode, called Manufacturing Mode, that allows the target to be controlled by a host computer such as a laptop or desktop PC. Running special software supplied by General Software, the host can access the target's drives and manage the file systems on the target, reprogram flash memories, and test target hardware.

A full discussion of the uses of Manufacturing Mode is beyond the scope of this chapter. Complete documentation and host-side software is available directly from General Software. For more information, visit the General Software web site at http://www.gensw.com.

5.10.1 Console Redirection

The system can operate either with a standard PC/AT or PS/2 keyboard and VGA video monitor, or with a special emulation of a console over an RS232 cable connected to a host computer running a terminal program. To see an example session with HYPERTERMINAL, see the debugger section's screen display (Figure 11).

To use the Console Redirection feature, simply remove the video display card from the system so that no video ROM is available for the BIOS to detect. In the absence of any video support, the BIOS automatically switches its keyboard and screen functions to serial I/O over COM1 on the board. The hardware connection to the host computer requires a null modem cable.

The software on the target can be any terminal emulation program that supports ANSI terminal mode, using 9600 baud, no parity, and one stop bit (Note: This can be modified by the OEM during BIOS adaptation.) The program must be set to not use flow control, or the console may seem to stall or not accept input.

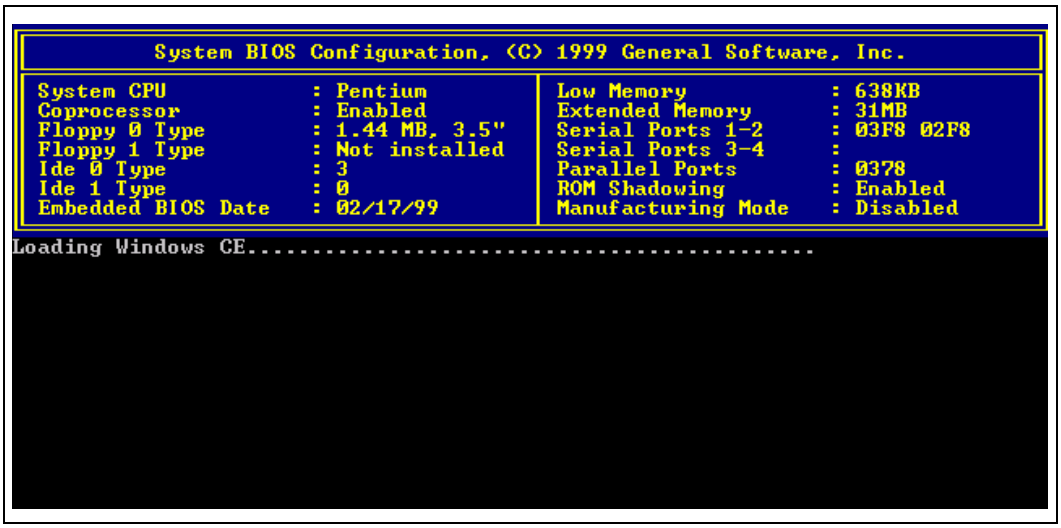
Caution: HYPERTERMINAL's default setting is to use flow control, which will render the console inoperative. To change this, create a new session, change the flow control setting to "none", save the session, and exit HYPERTERMINAL. Then reinvoke HYPERTERMINAL with the session and it will operate with the new flow control setting.

5.10.2 CE-Ready Windows CE Loader

Your system's BIOS is "CE-Ready" and can directly boot Windows CE* without loading an intermediate operating system such as DOS and LOADCEPC. Instead, the NK.BIN file can be placed on a disk drive or drive emulator, and then the BIOS can be configured through the Basic CMOS Configuration Setup Screen to boot the NK.BIN file from the boot drives instead of the boot records on those drives.

To configure your system to boot Windows CE natively from a disk drive, set the "Boot Method" field to "Windows CE" in the Basic CMOS Configuration Setup Screen. Then, place a copy of NK.BIN suitable for execution by LOADCEPC in the root directory of your normal boot drive, such as drive C:. Then, reboot the system. The configuration box should be displayed (Figure 10), and immediately following should be the message "Loading Windows CE…" followed by a series of dots, indicating that the loading process is continuing. Once fully loaded, Windows CE takes over the system and runs using the standard PC keyboard, screen, and PS/2 mouse.

Figure 10. CE-Ready Boot Feature

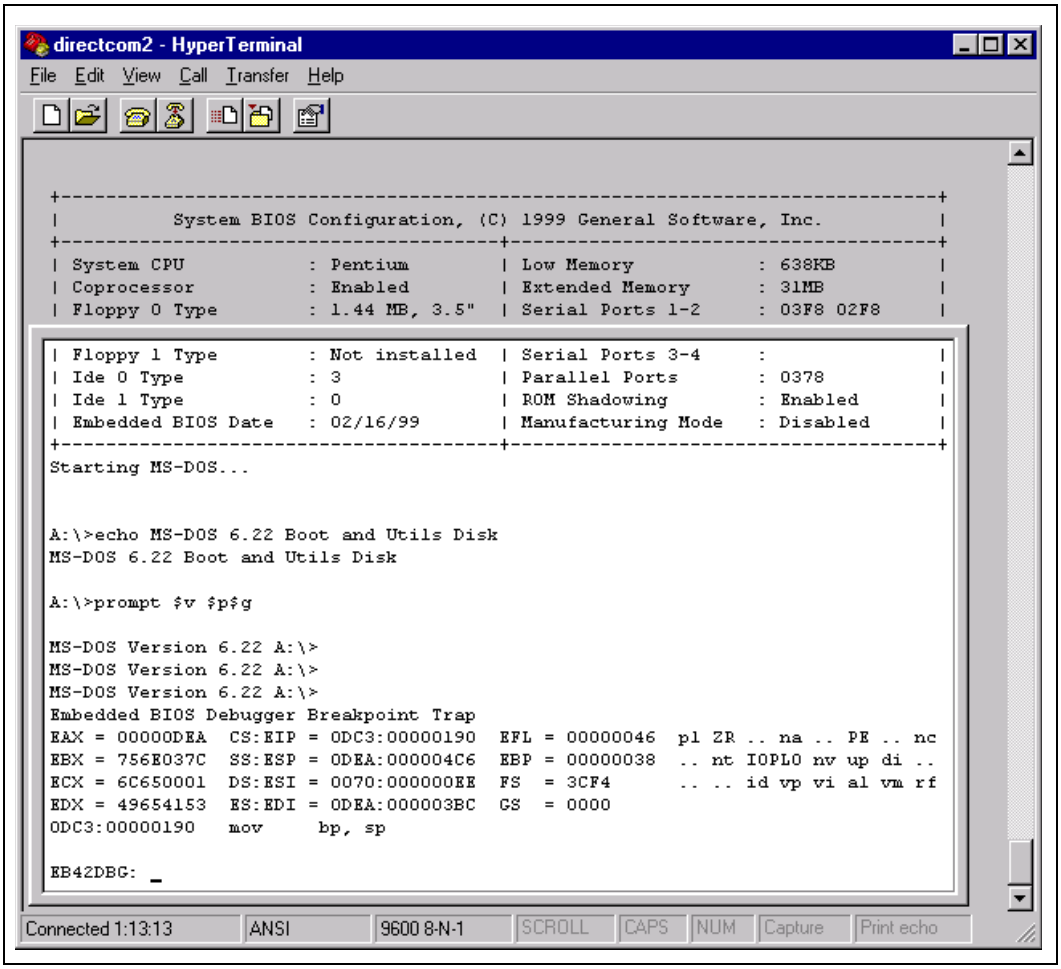


5.10.3 Integrated BIOS Debugger

The system's BIOS contains a built-in debugger that can be a valuable tool to aid the board bring-up process on new designs similar to the evaluation board. It supports a DOS SYMDEB-style command line interface, and can be used on the main console's keyboard and screen, or over a redirected connection to a terminal program (see "Console Redirection" on page 49).

To activate the debugger at any time from the main console, press the left shift and the control keys together. A display similar to the one in the HYPERTERMINAL session below (Figure 11) will appear, containing the title, “Embedded BIOS Debugger Breakpoint Trap” and a snapshot of the processor general registers.

Figure 11. Integrated BIOS Debugger Running Over a Remote Terminal



To leave the debugger and resume the interrupted activity (whether POST, BIOS, DOS, Windows, or an application program), enter the “G” command (short for “go”) and press ENTER. If you were at a DOS prompt when you entered the debugger, then DOS will still be waiting for its command, and will not prompt again until you press ENTER again.

The debugger can also be entered from the Setup Screen System, and as a boot activity (see “Basic CMOS Configuration Screen” on page 43), as a last ditch effort during board bring-up and development if no bootable device is available.

If your version of DOS, an application, or any OEM-supplied BIOS extensions have debugging code (i.e., “INT 3” instructions) remaining, then these will invoke the debugger automatically, although this is not an error. To continue, use the “G” command. When Embedded BIOS is adapted by the OEM, the debugger can be removed from the final production BIOS, and superfluous debugging code in the application will not cause the debugger to be invoked.

A complete discussion of the debugger is beyond the scope of this chapter; however, complete documentation is available from General Software via the web at http://www.gensw.com.

5.11 Embedded BIOS POST Codes

Embedded BIOS writes progress codes, also known as POST codes, to I/O port 80H during POST, in order to provide information to OEM developers about system faults. These POST codes may be monitored on the on-board Post Code Debugger located at U12 and U13. They are not displayed on the screen. For more information about POST codes, contact General Software.

Mnemonic Code	Code	System Progress Report
POST_STATUS_START	00h	Start POST (BIOS is executing).
POST_STATUS_CPUTEST	01h	Start CPU register test.
POST_STATUS_DELAY	02h	Start power-on delay.
POST_STATUS_DELAYDONE	03h	Power-on delay finished.
POST_STATUS_KBDBATRDY	04h	Keyboard BAT finished.
POST_STATUS_DISABSHADOW	05h	Disable shadowing & cache.
POST_STATUS_CALCCKSUM	06h	Compute ROM CRC, wait for KBC.
POST_STATUS_CKSUMGOOD	07h	CRC okay, KBC ready.
POST_STATUS_BATVRFY	08h	Verifying BAT command to KB.
POST_STATUS_KBDCMD	09h	Start KBC command.
POST_STATUS_KBDDATA	0ah	Start KBC data.
POST_STATUS_BLKUNBLK	0bh	Start pin 23,24 blocking & unblocking.
POST_STATUS_KBDNOP	0ch	Start KBC NOP command.
POST_STATUS_SHUTTEST	0dh	Test CMOS RAM shutdown register.
POST_STATUS_CMOSDIAG	0eh	Check CMOS checksum.
POST_STATUS_CMOSINIT	0fh	Initialize CMOS contents.
POST_STATUS_CMOSSTATUS	10h	Initialize CMOS status for date/time.
POST_STATUS_DISABDMAINT	11h	Disable DMA, PICs.
POST_STATUS_DISABPORTB	12h	Disable Port B, video display.
POST_STATUS_BOARD	13h	Initialize board, start memory bank detection.
POST_STATUS_TESTTIMER	14h	Start timer tests.
POST_STATUS_TESTTIMER2	15h	Test 8254 T2, for speaker, port B.
POST_STATUS_TESTTIMER1	16h	Test 8254 T1, for refresh.
POST_STATUS_TESTTIMER0	17h	Test 8254 T0, for 18.2Hz.
POST_STATUS_MEMREFRESH	18h	Start memory refresh.
POST_STATUS_TESTREFRESH	19h	Test memory refresh.
POST_STATUS_TEST15US	1ah	Test 15usec refresh ON/OFF time.
POST_STATUS_TEST64KB	1bh	Test base 64KB memory.
POST_STATUS_TESTDATA	1ch	Test data lines.
POST_STATUS_TESTADDR	20h	Test address lines.
POST_STATUS_TESTPARITY	21h	Test parity (toggling).
POST_STATUS_TESTMEMRDWR	22h	Test Base 64KB memory.
POST_STATUS_SYSINIT	23h	Prepare system for IVT initialization.
POST_STATUS_INITVECTORS	24h	Initialize vector table.
POST_STATUS_8042TURBO	25h	Read 8042 for turbo switch setting.
POST_STATUS_POSTTURBO	26h	Initialize turbo data.
POST_STATUS_POSTVECTORS	27h	Modification of IVT.
POST_STATUS_MONOMODE	28h	Video in monochrome mode verified.
POST_STATUS_COLORMODE	29h	Video in color mode verified.
POST_STATUS_TOGGLEPARITY	2ah	Toggle parity before video ROM test.
POST_STATUS_INITBEFOREVIDEO	2bh	Initialize before video ROM check.
POST_STATUS_VIDEOROM	2ch	Passing control to video ROM.

POST_STATUS_POSTVIDEO	2dh	Control returned from video ROM.
POST_STATUS_CHECKEGAVGA	2eh	Check for EGA/VGA adapter.
POST_STATUS_TESTVIDEOMEMORY	2fh	No EGA/VGA found, test video memory.
POST_STATUS_RETRACE	30h	Scan for video retrace signal.
POST_STATUS_ALTDISPLAY	31h	Primary retrace failed.
POST_STATUS_ALTRETRACE	32h	Alternate found.
POST_STATUS_VRFYSWADAPTER	33h	Verify video switches.
POST_STATUS_SETDISPMODE	34h	Establish display mode.
POST_STATUS_CHECKSEG40A	35h	Initialize ROM BIOS data area.
POST_STATUS_SETCURSOR	36h	Set cursor for power-on msg.
POST_STATUS_PWRONDISPLAY	37h	Display power-on message.
POST_STATUS_SAVECURSOR	38h	Save cursor position.
POST_STATUS_BIOSIDENT	39h	Display BIOS identification string.
POST_STATUS_HITDEL	3ah	Display "Hit <DEL> to ..." message.
POST_STATUS_VIRTUAL	40h	Prepare protected mode test.
POST_STATUS_DESCR	41h	Prepare descriptor tables.
POST_STATUS_ENTERVM	42h	Enter virtual mode for memory test.
POST_STATUS_ENABINT	43h	Enable interrupts for diagnostics mode.
POST_STATUS_CHECKWRAP1	44h	Initialize data for memory wrap test.
POST_STATUS_CHECKWRAP2	45h	Test for wrap, find total memory size.
POST_STATUS_HIGHPATTERNS	46h	Write extended memory test patterns.
POST_STATUS_LOWPATTERNS	47h	Write conventional memory test patterns.
POST_STATUS_FINDLOWMEM	48h	Find low memory size from patterns.
POST_STATUS_FINDHIMEM	49h	Find high memory size from patterns.
POST_STATUS_CHECKSEG40B	4ah	Verify ROM BIOS data area again.
POST_STATUS_CHECKDEL	4bh	Check for <DEL> pressed.
POST_STATUS_CLREXTMEM	4ch	Clear extended memory for soft reset.
POST_STATUS_SAVEMEMSIZE	4dh	Save memory size.
POST_STATUS_COLD64TEST	4eh	Cold boot: Display 1st 64KB memtest.
POST_STATUS_COLDLOWTEST	4fh	Cold boot: Test all of low memory.
POST_STATUS_ADJUSTLOW	50h	Adjust memory size for EBDA usage.
POST_STATUS_COLDHITEST	51h	Cold boot: Test high memory.
POST_STATUS_REALMODETEST	52h	Prepare for shutdown to real mode.
POST_STATUS_ENTERREAL	53h	Return to real mode.
POST_STATUS_SHUTDOWN	54h	Shutdown successful.
POST_STATUS_DISABA20	55h	Disable A20 line.
POST_STATUS_CHECKSEG40C	56h	Check ROM BIOS data area again.
POST_STATUS_CHECKSEG40D	57h	Check ROM BIOS data area again.
POST_STATUS_CLRHITDEL	58h	Clear "Hit <DEL>" message.
POST_STATUS_TESTDMAPAGE	59h	Test DMA page register file.
POST_STATUS_VRFYDISPMEM	60h	Verify from display memory.
POST_STATUS_TESTDMA0BASE	61h	Test DMA0 base register.
POST_STATUS_TESTDMA1BASE	62h	Test DMA1 base register.
POST_STATUS_CHECKSEG40E	63h	Checking ROM BIOS data area again.
POST_STATUS_CHECKSEG40F	64h	Checking ROM BIOS data area again.
POST_STATUS_PROGDMA	65h	Program DMA controllers.
POST_STATUS_INITINTCTRL	66h	Initialize PICs.
POST_STATUS_STARTKBDTEST	67h	Start keyboard test.
POST_STATUS_KBDRESET	80h	Issue KB reset command.
POST_STATUS_CHECKSTUCKKEYS	81h	Check for stuck keys.
POST_STATUS_INITCIRCBUFFER	82h	Initialize circular buffer.
POST_STATUS_CHECKLOCKEDKEYS	83h	Check for locked keys.
POST_STATUS_MEMSIZEMISMATCH	84h	Check for memory size mismatch.
POST_STATUS_PASSWORD	85h	Check for password or bypass setup.
POST_STATUS_BEFORESETUP	86h	Password accepted.

```
POST_STATUS_CALLSETUP        87h   Entering setup system.
POST_STATUS_POSTSETUP        88h   Setup system exited.
POST_STATUS_DISPPWRON        89h   Display power-on screen message.
POST_STATUS_DISPWAIT         8ah   Display "Wait..." message.
POST_STATUS_ENABSHADOW       8bh   Shadow system & video BIOS.
POST_STATUS_STDCMOSSETUP     8ch   Load standard setup values from CMOS.
POST_STATUS_MOUSE            8dh   Test and initialize mouse.
POST_STATUS_FLOPPY           8eh   Test floppy disks.
POST_STATUS_CONFIGFLOPPY     8fh   Configure floppy drives.
POST_STATUS_IDE              90h   Test hard disks.
POST_STATUS_CONFIGIDE        91h   Configure IDE drives.
POST_STATUS_CHECKSEG40G      92h   Checking ROM BIOS data area.
POST_STATUS_CHECKSEG40H      93h   Checking ROM BIOS data area.
POST_STATUS_SETMEMSIZE       94h   Set base & extended memory sizes.
POST_STATUS_SIZEADJUST       95h   Adjust low memory size for EBDA.
POST_STATUS_INITC8000        96h   Initialize before calling C800h ROM.
POST_STATUS_CALLC8000        97h   Call ROM BIOS extension at C800h.
POST_STATUS_POSTC8000        98h   ROM C800h extension returned.
POST_STATUS_TIMERPRNBASE     99h   Configure timer/printer data.
POST_STATUS_SERIALBASE       9ah   Configure serial port base addresses.
POST_STATUS_INITBEFORENPX    9bh   Prepare to initialize coprocessor.
POST_STATUS_INITNPX          9ch   Initialize numeric coprocessor.
POST_STATUS_POSTNPX          9dh   Numeric coprocessor initialized.
POST_STATUS_CHECKLOCKS       9eh   Check KB settings.
POST_STATUS_ISSUEKBDID       9fh   Issue keyboard ID command.
POST_STATUS_RESETID          0a0h  KB ID flag reset.
POST_STATUS_TESTCACHE        0a1h  Test cache memory.
POST_STATUS_DISPSOFTERR      0a2h  Display soft errors.
POST_STATUS_TYPEMATIC        0a3h  Set keyboard typematic rate.
POST_STATUS_MEMWAIT          0a4h  Program memory wait states.
POST_STATUS_CLRSCR           0a5h  Clear screen.
POST_STATUS_ENABPTYNMI       0a6h  Enable parity and NMIs.
POST_STATUS_INITE000         0a7h  Initialize before calling ROM at E000h.
POST_STATUS_CALLE000         0a8h  Call ROM BIOS extension at E000h.
POST_STATUS_POSTE000         0a9h  ROM extension returned.
POST_STATUS_DISPCONFIG       0b0h  Display system configuration box.
POST_STATUS_INT19BOOT        00h   Call INT 19h bootstrap loader.
POST_STATUS_LOWMEMEXH        0b1h  Test low memory exhaustively.
POST_STATUS_EXTMEMEXH        0b2h  Test extended memory exhaustively.
POST_STATUS_PCIENUM          0b3h  Enumerate PCI busses.
```

5.12 Embedded BIOS Beep Codes

Embedded BIOS tests much of the system hardware early in POST before messages can be displayed on the screen. When system failures are encountered at these early stages, POST uses beep codes (a sequence of tones on the speaker) to identify the source of the error.

The following is a comprehensive list of POST beep codes for the system BIOS. BIOS extensions, such as VGA ROMs and SCSI adapter ROMs, may use their own beep codes, including short/long sequences, or possibly beep codes that sound like the ones below. When diagnosing a system failure, remove these adapters if possible before making a final determination of the actual POST test that failed.

Mnemonic Code	Beep Count	Description of Problem
POST_BEEP_REFRESH	1	Memory refresh is not working.
POST_BEEP_PARITY	2	Parity error found in 1st 64KB of memory.
POST_BEEP_BASE64KB	3	Memory test of 1st 64KB failed.
POST_BEEP_TIMER	4	T1 timer test failed.
POST_BEEP_CPU	5	CPU test failed.
POST_BEEP_GATEA20	6	Gate A20 test failed.
POST_BEEP_DMA	7	DMA page/base register test failed.
POST_BEEP_VIDEO	8	Video controller test failed.
POST_BEEP_KEYBOARD	9	Keyboard test failed.
POST_BEEP_SHUTDOWN	10	CMOS shutdown register test failed.
POST_BEEP_CACHE	11	External cache test failed.
POST_BEEP_BOARD	12	General board initialization failed.
POST_BEEP_LOWMEM	13	Exhaustive low memory test failed.
POST_BEEP_EXTMEM	14	Exhaustive extended memory test failed.
POST_BEEP_CMOS	15	CMOS restart byte test failed.
POST_BEEP_ADDRESS_LINE	16	Address line test failed.
POST_BEEP_DATA_LINE	17	Data line test failed.
POST_BEEP_INTERRUPT	18	Interrupt controller test failed.
POST_BEEP_PASSWORD	1	Incorrect password used to access SETUP.

PLD Code Listing A

The code listing below is for the 22V10 PLD.

```
TITLE       22V10 PORT 80 ADDRESS DECODER / FLASH DECODE
PATTERN     1
REVISION    B
AUTHOR      CHRIS BANYAI
COMPANY     INTEL CORPORATION
DATE        10/1/97

OPTIONS
    SECURITY = OFF


;  ( part was 22V10FN before conversion )
CHIP  P80B iPLD22V10N

PIN         19    IOWR_BAR
PIN          3    AEN
PIN      [6:7]    SA[0:1]
PIN     [9:13]    SA[2:6]
PIN         16    SA7
PIN      [5:4]    SA[8:9]
PIN    [26:23]    SA[19:16]
PIN    [21:20]    SA[15:14]
PIN          2    SEL

PIN         18   /CS_BAR
PIN         17   /CS_DOC
PIN         27    OX

EQUATIONS
CS_BAR = /IOWR_BAR * /AEN * /SA0 * /SA1 * /SA2 * /SA3 * /SA4 * /SA5 * /SA6
              * SA7 * /SA8 * /SA9
CS_BAR.TRST = VCC

CS_DOC = /SEL * /AEN * SA19 * SA18 * /SA17 * /SA16 * SA15 * /SA14
       + SEL * /AEN * SA19 * SA18 * /SA17 * SA16 * /SA15 * /SA14
CS_DOC.TRST = VCC

OX = /IOWR_BAR
OX.TRST = VCC

SIMULATION

    SETF /AEN /SA0 /SA1 /SA2 /SA3 /SA4 /SA5 /SA6 /SA7 /SA8 /SA9 IOWR_BAR
    SETF SA7 IOWR_BAR
    SETF /IOWR_BAR
    SETF IOWR_BAR
```

```
SETF AEN /IOWR_BAR
SETF /AEN
SETF IOWR_BAR
SETF SA0 /IOWR_BAR
SETF /SA0 /IOWR_BAR
SETF IOWR_BAR
SETF /SA0 /SA1 /SA2 /SA3 /SA4 /SA5 /SA6 /SA7 /SA8 /SA9
SETF /SA19 /SA18 /SA17 /SA16 /SA15 /SA14
SETF /SEL
SETF SA19 SA18 /SA17 /SA16 SA15 /SA14
SETF /SEL
SETF /AEN
SETF /SA19
SETF SA19
SETF /SA18
SETF SA18
SETF SA17
SETF /SA17
SETF SA16
SETF /SA16
SETF /SA15
SETF SA15
SETF SA14
SETF /SA14
SETF /SEL
SETF SA19 SA18 /SA17 SA16 /SA15 /SA14
SETF /SEL
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SETF SA15
SETF /SA15
SETF SA14
SETF /SA14
SETF /SEL
```

Bill of Materials B

Table 18 is the bill of materials for the baseboard. Table 19 is the bill of materials for the processor assembly.

Table 18. Baseboard Bill of Materials (Sheet 1 of 5)

Rev. 1.7

Reference Designator	Description	Manufacturer	Manufacturer P/N	Comments/ Changes from Rev D	Alternate Manufacturing Info	All Changes
J14,J15	Conn,Jumper2,1X2 25-mil sq/100-mil space,HDR2	3M	929647-09-02			
J20-24	Conn,Jumper3,1X3 25-mil sq/100-mil space,HDR3	3M	929647-09-03			
J12	Conn,Fan	AMP	173981-3			
XU9	PLCC, Socket 28	AMP	822271-1			
J19	Conn,CPU,400 Pin Array (BGA),BGA40X10-400R	Berg	74219-002			
U6	IC,Clock Generator,CK100,SSOP300 -48(PIN)	Cypress	CY2280PVC-11S			
U16	IC,Clock Buffer,18 Output low skew,SSOP300-48(PIN)	Cypress	CY2318ANZPVC-1			
Y2	Crystal,32.768KHz,XTAL/ MC-405	Epson	MC-405			
J4	Conn, Serial Stack,DB9MX2	FOXCONN	DM10156-73			
J3	Conn, DB25,DB25FM1	FOXCONN	DT11323-R5T			
J7,J8,J9	Conn,PCI Edge Recept,145154-120	FOXCONN	EH06001-PC-W			
J5,J6	Conn,ISA Edge Recept.,isa-98	FOXCONN	EQ04901-S6			
JP1	Conn,Floppy,17X2 Header	FOXCONN	HL07173-P4			
JP3,JP4	Conn, IDE,20X2 Header	FOXCONN	HL07206-D2			
J11	Conn,Power,5566DP-20/ ATX	FOXCONN	HM20100-P2			
J1	Conn,PS2 Keyboard / Mouse Connector	FOXCONN	MH11067-D2			
J13	Conn,AGP Edge Recept., 120 pins,AGP-124	FOXCONN	PC1243K-10			
J2	2 USB Stack Connectors	FOXCONN	UB1112C-D3			
U11	BIOS FLASH Memory,TSOP12X20/40S	INTEL	E28F004B5T60			Part # changed in previous rev
U8	VLSI,PIIX4,PCI to IDE &ISA Bridge,324 mBGA,BGA20x20-324	Intel	FW82371EB			

Table 18. Baseboard Bill of Materials (Sheet 2 of 5)

Rev. 1.7

Reference Designator	Description	Manufacturer	Manufacturer P/N	Comments/ Changes from Rev D	Alternate Manufacturing Info	All Changes
C99,C100,C132,C133,C209,C214	Chip Capacitor,10pF, 50V,CC0603	Kemet	C0603C100J5GAC			
C: 22,42-43,48-49,54,59-65,70-71,73,75-76,85-87,90-92,96-97,102,106-108,111-112,114,116-118, 126-127,129-131,142,147,157,159-162,174-176,181-183, 187-200,205-206,208,226-228	Chip Capacitor,0.1uF, 16V,CC0603	Kemet	C0603C104K4RAC	DO NOT POPULATE C143, C146,C203, C210, C215		
C27-C41,C44-C47,C50-C53	Chip Capacitor,470pF, 50V,CC0603	Kemet	C0603C471K5RAC			
C3-5,C8,C55-57,C94,C119-121, C134,C138, C145, C153	Cap,Tant,10uF,15V,C Case,6032	Kemet	T491C106K016AS			
C93,C103-105, C128,C152, C154-156	Cap,Tant,47uF, 20V,D Case,7343	Kemet	T491D476M020AS			
C2,C6,C58,C72, C84,C88,C89,C95, C109	Cap,Tant,100uF, 10V,D Case,7343	Kemet	T495D107M010AS			
C1,C7,C23,C66-C68,C74,C77-C82, C101,C113,C115, C141,C158, C163-173,C177-180, C184-186,C201-202,C204,C207, C211-213,C216-217,C220-C225	Chip Capacitor,0.01uF 50V,CC0603	Kemet	C0603C103J5RAC			

Table 18. Baseboard Bill of Materials (Sheet 3 of 5)

Rev. 1.7

Reference Designator	Description	Manufacturer	Manufacturer P/N	Comments/ Changes from Rev D	Alternate Manufacturing Info	All Changes
U9	IC,PLD,PLCC28,Socket28	LATTICE	GAL22V10B-7LJ			
U23	IC,Linear Voltage Regulator,SOT-223	Linear Tech.	LT1117-3.3cst			
U5	IC,Linear Voltage Regulator,SOT-223	Linear Tech.	LT1117CST			
XU11	40TSOP BIOS Socket,TSOP12X20/40S	Meritec	980020-40-01			
XU12,XU13	TIL311 SOCKET,DIP14	MILLMAX	110-99-314-41-001			
U25	IC,Logic,74ACT05,SO14	Motorola	MC74ACT05DR			
FB1-FB-4, FB9	Ferrite Bead, SM1806, Z-Bead	Murata	BLM41P750S			Changed part # on Rev. 1.7
FB5,FB6,FB7,FB8	Ferrite Bead, SM1806, Z-Bead	Murata	BLM41A800S			
U22	IC,Logic,74ALS00,SOIC14	National	DM74ALS00M			
U7	IC,Tranciever,8-Bit Bidirectional Buffer,SOIC20,SO20W	National	DM74ALS245AWM			
C69,C83,C98,C110	Cap,Electrolitic,220uF, 25v,6.3mmx11.2mm,PCAPR 200-300	Panasonic	ECE-A1EU221			
R48,R52,R98-R100, R106,R108-R116,R118-R122	Chip Resistor,0 Ohm Shunt,5%,CR0805	Panasonic	ERJ6GEY0R00V			
R25,R42,R45,R49,R63,R101,R102	Chip Resistor,1K,5%,CR0805	Panasonic	ERJ6GEYJ102V			
R2,R4,R5,R11,R40,R41,R43,R53-R56,R105,R117,R123-124,R127	Chip Resistor,10K,5%,CR0805	Panasonic	ERJ6GEYJ103V			
R1,R3,R88,R89.R90,R91	Chip Resistor,15K,5%,CR0805	Panasonic	ERJ6GEYJ153V			
R9	Chip Resistor,22,5%,CR0805	Panasonic	ERJ6GEYJ220V			
R10,R12,R13,R14,R39,R58,R70	Chip Resistor,220,5%,CR0805	Panasonic	ERJ6GEYJ221V			
R92-R95	Chip Resistor,27,5%,CR0805	Panasonic	ERJ6GEYJ270V			
R20,R44,R57,R71	Chip Resistor,2.7K,5%,CR0805	Panasonic	ERJ6GEYJ272V			

Table 18. Baseboard Bill of Materials (Sheet 4 of 5)

Rev. 1.7

Reference Designator	Description	Manufacturer	Manufacturer P/N	Comments/ Changes from Rev D	Alternate Manufacturing Info	All Changes
R17-R19,R21,R23,R26,R28-R32,R34,R36,R38	Chip Resistor,33,5%,CR0805	Panasonic	ERJ6GEYJ330V			
R22, R24, R27	Chip Resistor,47,5%,CR0805	Panasonic	ERJ6GEYJ470V			changed value (11/10/99)
R103,R104	Chip Resistor,470,5%,CR0805	Panasonic	ERJ6GEYJ471V			
R7,R64-R69, R125,R126, R128	Chip Resistor,4.7k,5%,CR0805	Panasonic	ERJ6GEYJ472V			
R72-R87,R96,R107	Chip Resistor,8.2K,5%,CR0805	Panasonic	ERJ6GEYJ822V			
S1,S2	Switch-Push Button,PBSW/ PNASNC2	Panasonic	EVQ-PHP03T			
RP2,RP3,RP41-RP47,RP54-RP56, RP58,RP60, RP61	Res,Array,SMT,33,5%,EXB-V	Panasonic	EXB33V330JV			
RP10,RP18, RP23	Res,Array,SMT,1K,5%,EXB-V	Panasonic	EXB38V102JV			
RP8-9,RP11,RP13-17,RP19-RP22, RP24,RP26-33, RP35-36, RP39, RP51-52,RP59	Res,Array,SMT,10K,5%,EXB-V	Panasonic	EXB38V103JV			
RP1,RP4	Res,Array,SMT,22,5%,EXB-V	Panasonic	EXB38V220JV			(RP48 changed value, see below)
RP25,RP37, RP49,RP50, RP53	Res,Array,SMT,2.7K,5%,EXB-V	Panasonic	EXB38V272JV			
RP57	Res,Array,SMT,47,5%,EXB-V	Panasonic	EXB38V470JV			
RP5,RP6,RP7, RP48	Res,Array,SMT,4.7K,5%,EXB-V	Panasonic	EXB38V472JV			RP48 changed value in Rev 1.6
RP12,RP34	Res,Array,SMT,5.6k,5%,EXB-V	Panasonic				
U24	IC,Logic,Inverter, Schmitt Trigger,SOIC14	Philips	74LVC14AD			

Table 18. Baseboard Bill of Materials (Sheet 5 of 5)

Rev. 1.7

Reference Designator	Description	Manufacturer	Manufacturer P/N	Comments/ Changes from Rev D	Alternate Manufacturing Info	All Changes
U10	IC,Logic,10 Bit Bus Switch,QSOP,SO24W	Quality Semi	QS3384SO			
Y1	Crystal,14.318MHz,XTAL,FOX-HC495D	Raltron	AS-14.31818-20			
F1-F3	Fuse,Drawing,SM250	RayChem	SMD250-2			
XBT1	Battery Holder Socket	Renata	HU-2032-1			
BT1	Battery	Reneta	CR2032			
D1,D2,D5	Diode,LED,SOT23-A	Siemens	LGS260-DO			
U1	VLSI,Super I/O,QFP128	SMSC	FDC37B787			
C122-C125	Chip Capacitor,47pF,CC0603	TDK	C1608C0G1H470 JT$			
C9-C21,C24-C26	Chip Capacitor,220pF,CC0603	TDK	C1608X7R1H221 KT009A			
U15	IC,Logic,3 state buffer,SOP-14	TI	74LVC125A			
U21	IC,Logic,SOP-14	TI	74LVC14A			
U3,U4	IC,RS232 Transceiver, SOIC20,SO20W	TI	GD75232DW			
U2	IC,Logic,Open Drain Buffer,SOP-14	TI	SN7407D			
U12,U13	7 Segment LED display,DIP14	TI	TIL311			
D3-D4,D6-D7	Schottky Diode,SOT23-E	ZETEX	BAT54			
R8,R15,R16, R46,R47	Chip Resistor,124,1%,CR0805	Panasonic	ERJ-6ENF1240V			
RP38,RP40	Res,Array,SMT,270,5%,EXB-V	Panasonic	EXB38V271JV			
R300-R307	Chip Resistor,0,5%,CR0805	Panasonic	ERJ6GEY0R00V			
R50	Chip Resistor,680,5%,CR0805	Panasonic	ERJ6GEYJ681V			
R308	Chip Resistor,33,5%,CR0805	Panasonic	ERJ6GEYJ330V			
R309	Chip Resistor,0 Ohm Shunt,5%,CR0805	Panasonic	ERJ6GEY0R00V			

Table 19. PGA370 Socket Processor Assembly Bill of Materials (Sheet 1 of 3)

Rev. 4.6

Reference Designator	Description	Manufacturer	Manufacturer P/N	Alternate Manufacturing Info	All Changes
R54,R66,R79	0, CR0805	PANASONIC	ERJ-6GEY0R00V	DALE - CRCW0805000ZT	
R68,R71,R72	2.2, CR1206	PANASONIC	ERJ-8RQJ2R2V		
R63,R65	10, CR0805	PANASONIC	ERJ-6GEYJ100V		
Q1,Q2,Q3,Q4	N DGS, 25V, SOT-23	FAIRCHILD	FDV301N		Changed Part # and renumbered transistors
C84,C85,C94,C95,C96, C97,C98	0.01uF, 10V, CC0603	PANASONIC	ECJ-1VB1A103K	KEMET - C0603C103K8R	
C145,C146	0.1uF, 25V, CC603	PANASONIC	ECJ-1VB1E104K	MURATA - GRM39Y5V104Z025AD	
C3,C4,C5,C6,C7,C8, C9, C66,C67,C68,C69,C70, C71,C72,C73,C74,C75, C76,C77,C78,C79,C80, C81,C82,C83,C89,C90, C91,C92,C93,C101, C102,C103,C106,C110,C113, C115,C128,C129,C131, C132,C147,C149,C151, C152,C153, C154	0.1uF, 16V, CC0603	PANASONIC	ECJ-1VB1C104K	KEMET - C0603C104K4R	
C137,C138	0.1uF, 25V, 805	MURATA	GRM40X76104K025AD	KEMET - C805C104K3RAC (USE ANY VOLTAGE ABOVE 16V)	
R61	1.00K 1%, CR0805	PANASONIC	ERJ-6ENF1001V		
R86,R87,R90,R91,R106, R107	1.5K, CR0805	PANASONIC	ERJ-6GEYJ152V		
C150	10 pf, 50V, CC0603	PANASONIC	ECU-V1H100DCM	KEMET - C0603C100K5G	
R60	100 1%, CR0805	PANASONIC	ERJ-6ENF1000V		
R70,R78,R88,R92	10K, CR0805	PANASONIC	ERJ-6GEYJ103V		
RP64	10K, EXB-V	PANASONIC	EXB-V8V103JV		
R97,R101	110 ohm 1%, CR0805	PANASONIC	ERJ-6ENF1100V		
R57,R58,R59	150 1%, CR0805	PANASONIC	ERJ-6ENF1500V		
R47,R96,R98,R108, R109, R110	150 ohm, CR0805	PANASONIC	ERJ-6GEYJ151V		

Table 19. PGA370 Socket Processor Assembly Bill of Materials (Sheet 2 of 3)

Rev. 4.6

Reference Designator	Description	Manufacturer	Manufacturer P/N	Alternate Manufacturing Info	All Changes
R15,R32,R33,R34,R35, R36,R37,R38,R39,R42, R43,R45,R67,R80,R93, R99	1K, CR0805	PANASONIC	ERJ-6GEYJ102V		
C112,C114	1uF, 10V, CC0805	PANASONIC	ECJ-2YB1A105K	KEMET - C0805C105K8R	
C100	20pF, 16V, CC0603	PANASONIC	ECU-V1C200JCV	MURATA - GRM39COG200J016	
R19,R26,R27,R103	22 ohm, CR0805	PANASONIC	ERJ-6GEYJ220V		
C107,C108,C109,C111, C118,C119,C120,C121	2200uF, 16V, PCAPR200-500	PANASONIC	EEU-FC1C222		
R6,R7,R31,R40,R46, R49, R52,R105,R112	270 ohm, CR0805	PANASONIC	ERJ-6GEYJ271V		added R6, R7
R69,R74,R76,R94	3.0 milliohms 5%, CR2512	DALE/VISHAY	WSL-2512 0.003 5%		
R44,R111	3.3K, CR0805	PANASONIC	ERJ-6GEYJ332V		
R81	330 ohm, CR0805	PANASONIC	ERJ-6GEYJ331V		
C148	33uF, 16V, 7343	KEMET	T495D336M016AS	AVX - TPSD336M020S0200	
C25,C26,C27,C28,C29, C35,C36,C37,C38,C39, C63	4.7uF, 10V, CC1206	PANASONIC	ECJ-3YB1A475Z	MURATA - GRM42-6X5R475K010AD, TDK - CC1206CY5V475Z	
L1	4.7uH, CR0805	MURATA	LQG21N4R7K00T1	TDK - MLF2012A4R7K	
L2,L3	4.7uH, IND1855	BI TECH	HM00-98637A		
U4	443BX_10	INTEL	FW82443BX		
R50,R51	47 ohm, CR0805	PANASONIC	ERJ-6GEYJ470V		Qty per board corrected
C117	4700pF, 50V, CC0603	PANASONIC	ECJ-1VB1H472K	KEMET - C0603C472K5R	
C127,C130	470uF, 16V, PCAPR200-300	PANASONIC	EEU-FC1C471L		
R100	51 ohm 5%, CR0805	PANASONIC	ERJ-6GEYJ510V		

Table 19. PGA370 Socket Processor Assembly Bill of Materials (Sheet 3 of 3)

Rev. 4.6

Reference Designator	Description	Manufacturer	Manufacturer P/N	Alternate Manufacturing Info	All Changes
RP33,RP34,RP35,RP36, RP37,RP38,RP39,RP40, RP41,RP42,RP43,RP44, RP45,RP46,RP47,RP48, RP49,RP50,RP51,RP52, RP53,RP54,RP55,RP56, RP57,RP58,RP59,RP60, RP61	56 ohm, EXB-V	PANASONIC	EXB-V8V560JV		Qty per board corrected
RP62	0 ohm, EXB-V	PANASONIC	EXB-V8VR000V		
R77	56 ohm DISCRETE, CR0805	PANASONIC	ERJ-6GEYJ560V		
R53	680 ohm, CR0805	PANASONIC	ERJ-6GEYJ681V		
R55,R56	75 1%, CR0805	PANASONIC	ERJ-6ENF0750V		
R102,R104	86.6 ohm 1%, CR0805	PANASONIC	ERJ-6ENF86R6V		
U5	950554-00x, BGA40X10-400	BERG	74220-001		
D1	BAT54, SOT23	ZETEX	BAT54CT-ND		
J1	CON3, FAN CONNECTOR, 3 PIN HEADER	3M	2302-6111		
J3	CON4, 644518-4	AMP	644518-4		
J2	ITPM	AMP	104078-4		
U6	MAX1617, QSOP16	MAXIM	MAX1617MEE		
U12,U13	MTD3055V, TO252	MOTOROLA	MTD3055V		
U1	S370-256	AMP	916783-2		
U9	SC1185A, SO24W	SEMTECH	SC1185ACSW		
U10,U11	SUD50N03-07, TO252	SILICONIX	SUD50N03-07-T4		

Table 20. Key Components Bill of Materials

Rev. 1.1		
Description	**Manufacturer**	**Part #**
Development Kit Baseboard and Processor Assembly Board	Intel	EIAP3FMBDEVKIT EIACEL18FMBDVKT EIACEL25FMBDVKT
Intel® Pentium® III Processor at 850 MHz with 256 Kbyte L2 cache	Intel	RB80526PY850256
Intel® Celeron™ Processor at 850 MHz with 128 Kbyte L2 cache[1]	Intel	RB80526RY850128
Intel® Celeron™ Processor at 433 MHz with 128 Kbyte L2 cache[2]	Intel	FV80524RX433128
Thermal Solution	Agilent Technologies	Arcti-Cooler HACA-0001
100 MHz, 32 Mbyte, SDRAM DIMM	Micron Semiconductor Products	MT4LSDT464AG-10CB2
BIOS FLASH Memory, TSOP12X20/40S	Intel	E28F004B5T60
4.3 Gbyte Hard disk drive	varies	varies
QNX Software Package (pre-installed on HDD)	QNX	MR2509
Tornado 2.0/VxWorks CD	Wind River Systems	TEV-13306-ZC-00
69000 Video Card	Densitron	PCIX690LP
Intel® Pro/100+ Fast Ethernet Controller	Intel	PILA8460B

NOTE: This BOM does not include items such as mounting hardware, packaging material, documentation, etc., because these items are development kit specific and subject to change with no prior notice to the customer.

1. Shipped exclusively with kit: EIACEL18FMBDVKT
2. Shipped exclusively with kit: EIACEL25FMBDVKT

Schematics C

Schematics are provided for the following items listed below. Schematics are available from the Intel Developer's web site in OrCAD* (version 9.0 or later) and PDF format.

Baseboard:

- Revision History
- Block Diagram
- Mini-PCI Connector (Not Populated)
- Processor Assembly Connector
- DIMM0
- DIMM1
- DIMM2 (Not Populated)
- Clocks
- ISA/PCI Pullups
- PCI Slots 0 & 1
- PCI Slot 2
- AGP Connector
- PIIX4 Part 1
- PIIX4 Part 2
- IDE Connectors
- Super I/O
- USB Connectors
- ISA Connectors
- COMx, DB25, Floppy
- BIOS/Port 80
- ATX Power Connector
- Unused Gates

Processor Assembly:

- Revision History
- Block Diagram
- PGA370 Host Interface
- PGA370 Other
- PGA370 Power
- 440BX Host Interface

- 440BX Memory Interface
- Connectors
- GTL+ Termination
- Bus Ratio, Thermal, ITP
- Voltage Regulator
- Layout Guidelines

Modular Reference Design
System Electronics Board

History

Changes made to Revision E.

1. Removed CS_B#[5:0]. Tied CS_Bn# to CS_An# at DIMM connectors.
2. Changed WE_B#, SCAS_B# and SRAS_B# to WE_A#, SCAS_A#, SRAS_A# on J17
3. Changed WE_A#, SCAS_A# and SRAS_A# to WE_B#, SCAS_B# and SRAS_B# on J16.
4. Pin K25 of the CPU connector has been changed from reserved to VCC_CMOS.
5. A20M#, INIT, SLP, IGNNE NMI,INTR, STPCLK# and SMI are now pulled up to VCC_CMOS.
6. A20M#, INIT, SLP, IGNNE NMI,INTR, STPCLK# and SMI have series resistors and 680 ohm pullups from 2.7K pullups.
7. Removed Pullup on FERR#. Processor assembly or interposer cards must pull this signal up.
8. Modified Boot Block flash to support 28F004B5.
9. Removed Series resistor from MAB12#. Processor Assembly must configure BX FSB frequency.
10. Removed flash daughter card from schematics.
11. Changed MAB12#_R net to FQS.
12. Removed FQS pullups(formerly MAB12#_R).
13. Added R308 as series termination on BXDCLKO.
14. Update RTC Crystal section.
15. Removed speaker connector.
16. Pin names A01-A09 changed to A1-A9 on ISA and DIMM connectors
17. Changed FB1-FB4, FB9 part # to BLM41P750S, 75 Ohm/100 MHz/3 A

Changes made to Revision D.

1. Added Signals PWROK(A24) +12V(A33) MB12#_R(B33) to J19A.
2. Moved J20
3. Added C229 to -PCIRST

Changes made to Revision C.

1. Tied VBAT (pin 65) to 3.3V on Super I/O.

Changes made to Revision B.

1. Swapped AD23 and AD19 on 400 pin connector.
2. Separated CSEL on IDE0 and IDE1
3. Swapped pins 1 and 3 (V5 with TP) on CPU-Fan connector.
4. Tied VBAT (pin 65) to 5.0V on Super I/O.
5. Changed RP48 to 4.7K. (Pullups for mouse and keyboard.)
6. Inverted POWERON# signal (SUSC#) from PIIX4 to control soft-on feature.
7. Changed Bulk decoupling on +12 and -12 to 2x220uF from 2x400uF.
8. Changed Bulk decoupling cap C154 from 10uF to 47uF to reduce BOM line items.

Revision E

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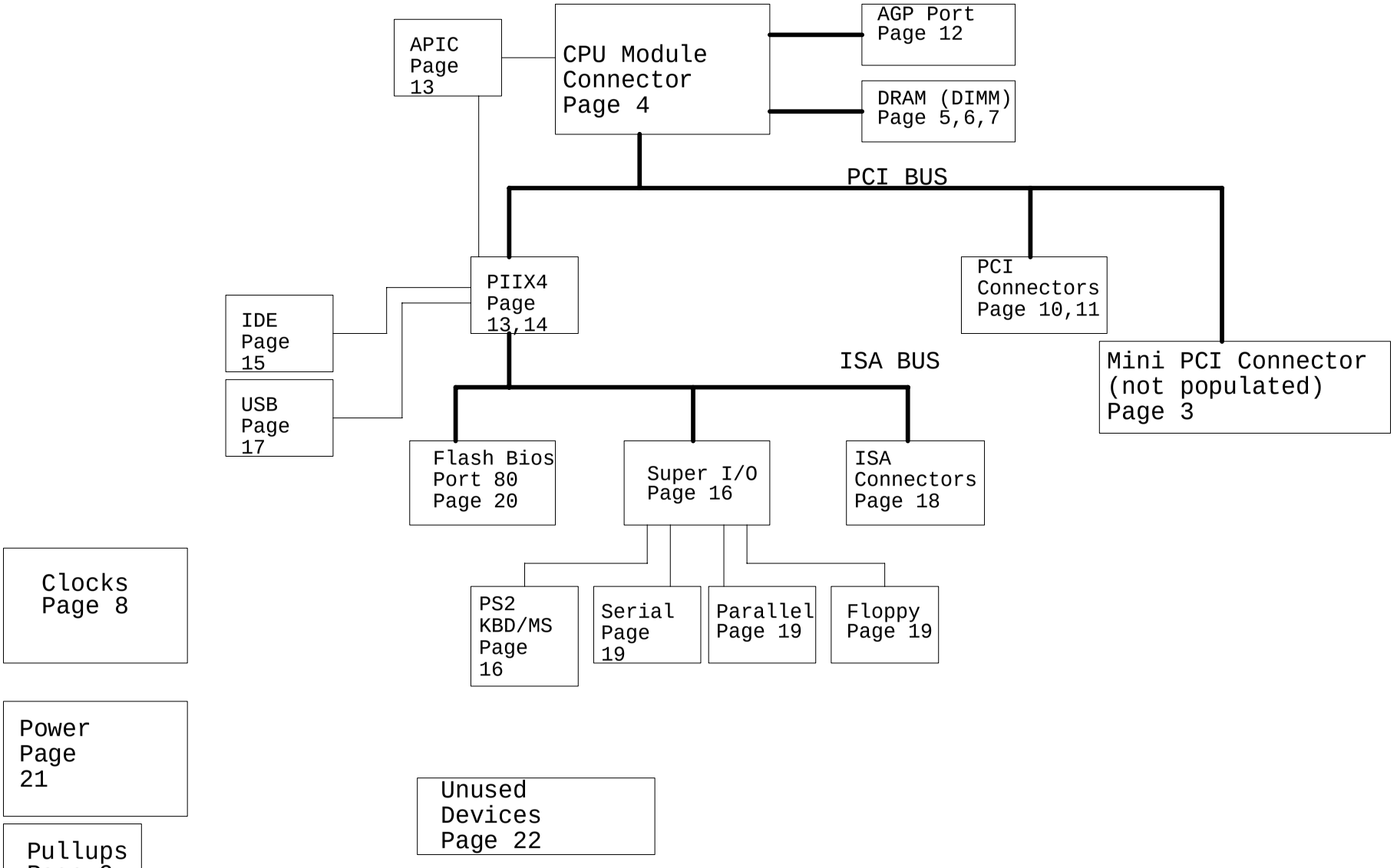

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Date: Friday, February 16, 2001	Sheet 2 of 22	

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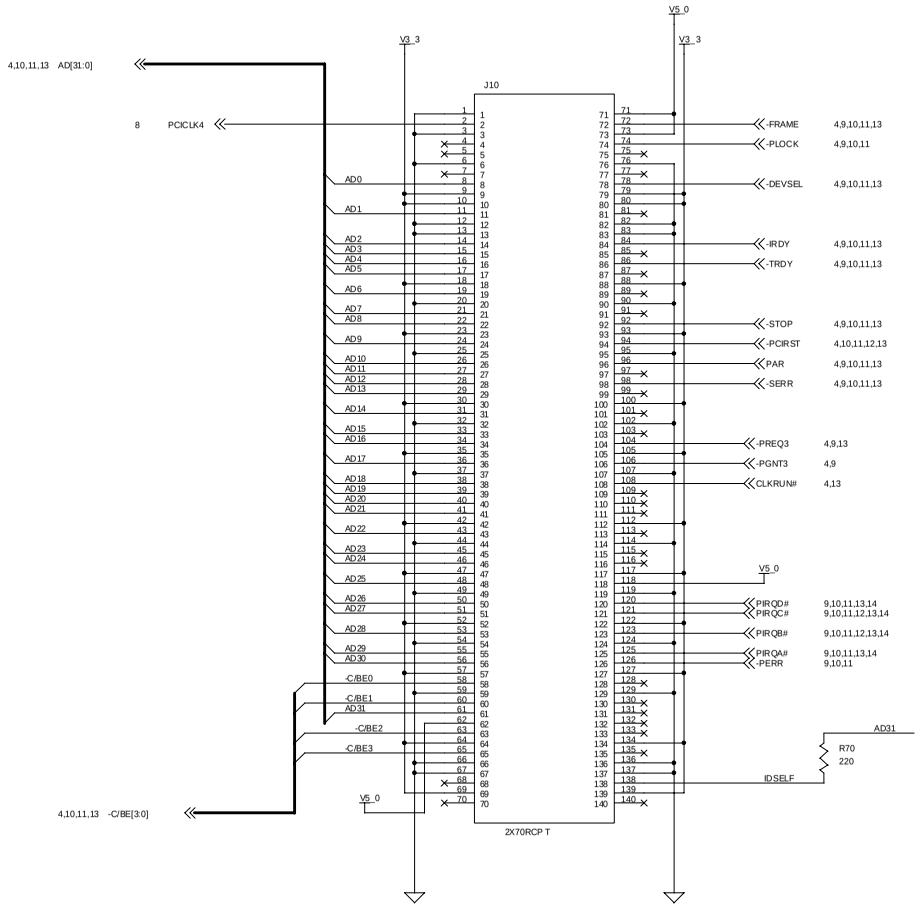

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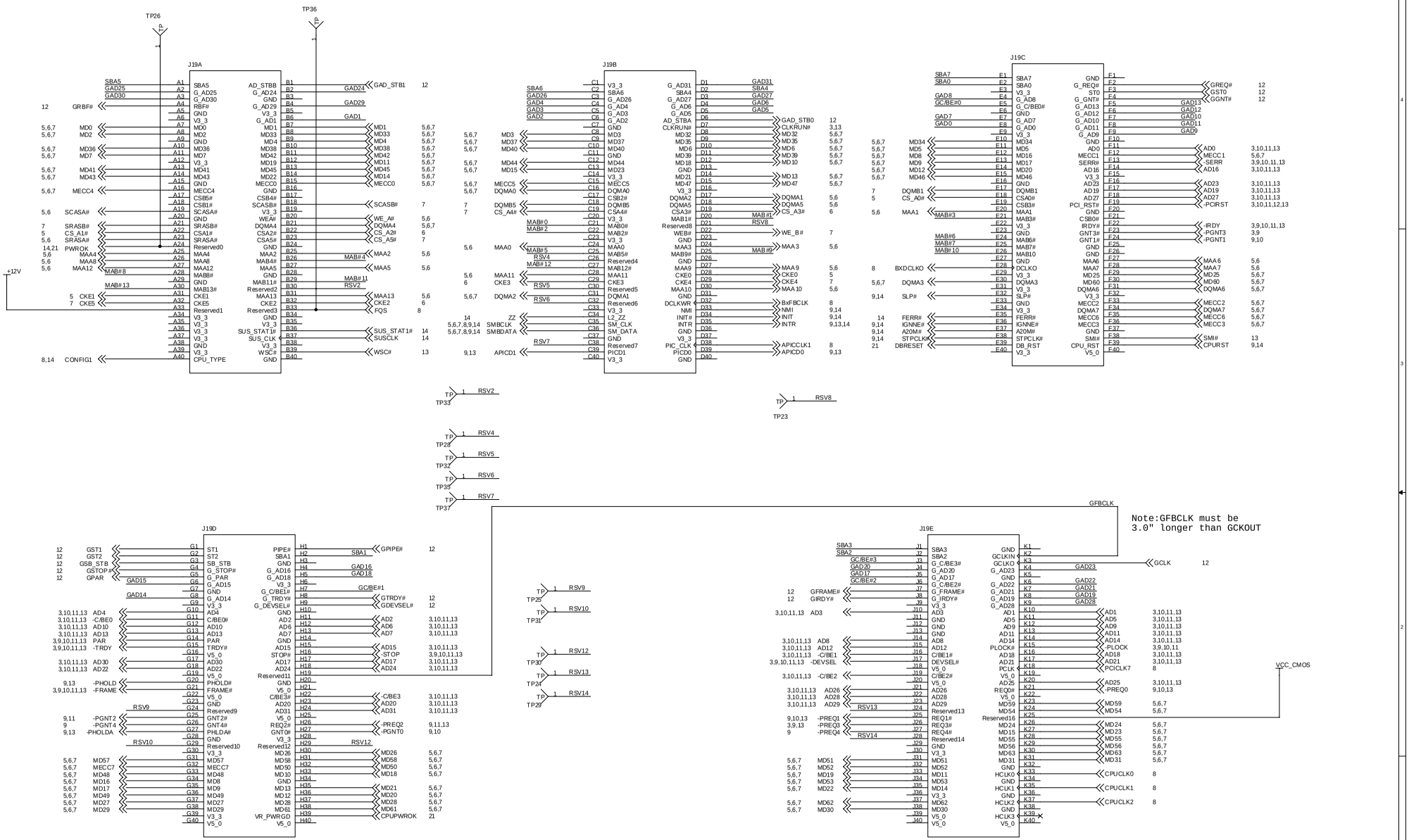

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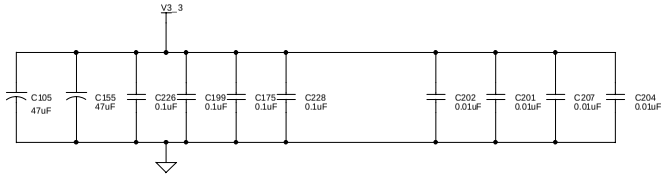
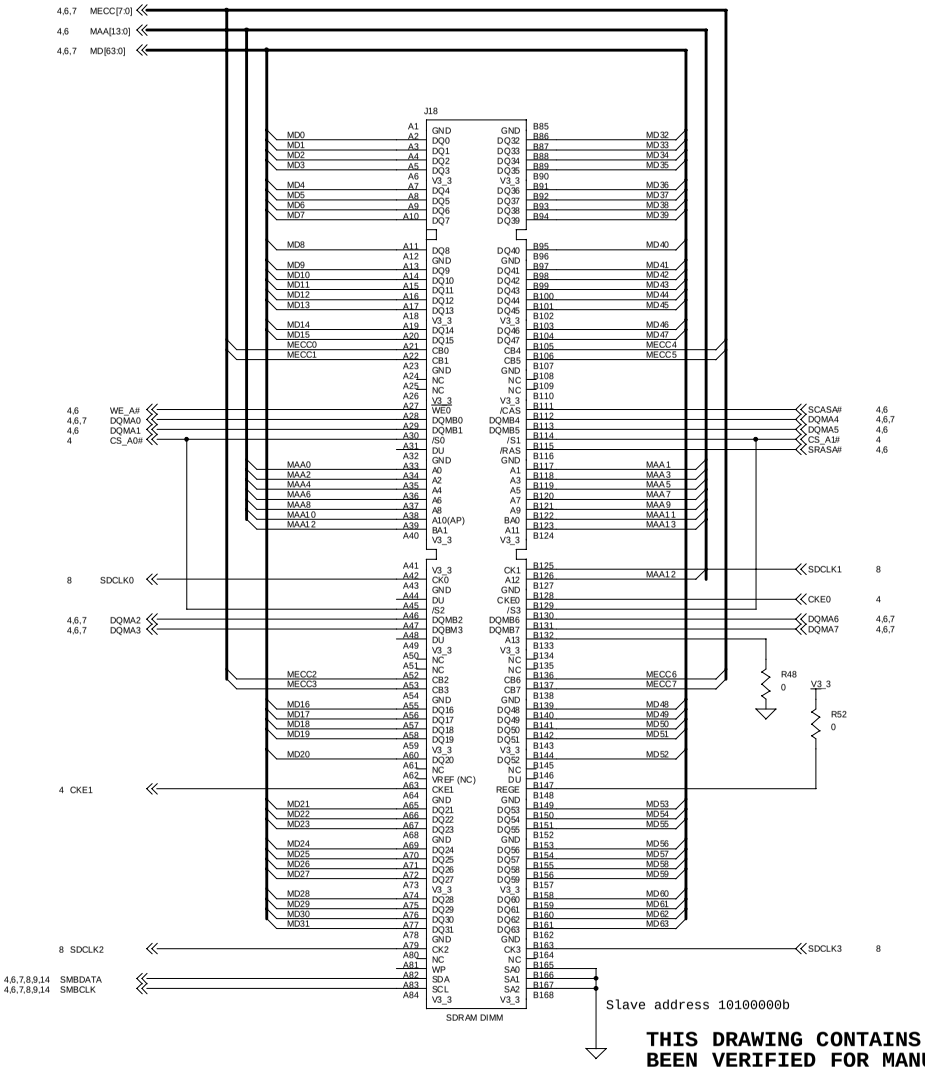
Size: C	Document Number: <Doc>		Rev: E
Date: Friday, February 16, 2001	Sheet 4 of 22		



Socket 0



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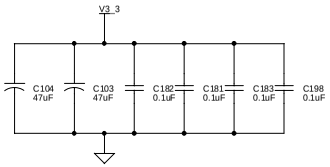
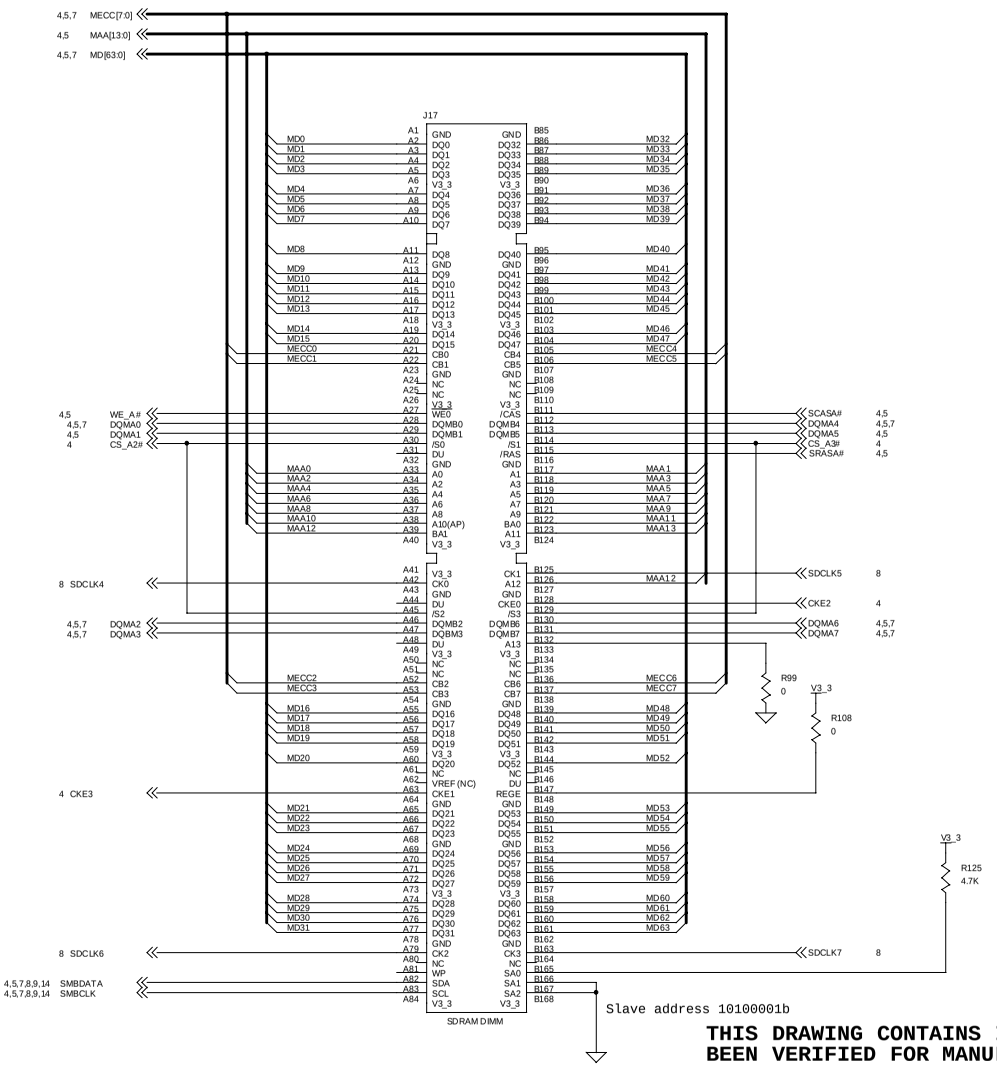
Title: DIMM0		
Size: C	Document Number: <Doc>	Rev: E
Date: Friday, February 16, 2001	Sheet 5 of 22	



Socket 1



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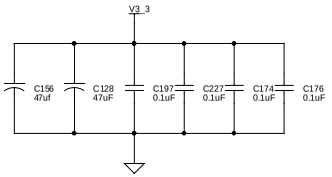
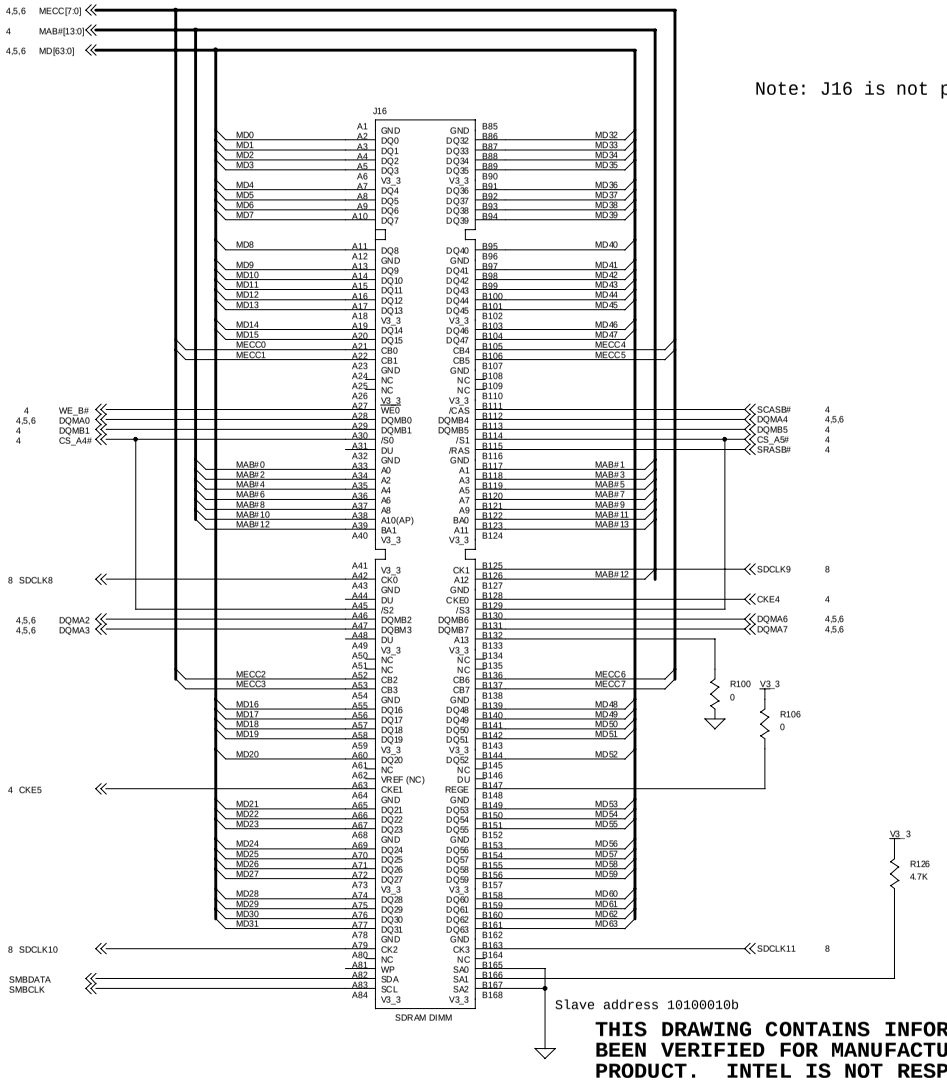
Title: DIMM1			
Size: C	Document Number: <Doc>		Rev: E
Date: Friday, February 16, 2001	Sheet 6 of 22		



Socket 2

Note: J16 is not populated



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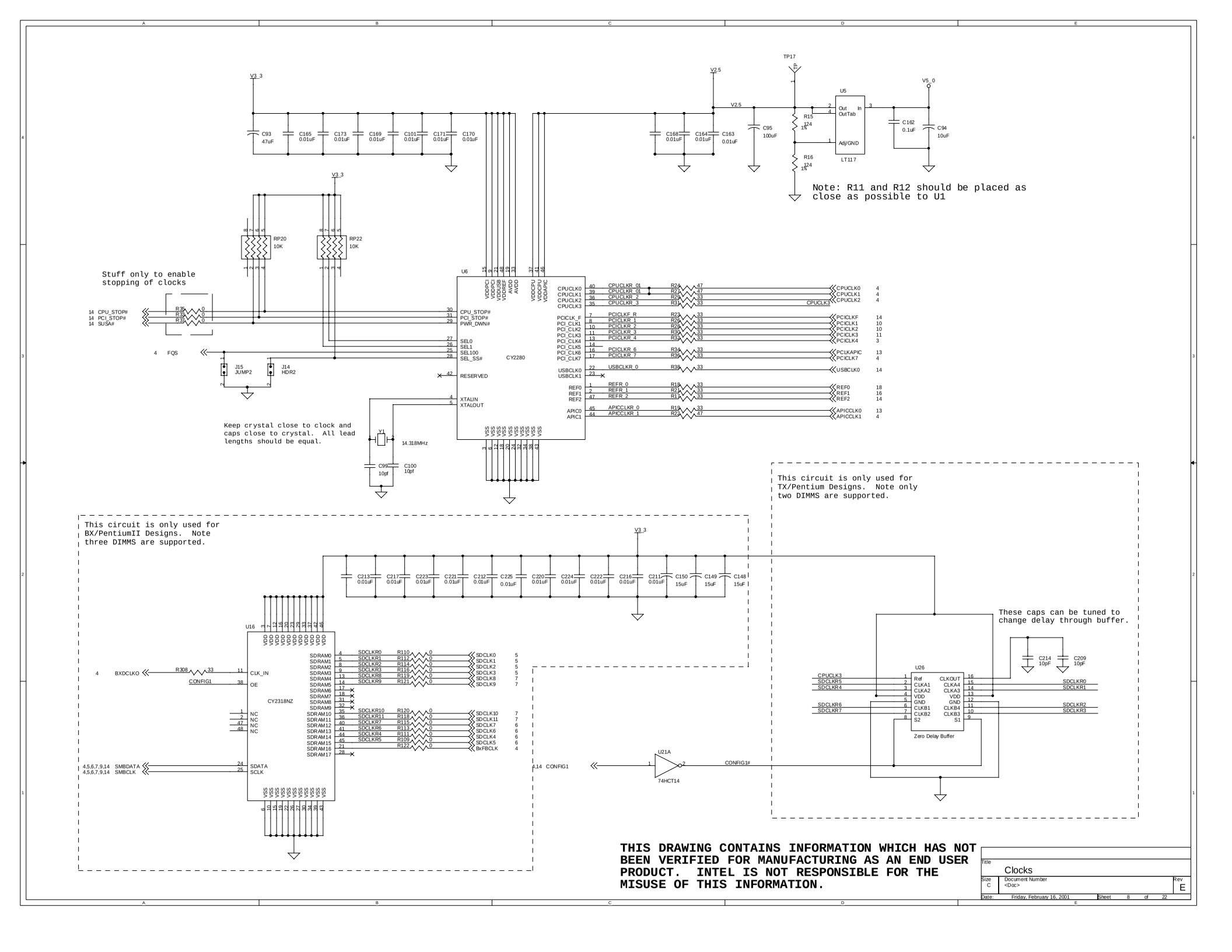
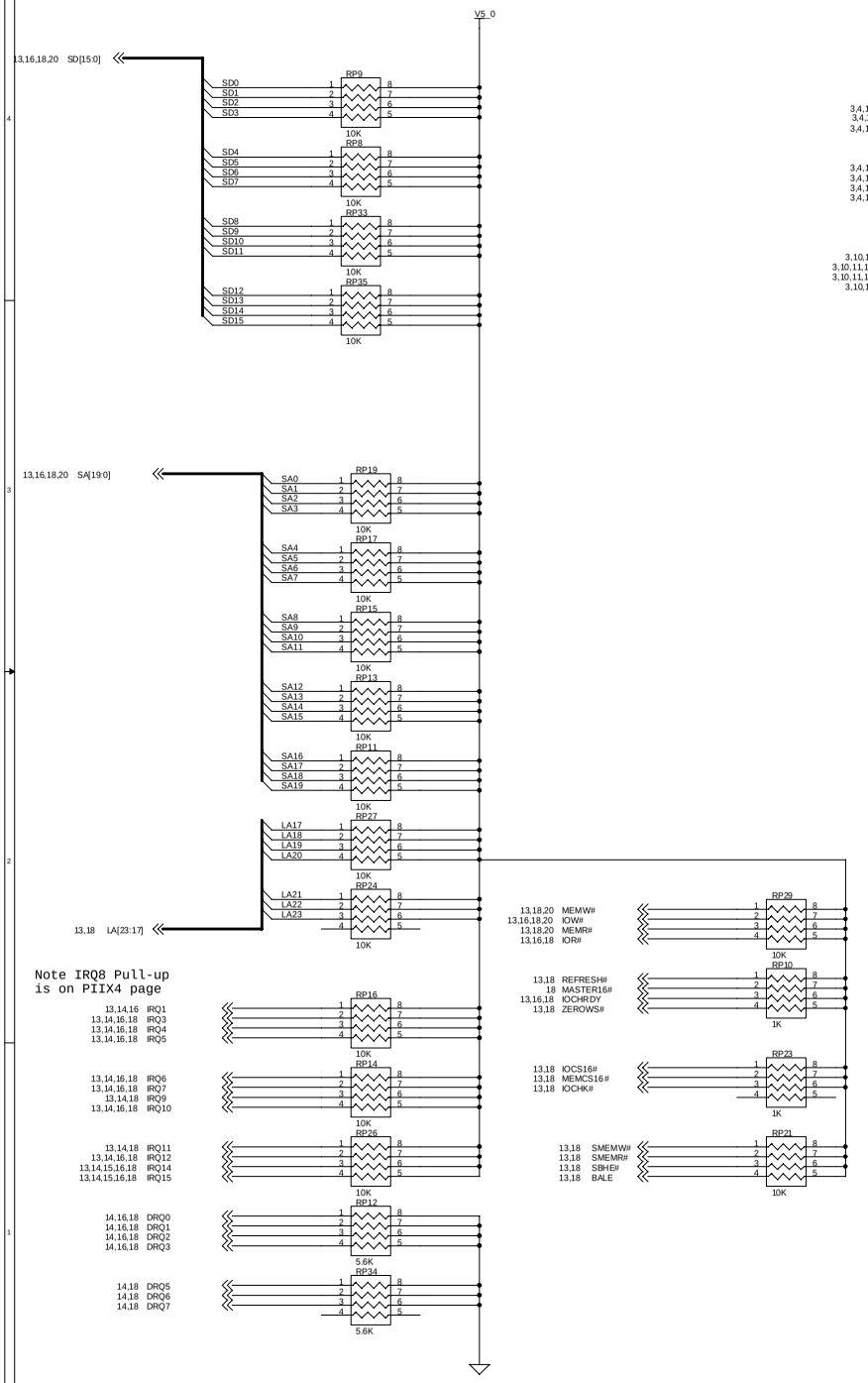
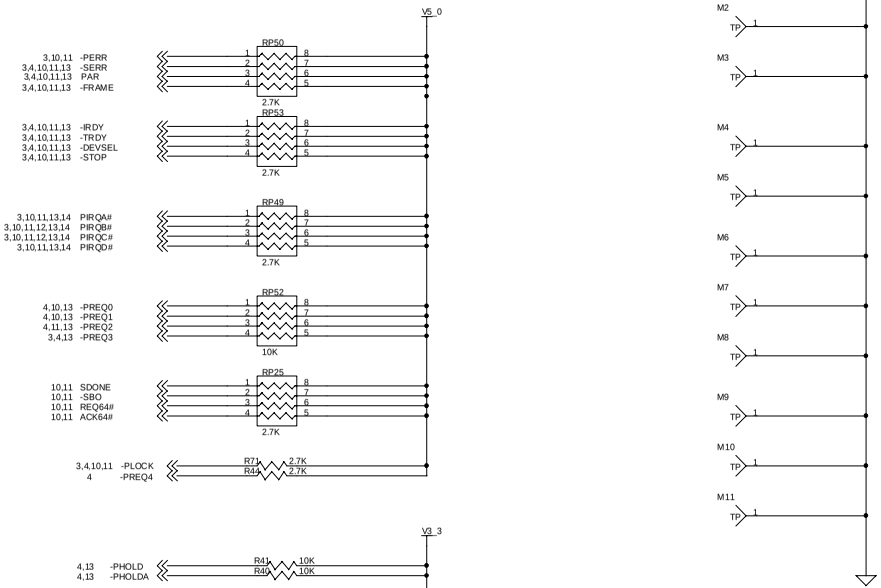
Title	DIMM2	
Size: C	Document Number: <Doc>	Rev: E
Date: Friday, February 16, 2001	Sheet 7 of 22	


Note: R11 and R12 should be placed as close as possible to U1
Stuff only to enable stopping of clocks
Keep crystal close to clock and caps close to crystal. All lead lengths should be equal.
This circuit is only used for BX/PentiumII Designs. Note three DIMMS are supported.
This circuit is only used for TX/Pentium Designs. Note only two DIMMS are supported.
These caps can be tuned to change delay through buffer.
CY2280
CY2318NZ
Zero Delay Buffer
LT117
74HCT14
THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.
Title
Clocks
Size C
Document Number <Doc>
Rev E
Date: Friday, February 16, 2001
Sheet 8 of 22

ISA Pullups



PCI Pullups



Title	ISA/PCI Pullups	
Size C	Document Number <Doc>	Rev E
Date: Friday, February 16, 2001	Sheet 9 of 22	

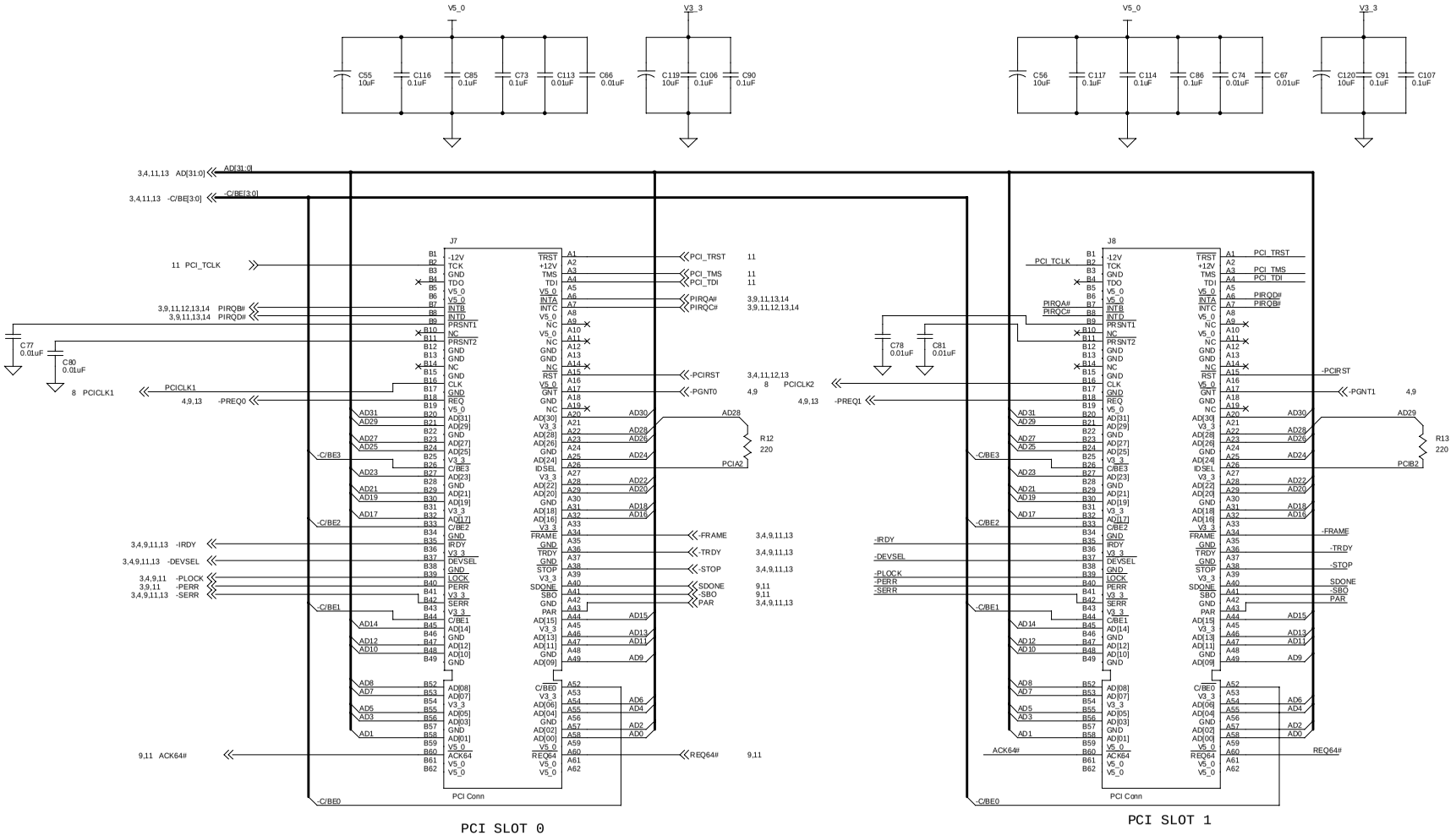
J7/J8 V5_0:
    A5, A8, A10, A16, A59, A61, A62 | A1, A3, A4
    B5, B6, B19, B22, B59, B61, B62

J7/J8 V3_3:
    A21, A27, A33, A39 A45, A53
    B25, B31, B36, B41, B43, B54

J7/J8 NC:
    A9, A11, A14, A19
    B10, B14

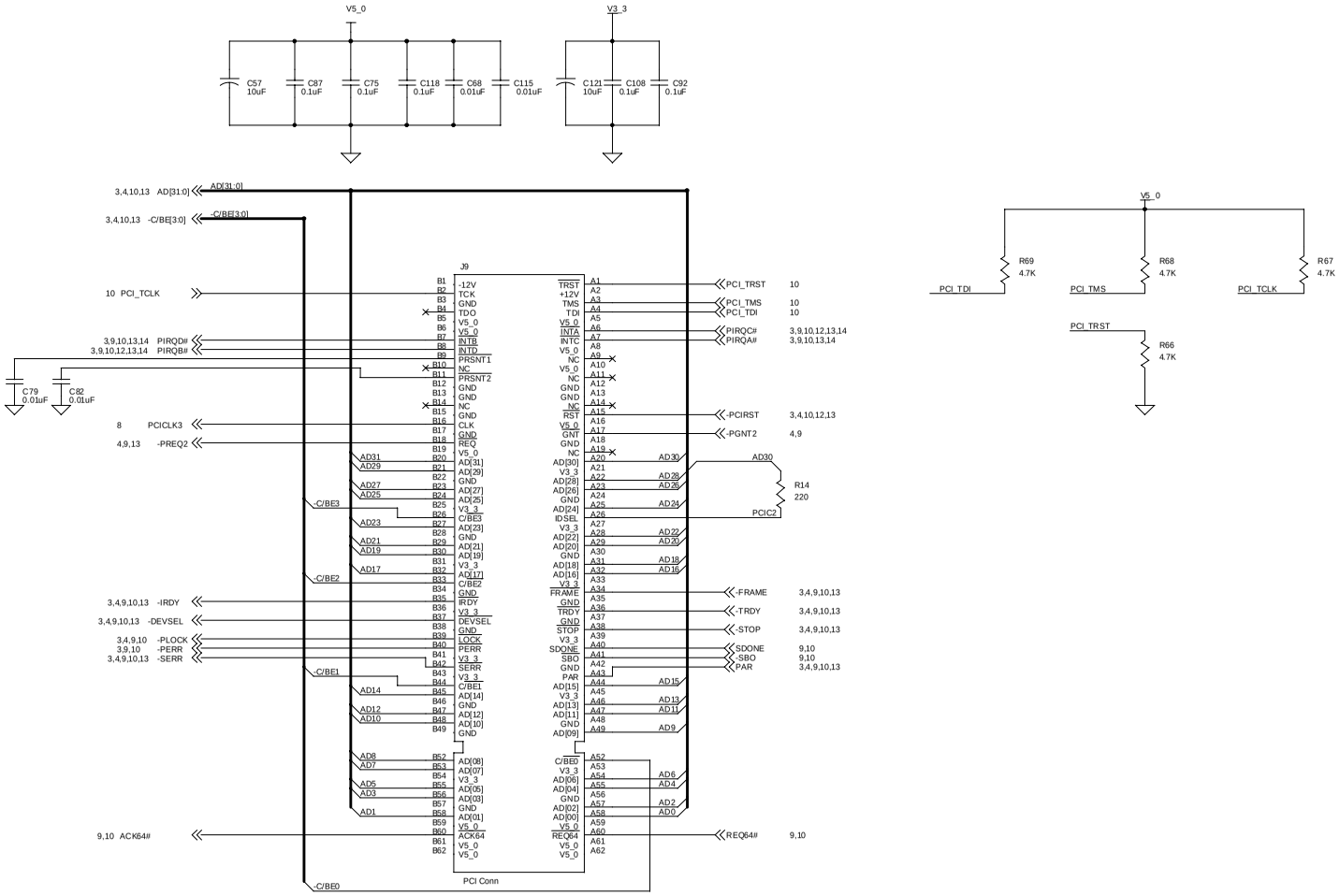
J7/J8 GND:
   A12, A13, A18, A24, A30, A35, A37, A42, A48, A56
   B3, B12, B13, B15, B17, B28, B34, B38, B46, B49,
B57

J7/J8 +12V: A2
      -12V: B1



THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Title: PCI Slots 0 & 1		
Size: C	Document Number: <Doc>	Rev: E
Date: Friday, February 16, 2001	Sheet 10 of 22	



PCI SLOT 2

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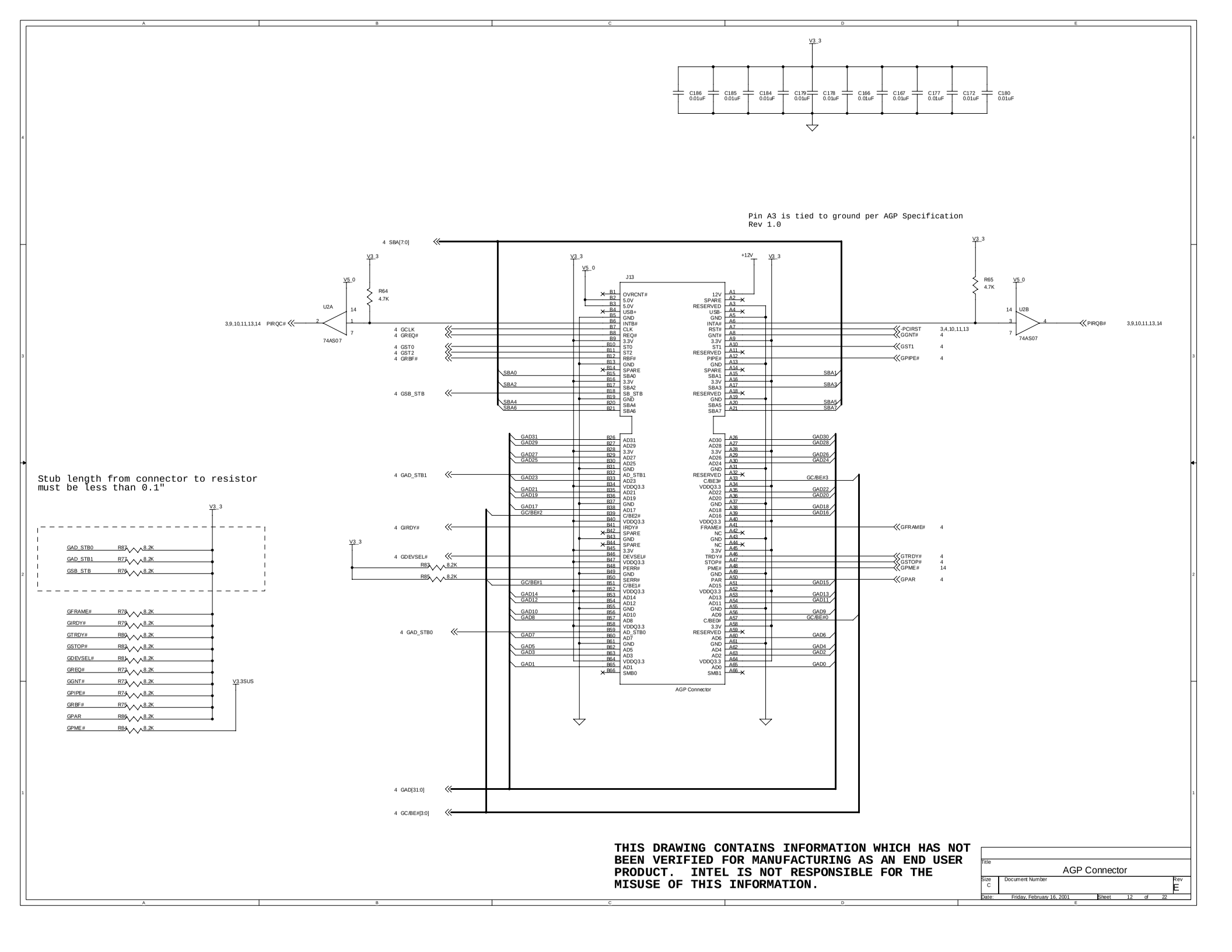
Title: PCI Slot 2		
Size: C	Document Number: <Doc>	Rev: E
Date: Friday, February 16, 2001	Sheet 11 of 22	



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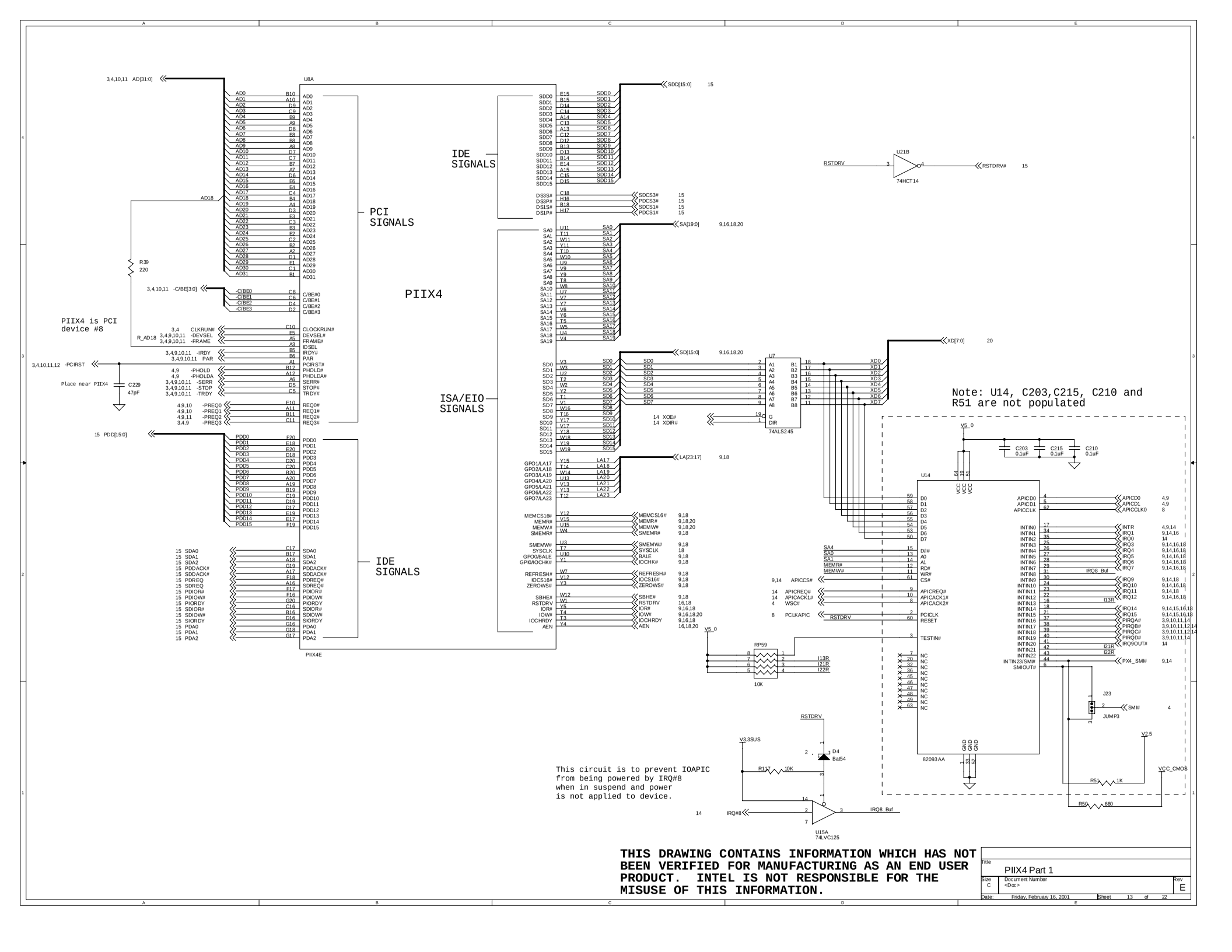
Title	AGP Connector		
Size C	Document Number		Rev E
Date: Friday, February 16, 2001	Sheet 12 of 22		


PIIX4 is PCI device #8
PCI SIGNALS
IDE SIGNALS
PIIX4
ISA/EIO SIGNALS
IDE SIGNALS
PIIX4E
U8A
Note: U14, C203,C215, C210 and R51 are not populated
This circuit is to prevent IOAPIC from being powered by IRQ#8 when in suspend and power is not applied to device.
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Title
PIIX4 Part 1
Size C
Document Number <Doc>
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Date: Friday, February 16, 2001
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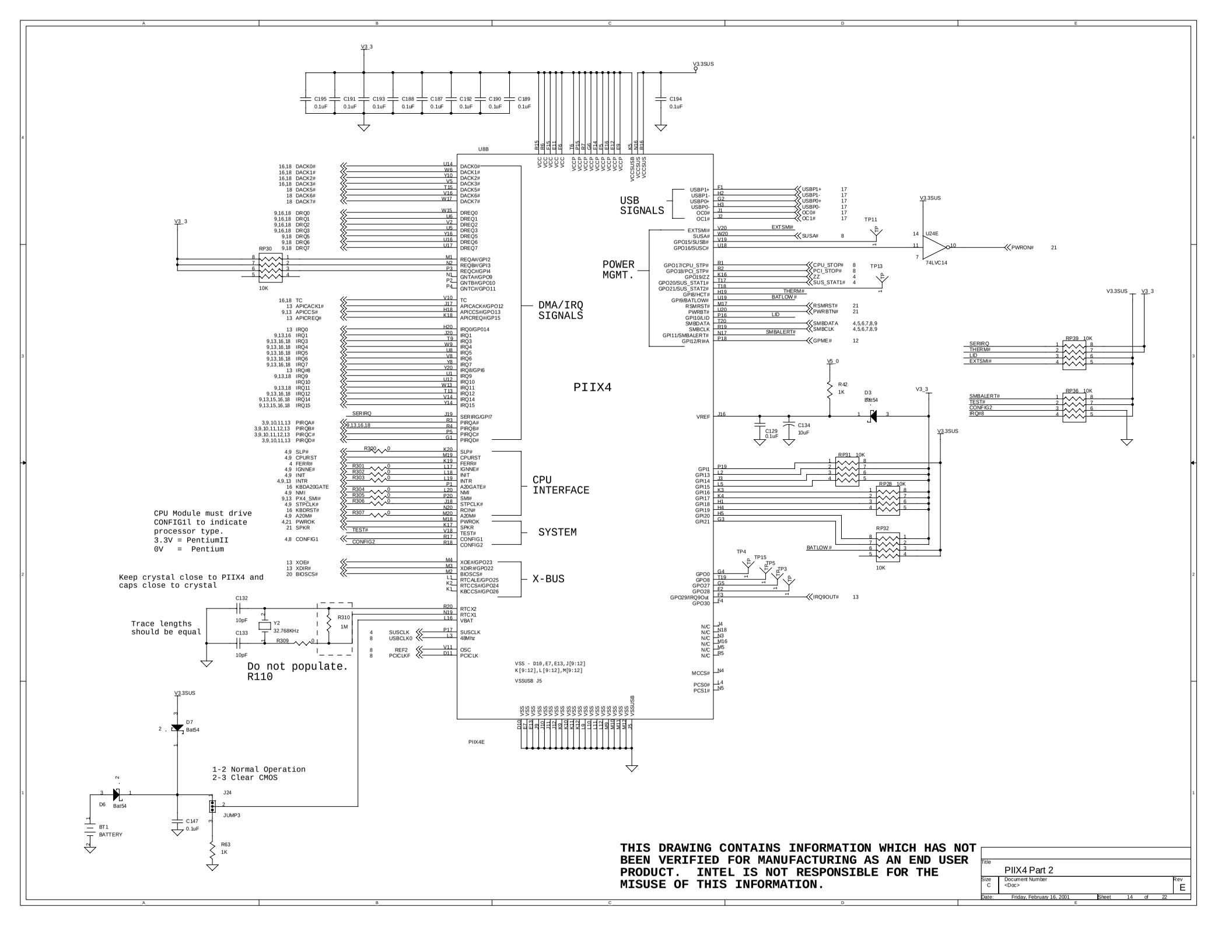
PIIX4
DMA/IRQ SIGNALS
CPU INTERFACE
SYSTEM
X-BUS
USB SIGNALS
POWER MGMT.
U8B
PIIX4E
CPU Module must drive CONFIG1l to indicate processor type.
3.3V = PentiumII
0V = Pentium
Keep crystal close to PIIX4 and caps close to crystal
Trace lengths should be equal
Do not populate. R110
1-2 Normal Operation
2-3 Clear CMOS
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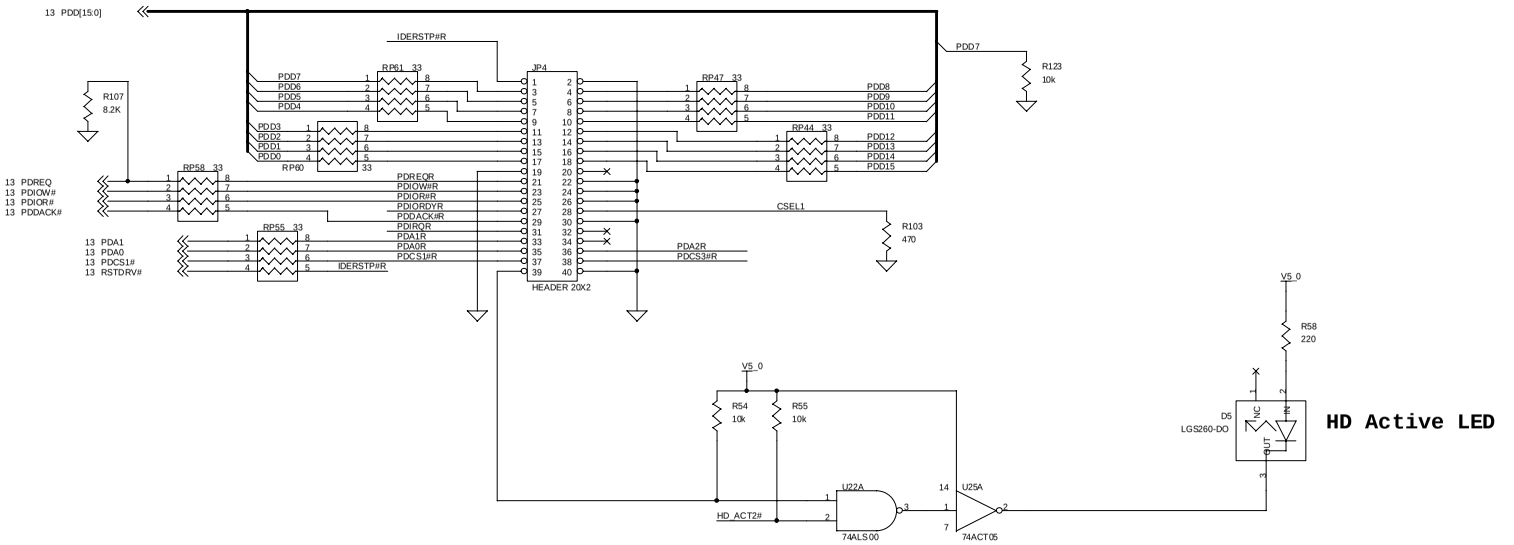
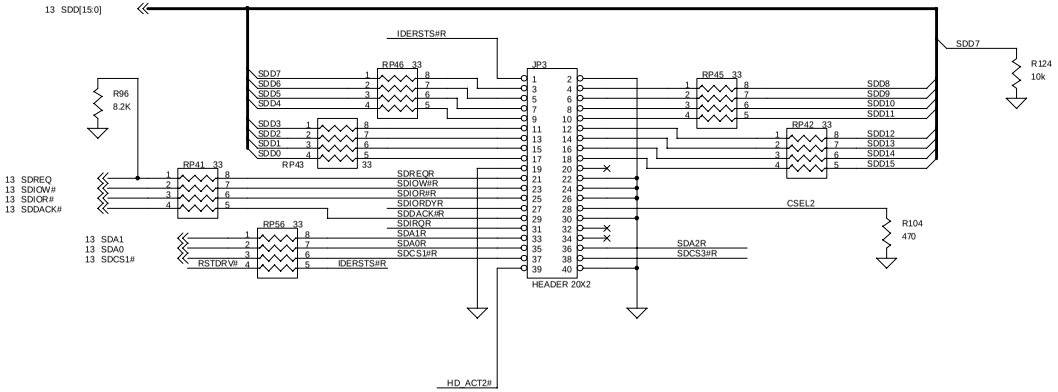
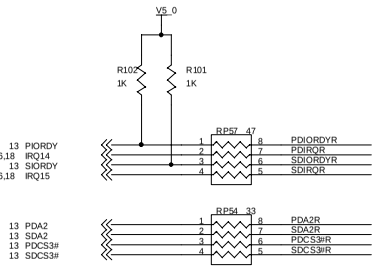
Title
PIIX4 Part 2
Size C
Document Number <Doc>
Rev E
Date: Friday, February 16, 2001
Sheet 14 of 22

Primary IDE Connector



Secondary IDE Connector





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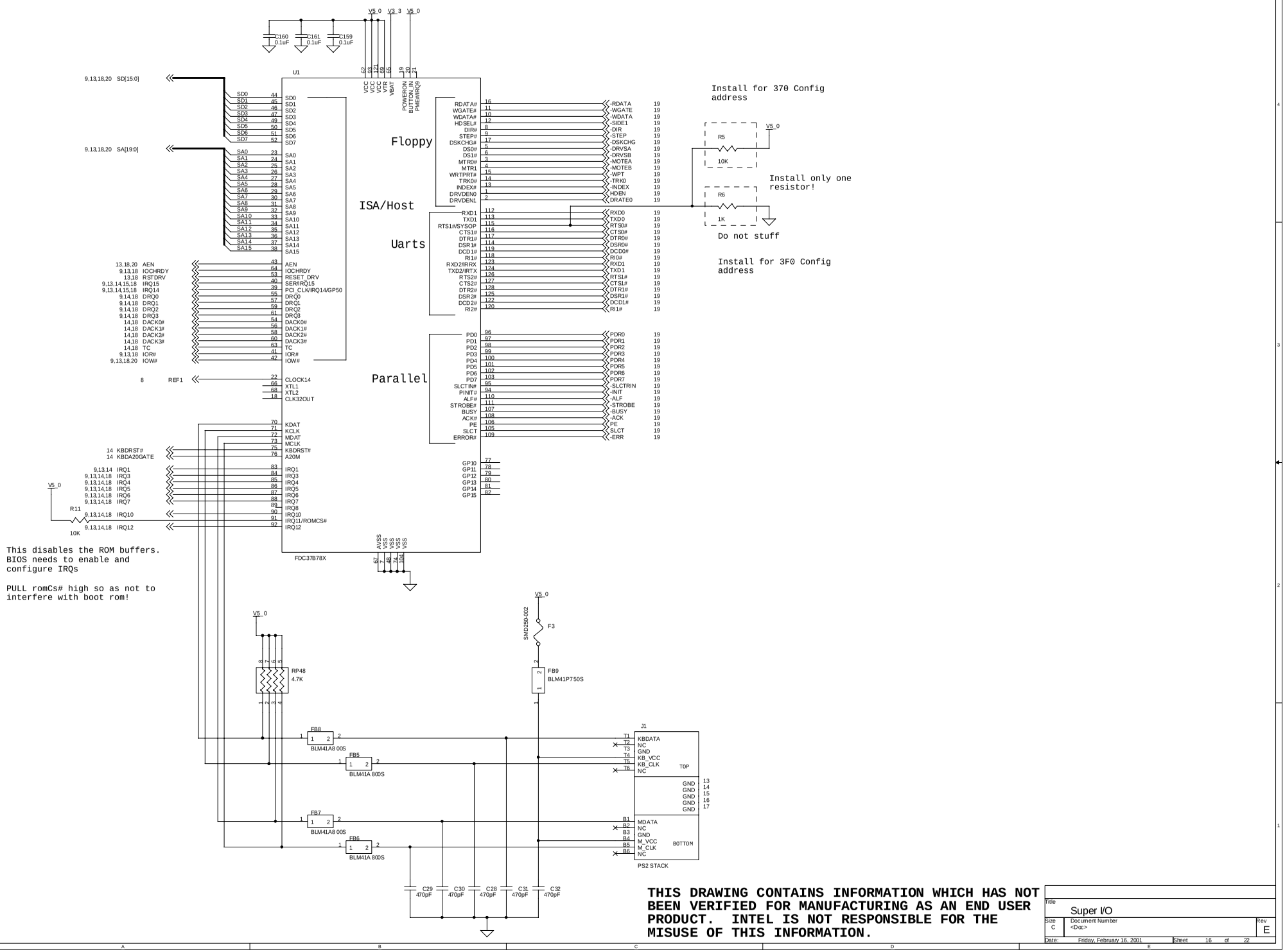
Title: IDE Connectors		
Size: C	Document Number: <Doc>	Rev: E
Date: Friday, February 16, 2001	Sheet 15 of 22	



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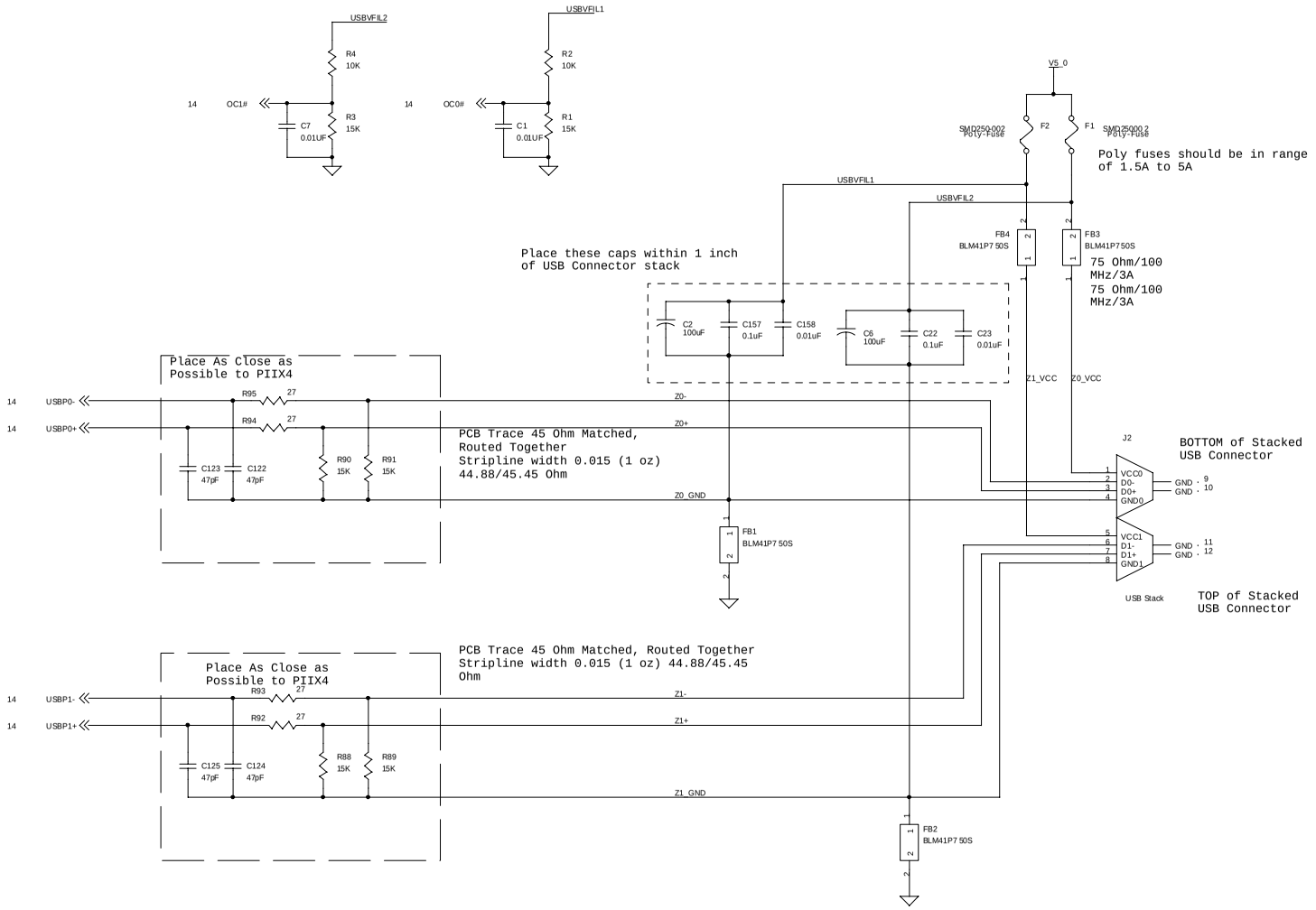
Title: Super I/O			
Size: C	Document Number: <Doc>		Rev: E
Date: Friday, February 16, 2001	Sheet 16 of 22		



NOTE 1: USB differential traces route together (Z0- & Z0+) and (Z1- & Z1+).
Must be 45 Ohm Matched
Stripline width 0.015 (for 1 oz)->44.88/45.45 Ohm.

NOTE 2: Protect differential traces w/ guard traces or
double space to any other signal.

NOTE 3: Place ferrites at connector.

NOTE 4: Poly-fuse min 1.5A
max 5A.

Title: USB Connectors			
Size: C	Document Number: <Doc>		Rev: E
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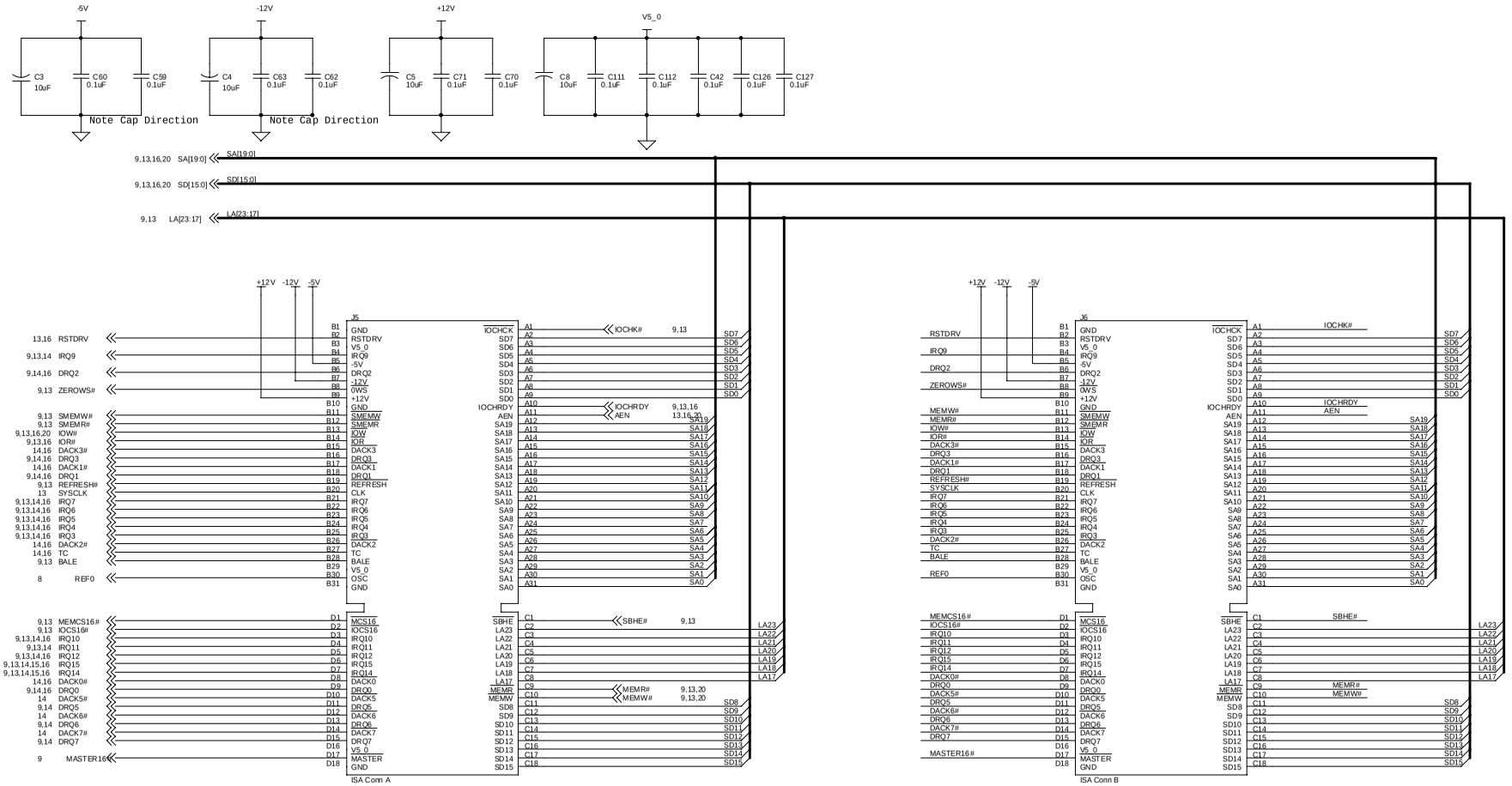
ISA Slots



J5/J6 V5_0:
B03, B29, B31, D16

J5/J6 GND:
B01, B10, D18

J5/J6: +12V B09
-12V B07
-5V B05

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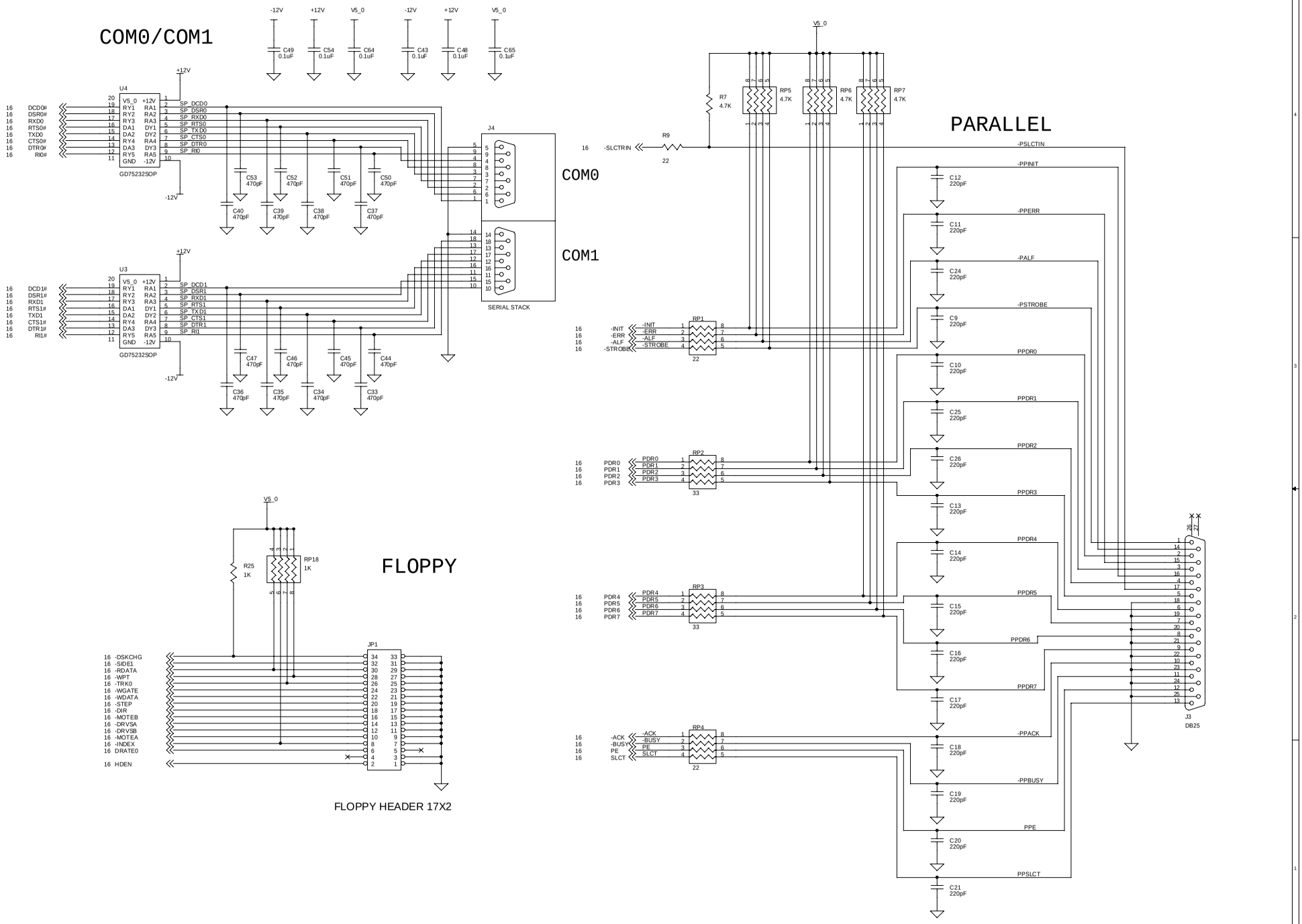
Title: ISA Connectors			
Size: C	Document Number: <Doc>		Rev: E
Date: Friday, February 16, 2001	Sheet 18 of 22		



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Title	COMx, DB25, Floppy	
Size: C	Document Number: <Doc>	Rev: E
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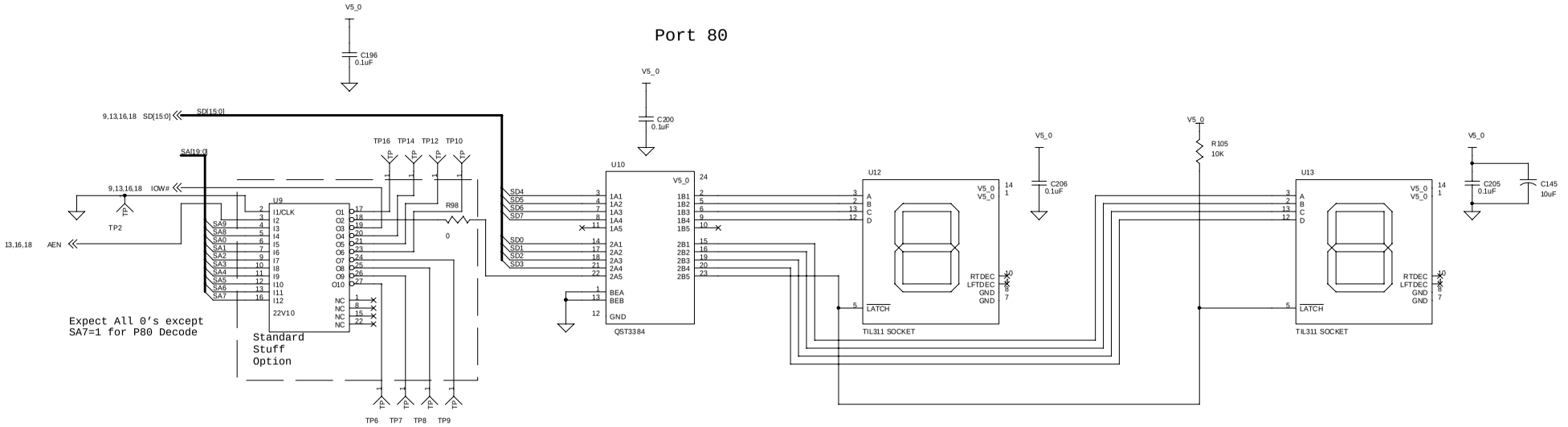
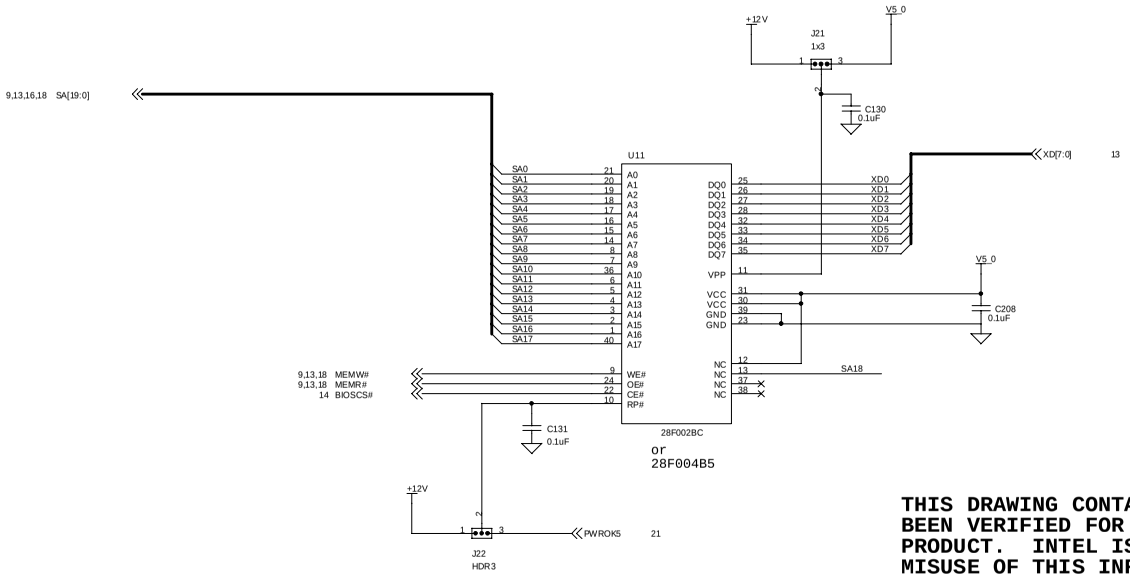
Port 80





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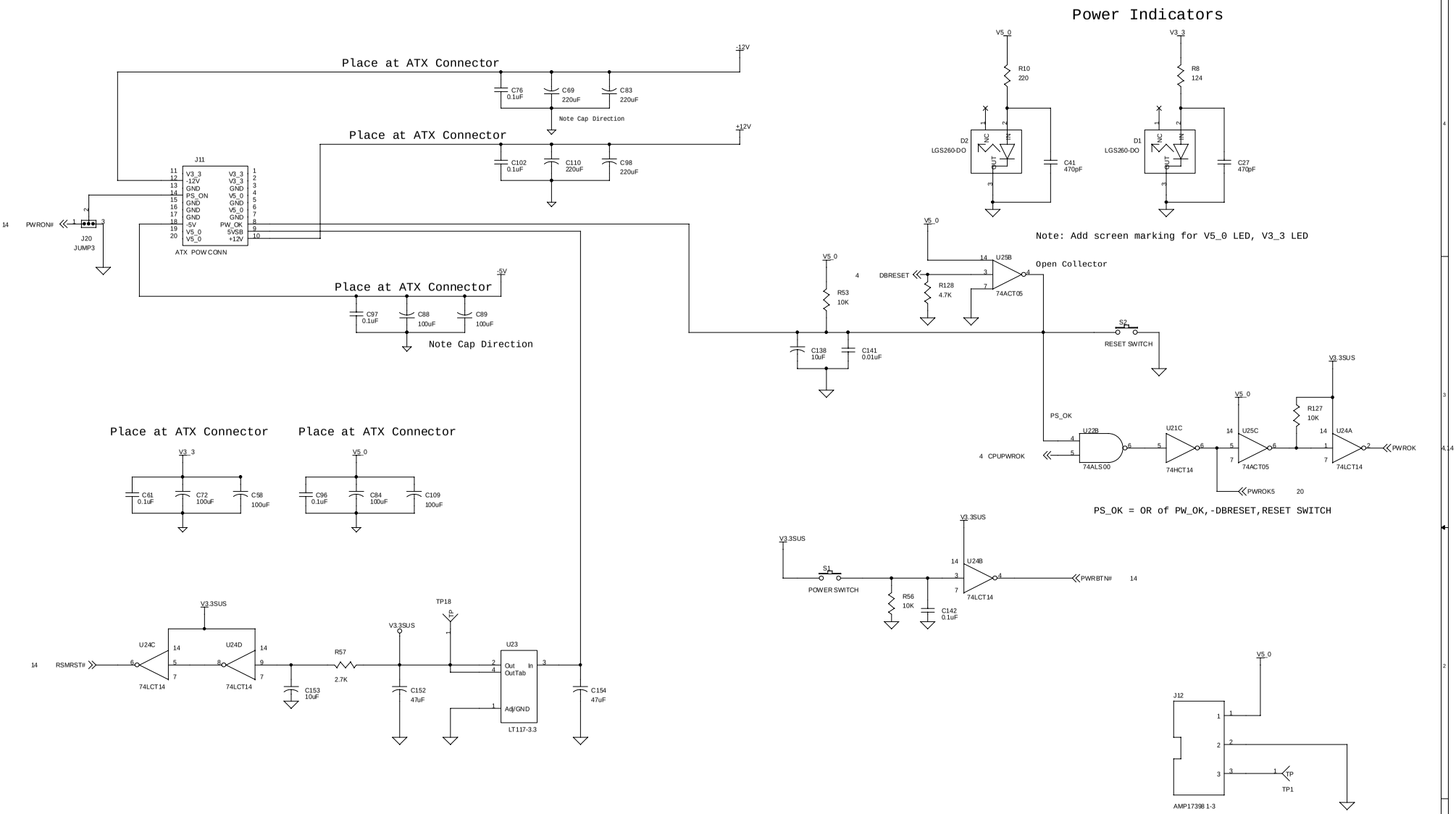
Title: BIOS/ Port 80		
Size: C	Document Number: <Doc>	Rev: E
Date: Friday, February 16, 2001	Sheet 20 of 22	



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Title	ATX Power Connector	
Size C	Document Number <Doc>	Rev E
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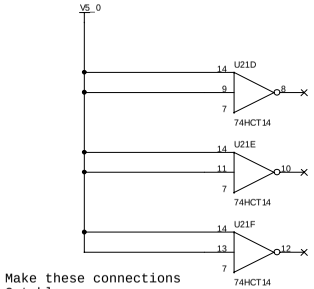
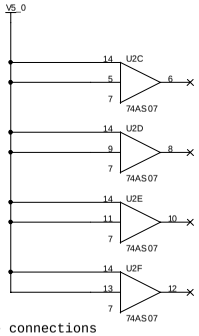
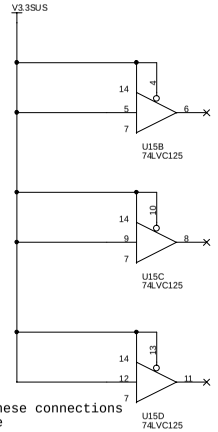


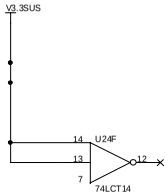
Make these connections
Cutable



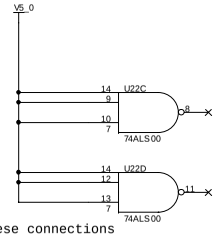
Make these connections
Cutable



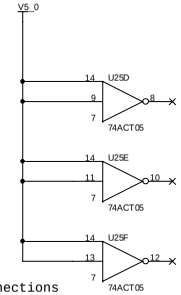
Make these connections
Cutable



Make these connections
Cutable



Make these connections
Cutable



Make these connections
Cutable

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Title: Unused Gates		
Size: C	Document Number: <Doc>	Rev: E
Date: Friday, February 16, 2001	Sheet 22 of 22	

Intel(R) 440BX Scalable Performance Board

Revision A3

History

Rev A3 changes
1. Changed Q6,Q4,Q5,Q7 to Q1,Q2,Q3,Q4 respectively and changed the MOSFET to a Fairchild FDV301N and changed the pinout for the SOT-23 package to correct it.
2. Added a 270 ohm pull-up to PREQ# page 10
3. Corrected the ITP female socket routing. Pinout was correct in A2, but the signals were routed incorrectly.
4. Changed silkscreen to read "Flexible Intel(R) 440BX AGPset/PGA370 Processor adapter"
5. Page 3: Silkscreen pin numbers for Socket-370 on TOP and BOTTOM layers.
6. Changed R6,R7 to 270 ohms
7. Made C1 a Don't Pop.
8. Changed all Don't Pops to have EMPTY as their value. this way they sort together when generating BOM.
9. Page 6, BX. Removed R16,R17,R18. Added silkscreen pin numbering for BX. Added four testpoints to ground under BX. Placed tuning caps C86,87,88 within 1/2 inch of BX.
10. Page 10. Changed 3.3V power to QS3257 to 5.0V. Changed R40 from 3.3K to 270 ohm.
11. BSEL0 pulled to 3.3V. (it was pulled to 2.5V).
12. R105 changed from 680 ohms to 280 ohms.
13. HCLK0,HCLK1 routing changed. These two signals must be on same layer, bottom layer, and not traverse multiple layers.
14. Also, on connector, pin K33, HCLK0 and pin K35, HCLK1 have been swapped. Now, in rev A3, HCLK0 is K35, and HCLK1 is K33. This is to accomodate routing these two signals on the same (bottom) layer. Otherwise, they would have criss-crossed. This has no effect on the circuit since the clocks are tied together on baseboard.
15. The three AGTL+ test signals BNR#,HD4#,HA27# had a min. of 1.6", this has been changed to a min. of 1.8".
16. Page 9. The AGTL+ signals min. has been changed to 1.8" (used to be 1.6").

Rev A2 Changes

HOST INTERFACE
1. Changed socket370 to socket370-256
2. Removed two 74LV07As from Host Interface page since these signals are being pulled up to VCC_CMOS on baseboard.
3. Removed RP1,RP2, R3,R2 pullups for CMOS signals.
4. Removed BSEL# pullup 270 ohm
5. Replaced Q1 with a MOSFET per design guide.
6. Added HRESET# termination on host interface page.
7. Added AH4 RESET pin and connected it to X4 RESET2#
8. Added 650 ohm pullup to FLUSH#

VID/Test Debug/Unused
1. Changed LC PLL component values per Aug 99 flexible design guide
2. Added 10K RP to VID
3. Removed 330 ohm RP from VID
4. Added CMOS conversion logic for THERMTRIP#
5. Added new BSEL0#,BSEL1# circuitry

S370-256 Power
1. Removed 20 1uF bypass caps. They are on the package for CuMine. C10-C24,C30-C34

BX Host Interface
1. Added CPURST# termination and layout guidelines
BX Memory Interface
2. Changed cap on DCLKWR to 20pf from 0.1uF. Removed resisitor.
3. Added 10K series resistor to MAB#12 (removed from baseboard)

Connector
1. VCC_CMOS to RESERVED16
2. Change BSEL# to BSEL0#

GTL+ Termination
1. Added new layout guidelines per flexible design guide Aug 99
2. Added four more VTT decoupling caps to bring the total to 20.
3. Changed 51 ohm pullup on PRDY0# to 150 ohm

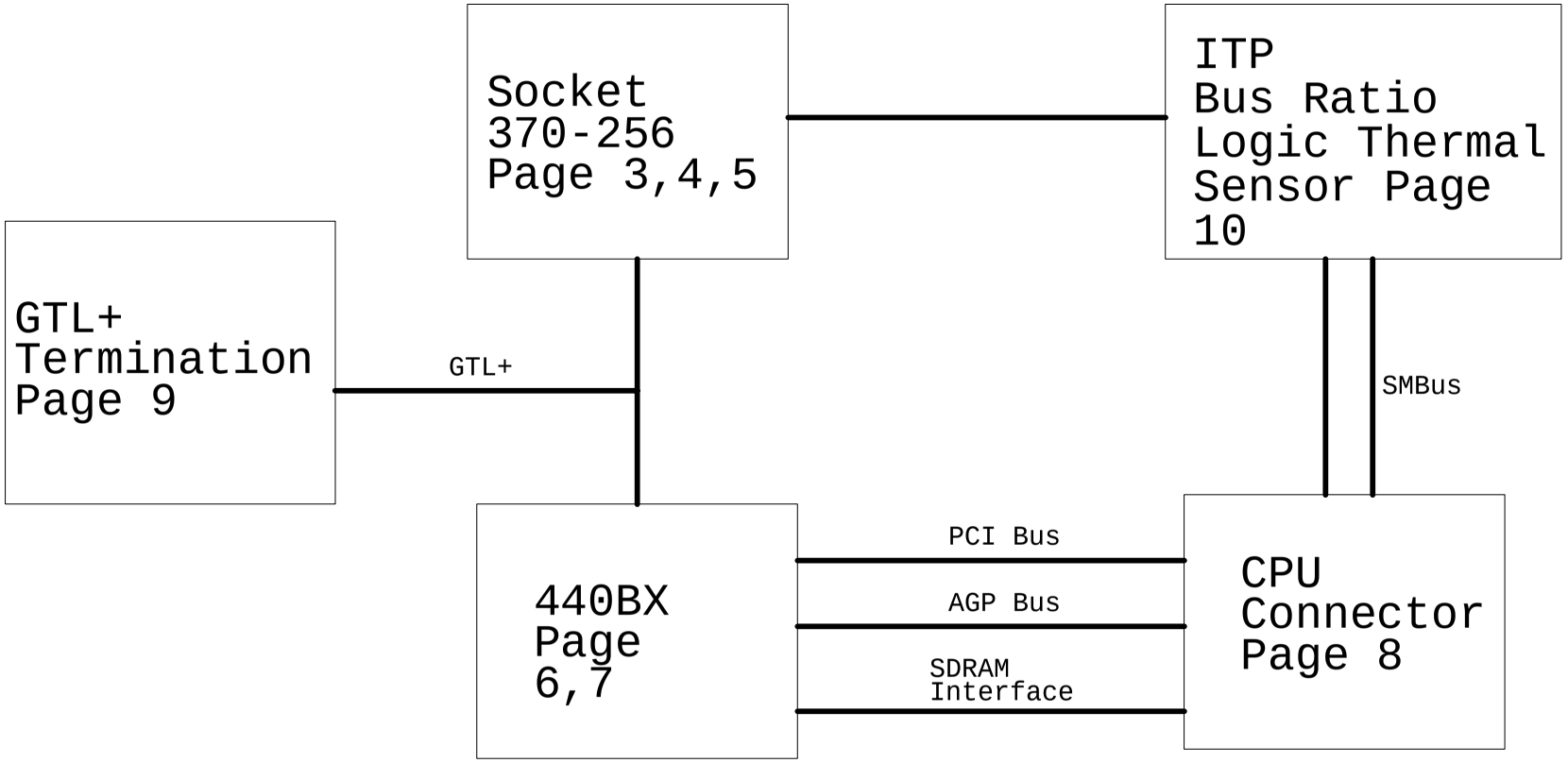
Bus Ratio/Thermal/ITP
1. removed pullup on HRESET# (followed flexible design guide)
2. move 270 ohm as a pullup for STBY# on MAX1617 per datasheet typical operating circuit. This place cap directly on VCC of MAX1617 per datasheet.
3. removed 10K "do not papulate" resistor from STBY#.
4. removed "do not populate" for QS3257
5. added "do not populate" for RP62 0 ohm for QS3257
6. removed R48 51 ohm pullup on PRDY#
7. Added 150 ohm pullups to PRDY1#, PRDY2#, PRDY3#
8. Replaced NAND gate inverter with FET for DBRESET.

Rev A1 Changes

1. Removed translator logic for PREQ0#
2. Removed termination resistors on BX side for GTL+
3. Added 20pF load on HCLK for BX clock compensating

Embedded Intel Architecture Division
Intel Corporation
5000 W. Chandler Blvd
Chandler AZ, 85044

Title	Intel(R) 440BX Scalable Performance Board	
Size C	Document Number	Rev A3
Date: Wednesday, April 26, 2000	Sheet 1 of 12	



Voltage
Regulator
Page 11

Layout
Guidelines
Page 12

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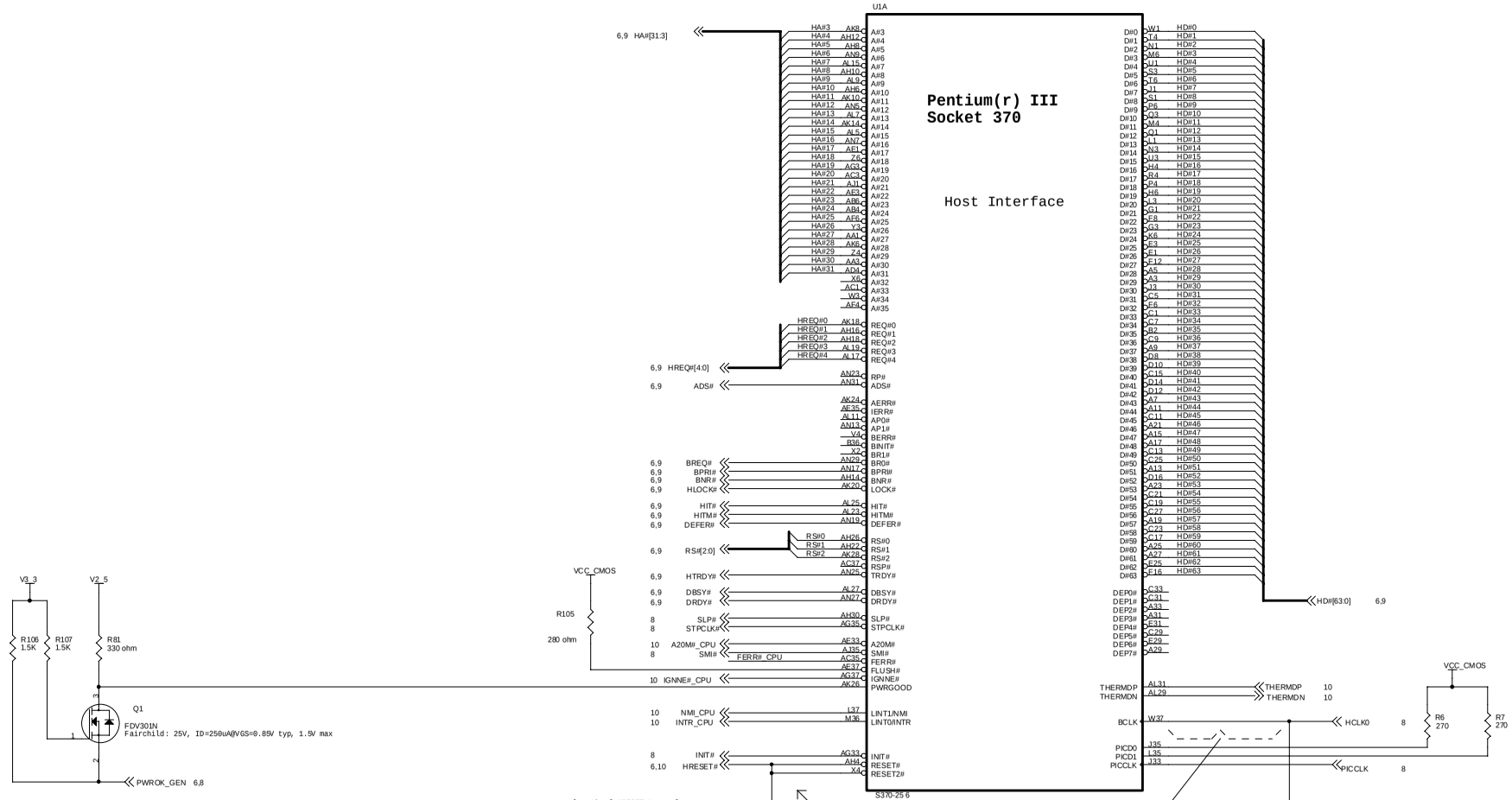
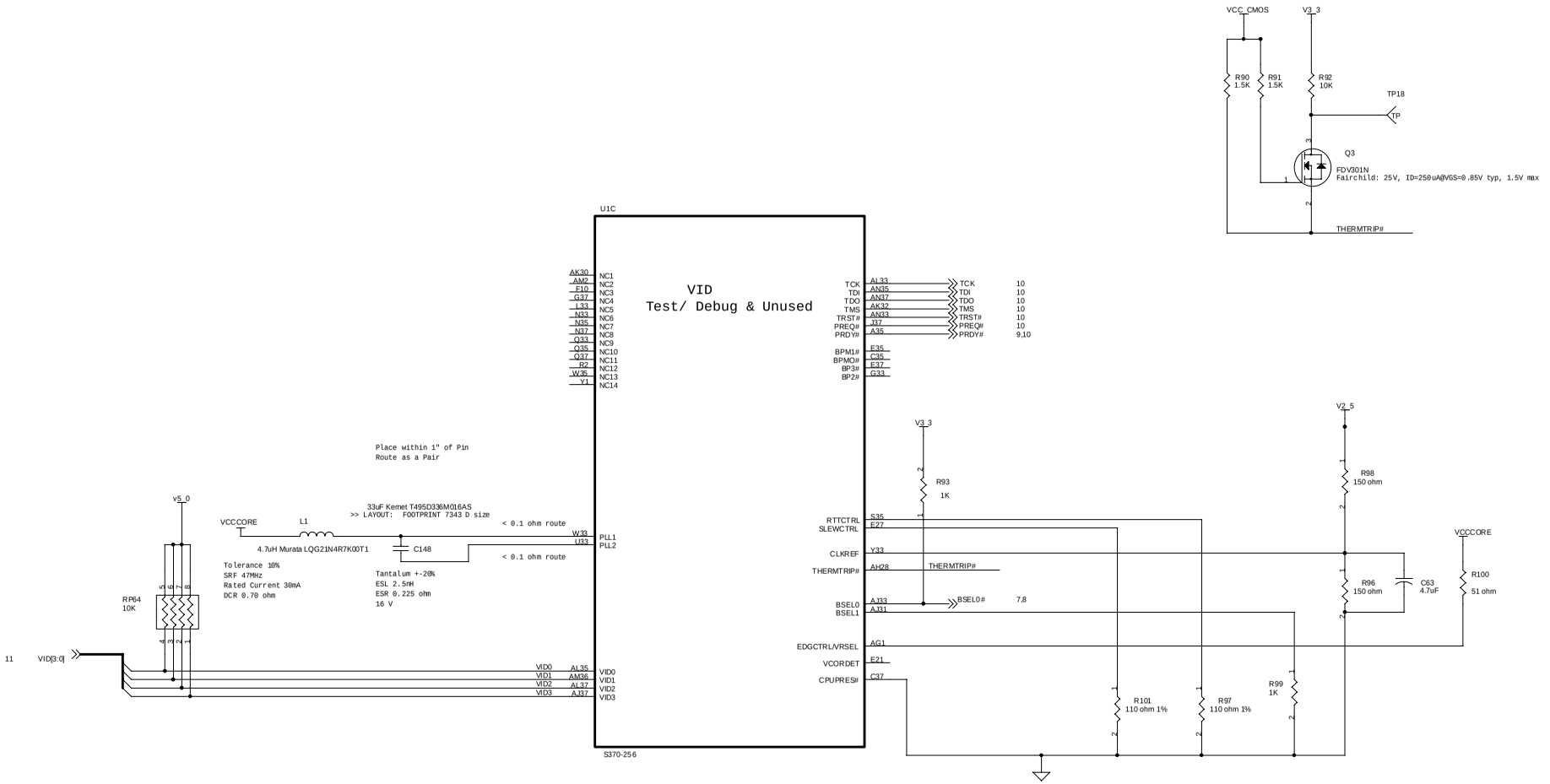
Intel Corporation
5000 W. Chandler Blvd
Chandler AZ, 85044

Title	Diagram	
Size C	Document Number: Intel(R) 440BX Scalable Performance Board	Rev A3
Date: Wednesday, April 26, 2000	Sheet 2 of 12	

>>LAYOUT: Silkscreen. Number socket-370 on top and bottow layer.



Embedded Intel Architecture Division Intel Corporation 5000 W. Chandler Blvd Chandler AZ, 85044	
Title	S370-256 Host Interface
Size: C	Document Number: Intel(R) 440BX Scalable Performance Board — Rev: A3
Date: Wednesday, April 26, 2000	Sheet 3 of 12



Embedded Intel Architecture Division Intel Corporation 5000 W. Chandler Blvd Chandler AZ, 85044	
Title	S370-256 Other
Size C	Document Number: Intel(R) 440BX Scalable Performance Board — Rev A3
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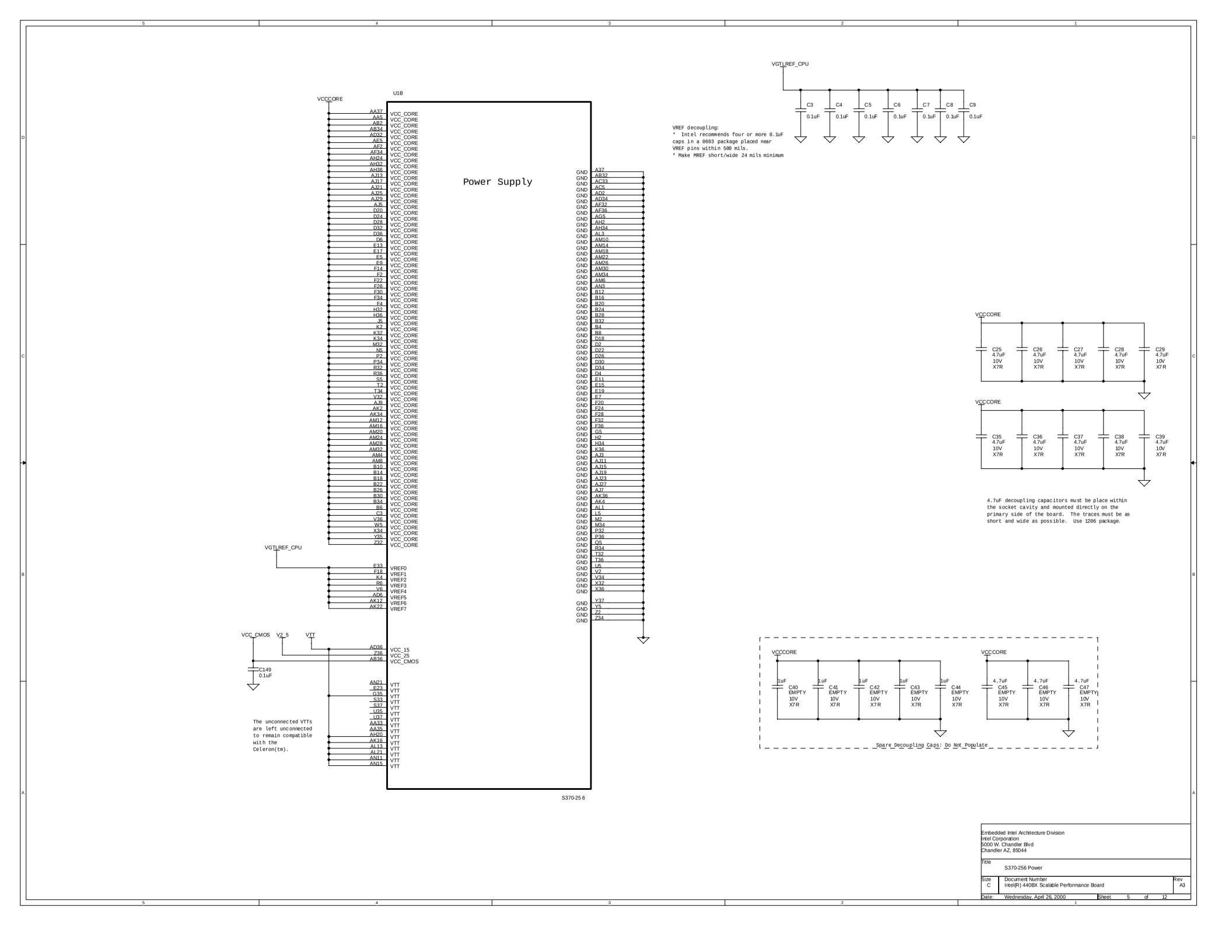

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Chandler AZ, 85044

Title: S370-256 Power

Size: C | Document Number: Intel(R) 440BX Scalable Performance Board | Rev: A3

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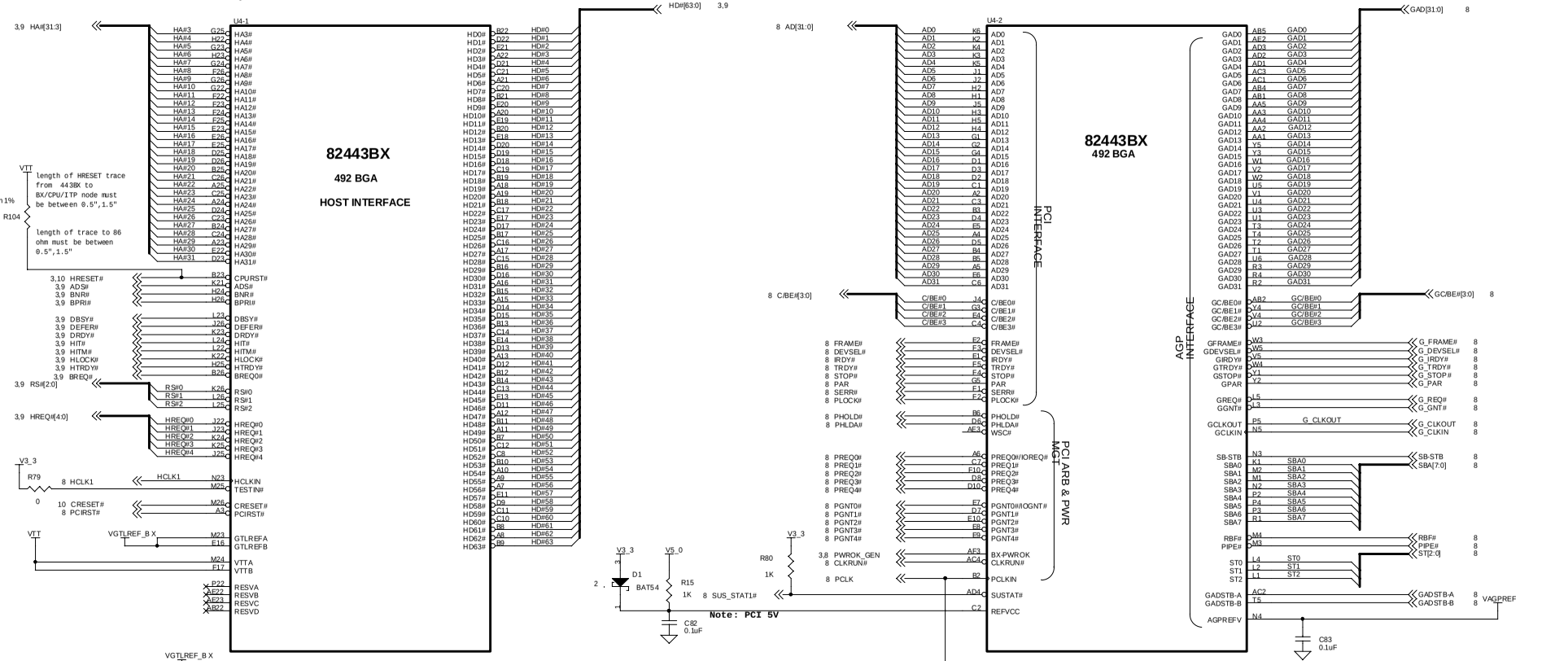
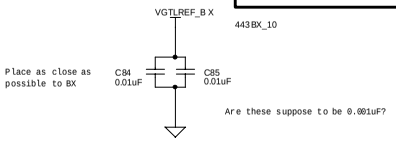
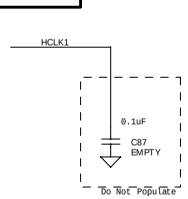
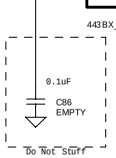
>>LAYOUT: Silkscreen. Put 82443BX pin numbers on both top and bottom layers.



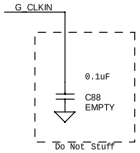




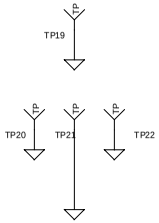
>>LAYOUT: place cap within 1/2 inch of BX.



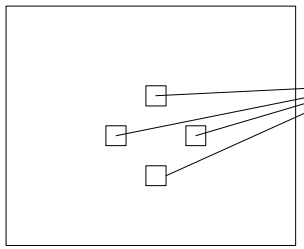
>>LAYOUT: place cap within 1/2 inch of BX.



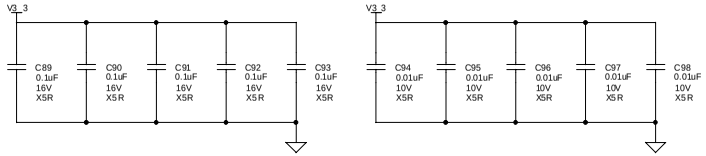
>>LAYOUT: place cap within 1/2 inch of BX.



82443BX bottom view



>>LAYOUT: GROUND PADS within inner ring of balls of BX on bottom layer



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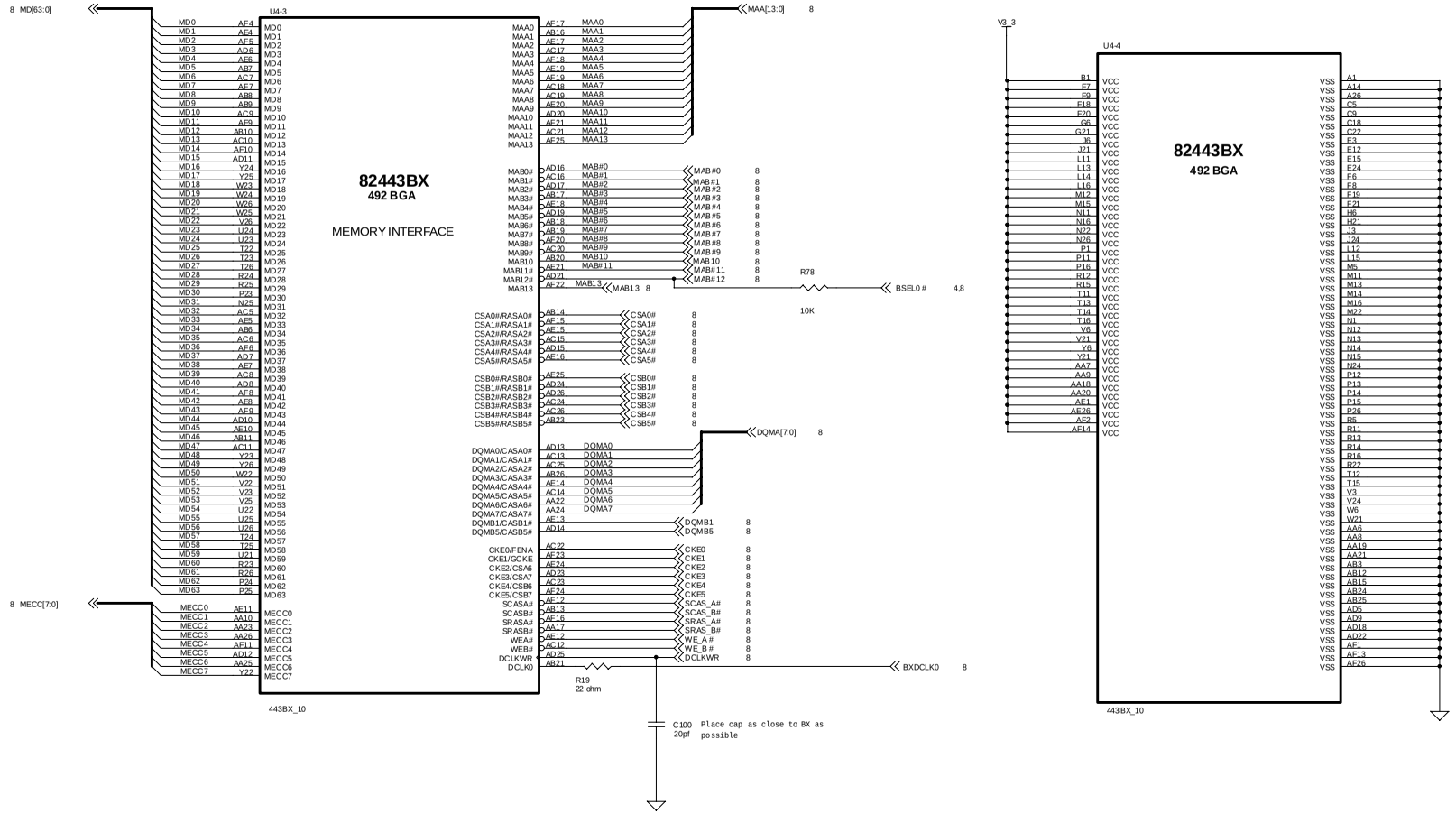
Title: 440BX Host Inteface

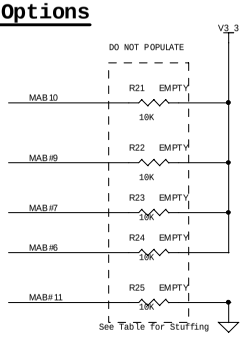
Size: C | Document Number: Intel(R) 440BX Scalable Performance Board | Rev: A3

Date: Wednesday, April 26, 2000 | Sheet 6 of 12



BX Strapping Options

Resistor	Function	Board Default Setting	Signal
R21	Quick Start Select	Do Not Stuff	MAB10#
R22	AGP Disable	Do Not Stuff	MAB9#
R23	Memory Module Configuration	Do Not Stuff	MAB7#
R24	Host Bus Buffer Mode Select	Do Not Stuff	MAB6#
R25	In-Order Queue Depth Enable.	Do Not Stuff	MAB11#



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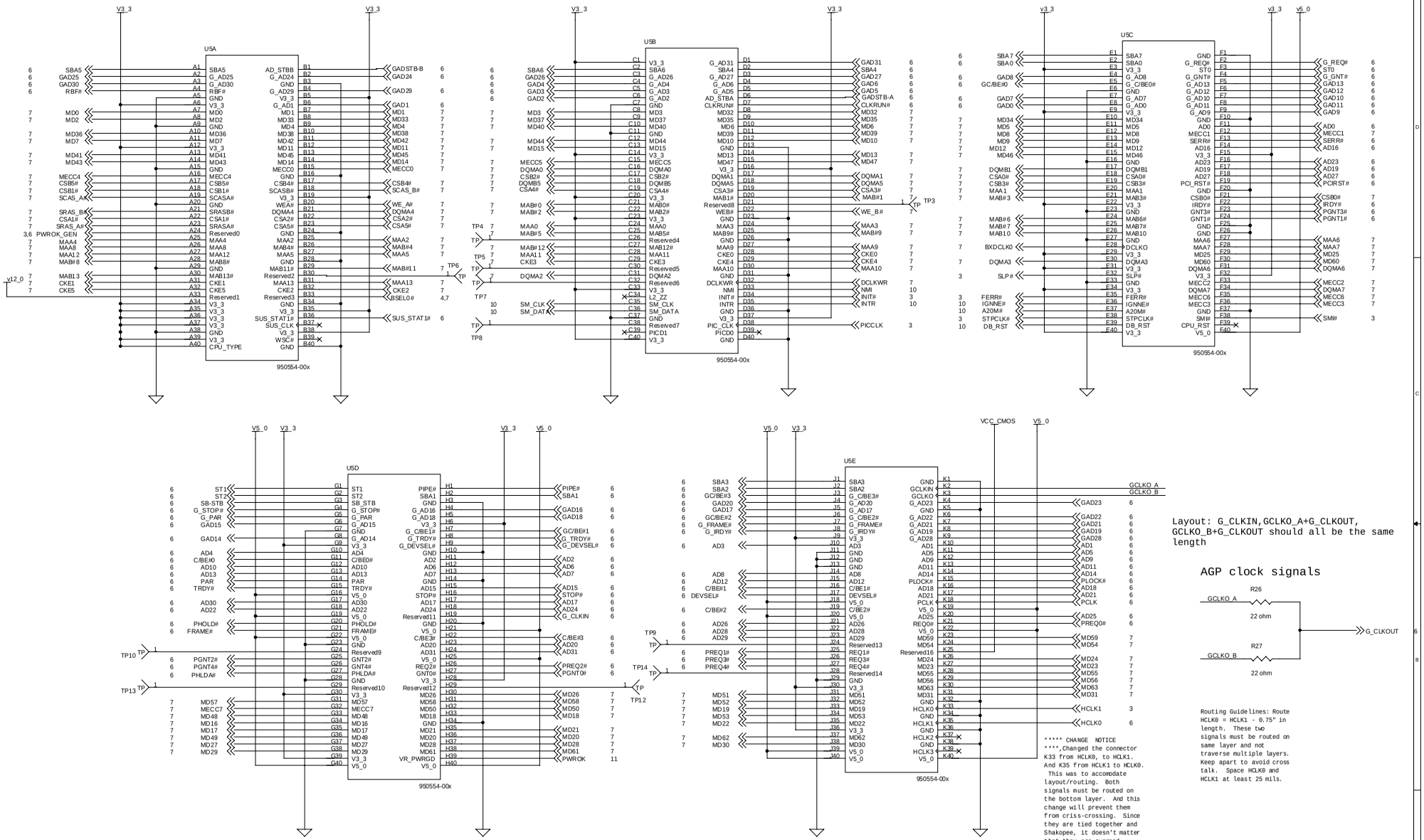
Title: 440BX Memory Interface

Size	Document Number	Rev
C	Intel(R) 440BX Scalable Performance Board	A3

Date: Wednesday, April 26, 2000 Sheet 7 of 12



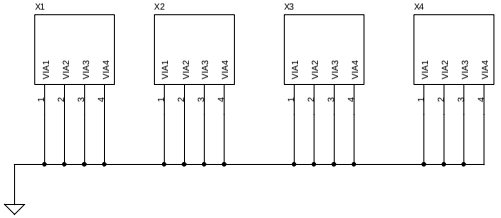
Layout: G_CLKIN,GCLKO_A+G_CLKOUT, GCLKO_B+G_CLKOUT should all be the same length

AGP clock signals

Routing Guidelines: Route HCLK0 = HCLK1 - 0.75" in length. These two signals must be routed on same layer and not traverse multiple layers. Keep apart to avoid cross talk. Space HCLK0 and HCLK1 at least 25 mils.

***** CHANGE NOTICE
****,Changed the connector K33 from HCLK0, to HCLK1. And K35 from HCLK1 to HCLK0. This was to accomodate layout/routing. Both signals must be routed on the bottom layer. And this change will prevent them from criss-crossing. Since they are tied together and Shakopee, it doesn't matter that they are swapped.

Mounting Holes



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Intel Corporation 5000 W. Chandler Blvd Chandler AZ, 85044	
Title: Connectors	
Size: C	Document Number: Intel(R) 440BX Scalable Performance Board — Rev: A3
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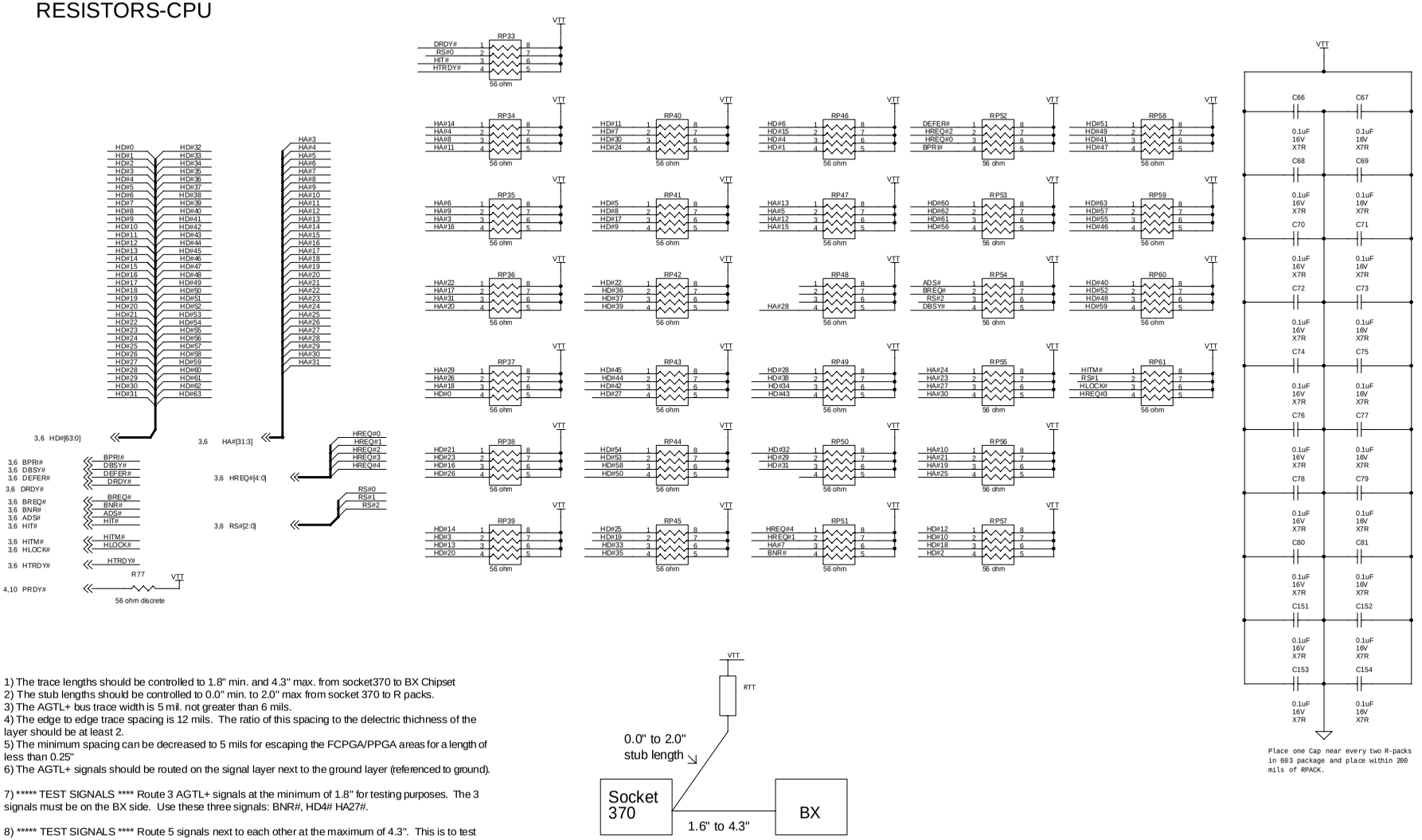
GTL+ TERMINATION RESISTORS-CPU



Place one Cap near every two R-packs in 603 package and place within 200 mils of RPACK.

1) The trace lengths should be controlled to 1.8" min. and 4.3" max. from socket370 to BX Chipset
2) The stub lengths should be controlled to 0.0" min. to 2.0" max from socket 370 to R packs.
3) The AGTL+ bus trace width is 5 mil. not greater than 6 mils.
4) The edge to edge trace spacing is 12 mils. The ratio of this spacing to the delectric thichness of the layer should be at least 2.
5) The minimum spacing can be decreased to 5 mils for escaping the FCPGA/PPGA areas for a length of less than 0.25"
6) The AGTL+ signals should be routed on the signal layer next to the ground layer (referenced to ground).

7) ***** TEST SIGNALS **** Route 3 AGTL+ signals at the minimum of 1.8" for testing purposes. The 3 signals must be on the BX side. Use these three signals: BNR#, HD4# HA27#.

8) ***** TEST SIGNALS **** Route 5 signals next to each other at the maximum of 4.3". This is to test crosstalk. The five signals are: HD29#, HD28#, HD43#, HD37#, HD44#.

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Title	GTL Termination	
Size C	Document Number: Intel(R) 440BX Scalable Performance Board	Rev A3
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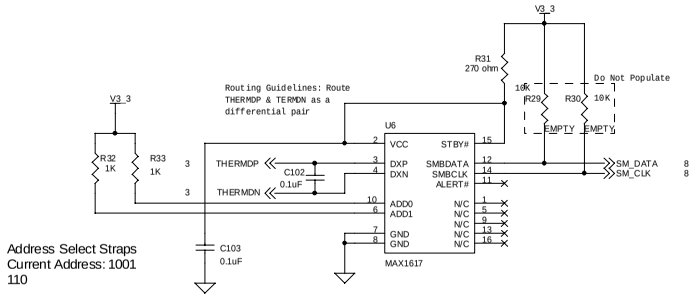
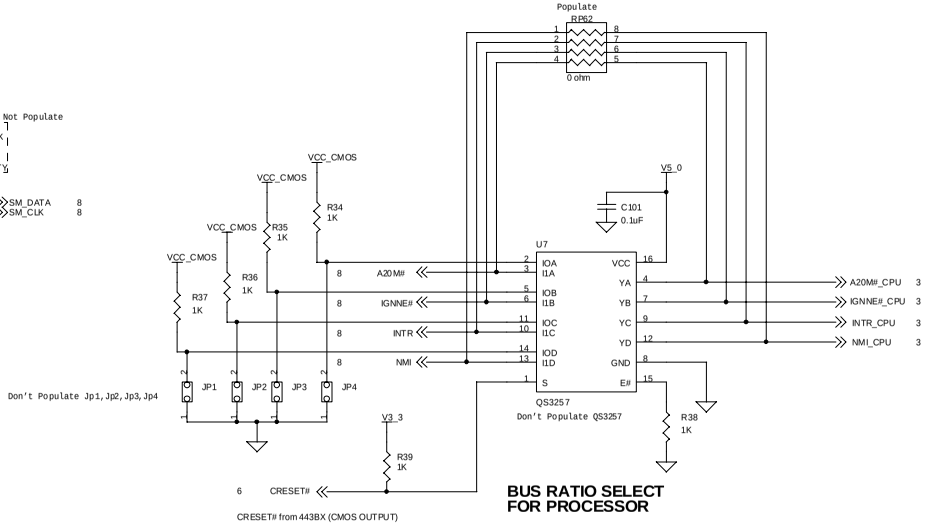
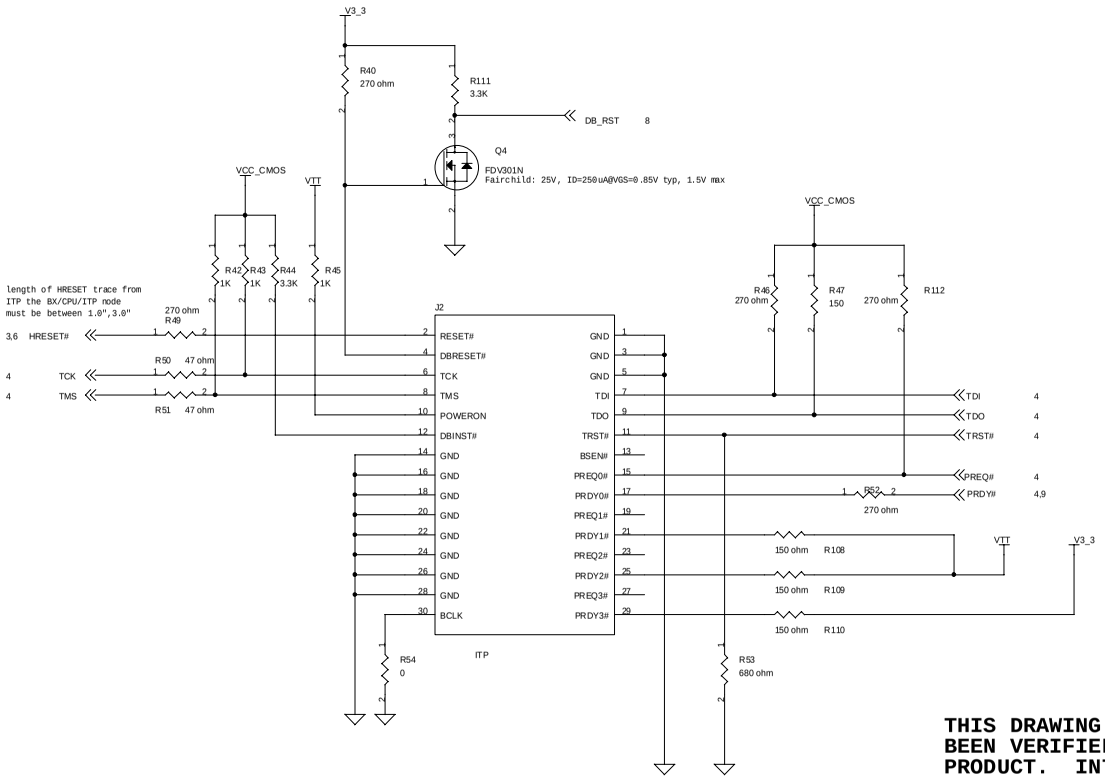
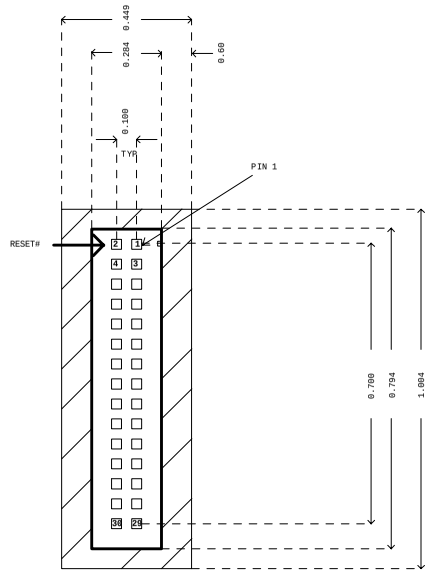


THERMAL SENSOR



BUS RATIO SELECT FOR PROCESSOR





>>> LAYOUT
1.5V connector, AMP 104078-4 Vertical Recepticle, Top View
of ITP connector with component keep-out area.

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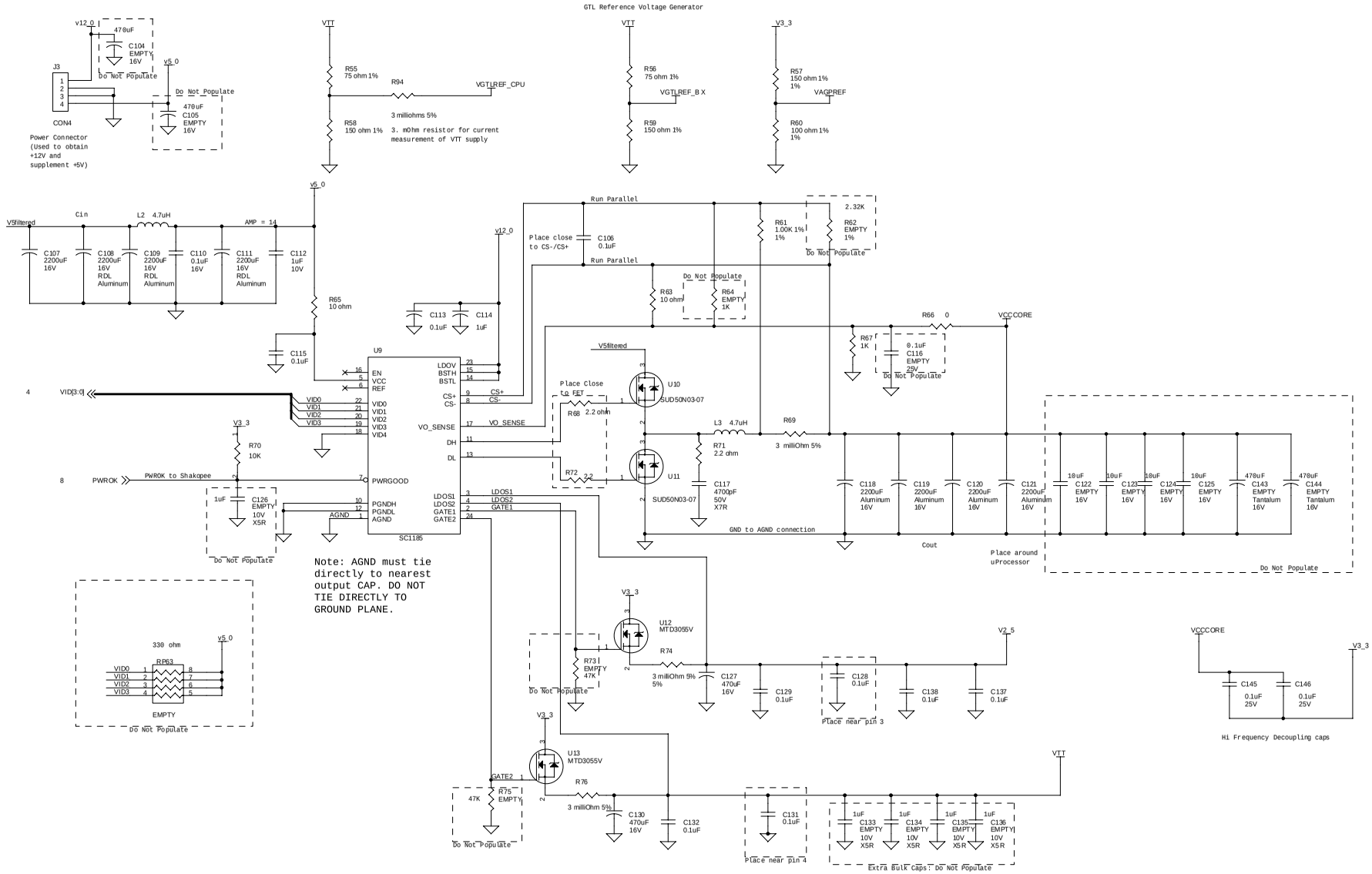
Title: Bus Ratio, Thermal, ITP	
Size: C	Document Number: Intel(R) 440BX Scalable Performance Board — Rev: A3
Date: Wednesday, April 26, 2000	Sheet 10 of 12



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Title	Voltage Regulator	
Size C	Document Number Intel(R) 440BX Scalable Performance Board	Rev A3
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Layout guideline checklist

Board

[ ] An 8 layer board, see right for stack up
[ ] The impedance of all signal layers are to be between 55 and 75 ohms.
[ ] The board impedance should be between 55 and 75 ohms (65 +/- 15%).
[ ] FR-4 material should be used for the board fab.
[ ] The ground plane should not be split.
[ ] If a signal must be routed for a short distance on a power plane, then use the VCC plane.
[ ] Keep vias for decoupling caps as close to the cap pads as possible.

S370_256 Host Interface

[ ] length of HRESET trace from CPU to BX/CPU/ITP node must be between 0.5",1.5"

[ ] HRESET# length of trace to 86 ohm must be between 0.5",1.5"

[ ] Pins AH4,X4 must be daisy chained

[ ] capacitor site on BCLK must be within 0.5" from socket370

[ ] Number pins on top and bottom of board. Silkscreen.

[ ] Place C86,C87,C88 within 1/2 inch of chip

[ ] Add 4 ground pads below BX in inner ring of balls as shown.

S370_256 Other

[ ] PLL1, PLL2 traces < 0.1 ohm route

S370_256 Power

[ ] VCC_CORE decoupling -- 4.7uF decoupling capacitors must be place within the socket cavity and mounted directly on the primary side of the motherboard. The traces must be as short and wide as possible. Use 1206 package.

[ ] VREF decoupling -- Intel recommends four or more 0.1uF caps in a 0603 package placed near VREF pins within 500 mils.
[ ] VREF decoupling --Make MREF short/wide 24 mils minimum

[ ] For VTT decoupling -- place one Cap near every two R-packs in 603 package and place within 200 mils of RPACK.

440BX Host Interface

[ ] length of HRESET trace from 443BX to BX/CPU/ITP node must be between 0.5",1.5"

[ ] length of trace to 86 ohm must be between 0.5",1.5"

440BX Memory Interface

[ ] Place DCLKWR cap as close to BX as possible

Bus Ratio, Thermal, ITP

[ ] length of HRESET trace from ITP the BX/CPU/ITP node must be between 1.0",3.0"

[ ] Route THERMDP & TERMDN as a differential pair

[ ] Make sure you route the ITP connector right. See page10 for the footprint.

8 Layer Board with the following stackup:

Signal (GTL +VTT)
GND
Signal - GTL
Signal
3.3 (most of the board) / GND (Under the S370 + BX)
Signal - GTL
GND
Signal - GTL - VccCore

Use the same stackup thicknesses as baseboard.

Trace Impedance:55 - 75Ohms. (shoot for 65, lower is better than higher!)
Top/bottom layer should be ½ oz cu, inner layers 1 oz cu

Connector

[ ] HCLK0 = HCLK1 - 0.75" in length. IMPORTANT route HCLK0 and HCLK1 on same layer, don't traverse multiple layers. Place on bottom layer. But keep two signals apart by a spacing of 25 mils. to avoid cross talk.

[ ] G_CLKIN,GCLKO_A+G_CLKOUT, GCLKO_B+G_CLKOUT should all be the same length

GTL Termination

[ ] The trace lengths should be controlled to 1.8" min. and 4.3" max. from socket370 to BX Chipset

[ ] The stub lengths should be controlled to 0.0" min. to 2.0" max from socket 370 to R packs.

[ ] The AGTL+ bus trace width is 5 mil. not greater than 6 mils.

[ ] The edge to edge trace spacing is 12 mils. The ratio of this spacing to the delectric thichness of the layer should be at least 2.

[ ] The minimum spacing can be decreased to 5 mils for escaping the FCPGA/PPGA areas for a length of less than 0.25"

[ ] The AGTL+ signals should be routed on the signal layer next to the ground layer (referenced to ground).

[ ] ***** TEST SIGNALS **** Route 3 AGTL+ signals at the minimum of 1.8" for testing purposes. The 3 signals must be on the BX side. Use these three signals: BNR#, HD4# HA27#.

[ ] ***** TEST SIGNALS **** Route 5 signals next to each other at the maximum of 4.3". This is to test crosstalk. The five signals are: HD29#, HD28#, HD43#, HD37#, HD44#.

Silkscreen

[ ] Flexible Intel(R) 440BX AGPset/PGA370 Processor adapter

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