INTEL® 440MX SCALABLE LOW POWER BOARD

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REVISION HISTORY

A 08-06-01 Initial Revision A Schematics

B 09-20-01 Changes to the following:
Changed TEST# pullup on MX to 3VSB
Super I/O: added circuitry to generate AEN during DMA cycles (needed on SMSC SIO)

NOTE: ALL RESISTORS +/- 1%, ALL CAPACITORS +/- 20% UNLESS OTHERWISE NOTED

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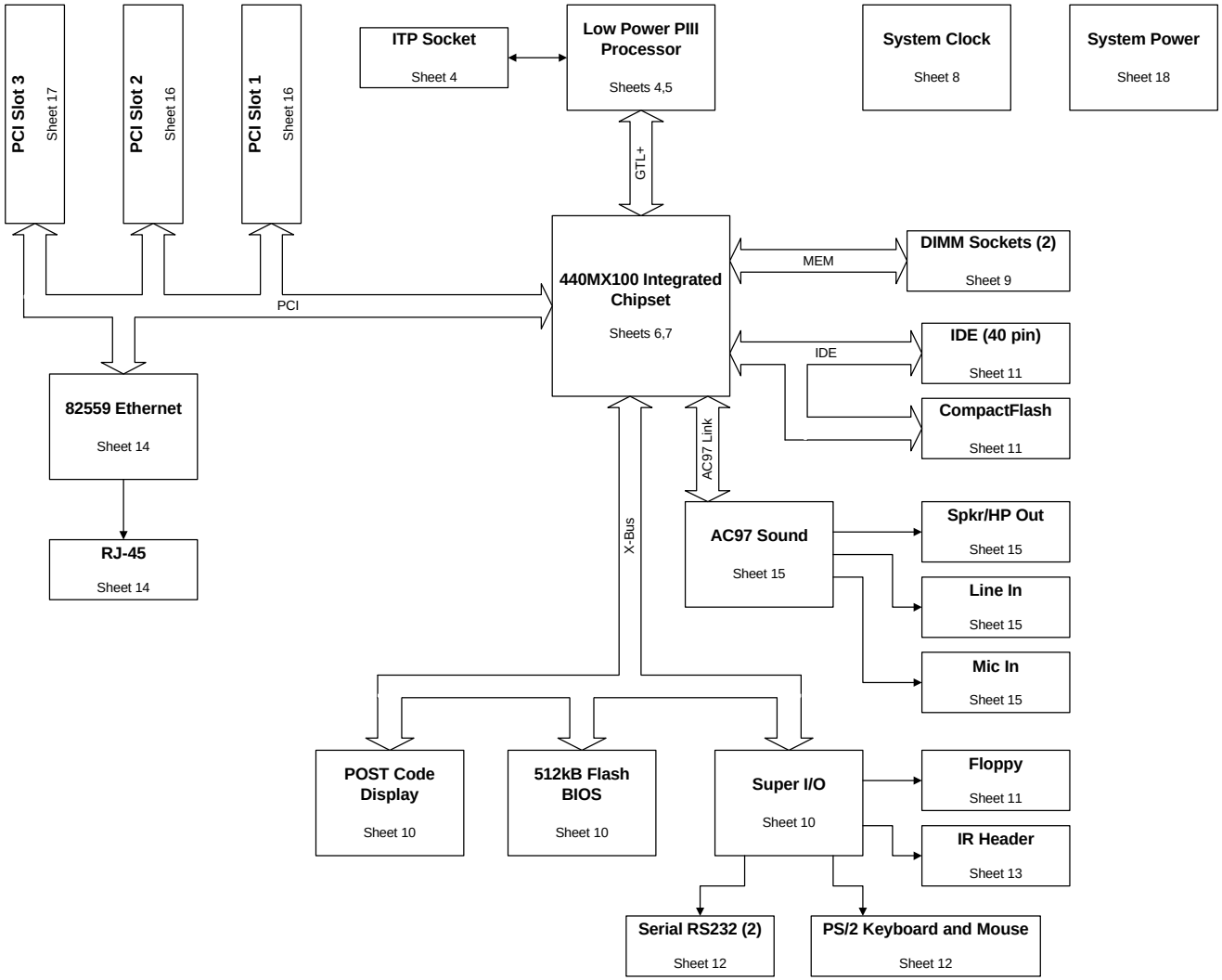
DATE: 05/30/01	B	DRAWING: 440MX SCALABLE LOW POWER BOARD	SHEET: 1 OF 19

INTEL® 440MX SCALABLE LOW POWER BOARD

BLOCK DIAGRAM



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TITLE: BLOCK DIAGRAM
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B
DRAWING: 440MX SCALABLE LOW POWER BOARD
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INTEL® 440MX SCALABLE LOW POWER BOARD
ROUTING GUIDELINES

General Board Design Requirements

- Nominal trace impedance must be 65 ohms +/- 10%.
- Vias for decoupling capacitors must be kept as close as possible to capacitor pad.
- Finished board thickness is .062” +/- .007”.
- Outer layers must be ½ oz copper before plating, inner layers must be 1 oz copper.
- Series termination resistors must be kept as close to the driving pins as possible
- Signals with multiple endpoints should be daisy-chained, signal should not split into branches.
- GND plane must not be split
- Bypass capacitors on signals going to I/O connectors should be located as close to the connector as possible
- Check specific schematic pages for additional routing information

CPU Routing Requirements

- GTL+ signals between the CPU and 440MX should be between 1.9” and 4.3” long.
- Route GTL+ signals on layer adjacent to GND, and do not change layers.
- Signals between the CPU and 440MX must not differ in length by more than 1”.
- Spacing between adjacent signals should be as large as possible > 10 mils except for short distances for fanout. Total distance for fanout allowance is 250 mil.
- Route VREF_GTL signal as a minimum 25 mil trace, and keep 25 mil from other traces.
- Route CPU_PLL[2:1] using 25 mil trace, minimize loop area, and keep 25 mil from other traces.

Clock Specific Routing Requirements

- Series damping resistors must be less than 0.5” from clock IC.
- Clock traces should be routed on inner layers, with layer transitions at an absolute minimum.
- Spacing between clock trace and any other trace should be > 12 mils, serpentine spacing > 18 mils.
- MX_HCLK must be between 3.25” and 5.85” long, and CPU_HCLK must be 877 mils +/- 1 mil longer than MX_HCLK.
- ITP_HCLK should be the same length as CPU_HCLK.
- PCI clocks to the slots should be the same length, +/- 2”, but less than 12.5” long.
- Onboard PCI device clocks same as above, but 2.5” longer than PCI clocks to slots.
- MEM_CLKs to the DIMMs should be the same length, +/- 0.1”, and between 1.0” and 4” long.
- CLK_DCLKOUT should be the same length as the MEM_CLKs, +/- 0.1”.
- CLK_DCLKIN should be 2.5” longer than CLK_DCLKOUT, +/- 0.1”.

Switching Power Supply Routing Requirements

- Keep all unrelated signals and power planes away from switching regulator and related circuitry.
- Power input and output traces should be routed with minimal length while maximizing width.

Memory Bus Routing Requirements

- Length of MEM Bus lines should be between 1” and 4”.
- Spacing between other MEM Bus traces should be 10mil, spacing should be 5 mil for no more than 0.5”.
- Spacing to non-MEM Bus traces should be atleast 20 mil.
- MEM Bus traces should not transition between layers, except to get to the topside for the chipset.

PCI Bus Routing Requirements

- PCI signals should be similar length, routed in a daisy-chain fashion together to each component, with the 440MX as the last component.
- Total length of PCI signals must be less than 25”.

NOTE: ALL RESISTORS +/- 1%, ALL CAPACITORS +/- 20% UNLESS OTHERWISE NOTED

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REV: B
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DRAWING: 440MX SCALABLE LOW POWER BOARD
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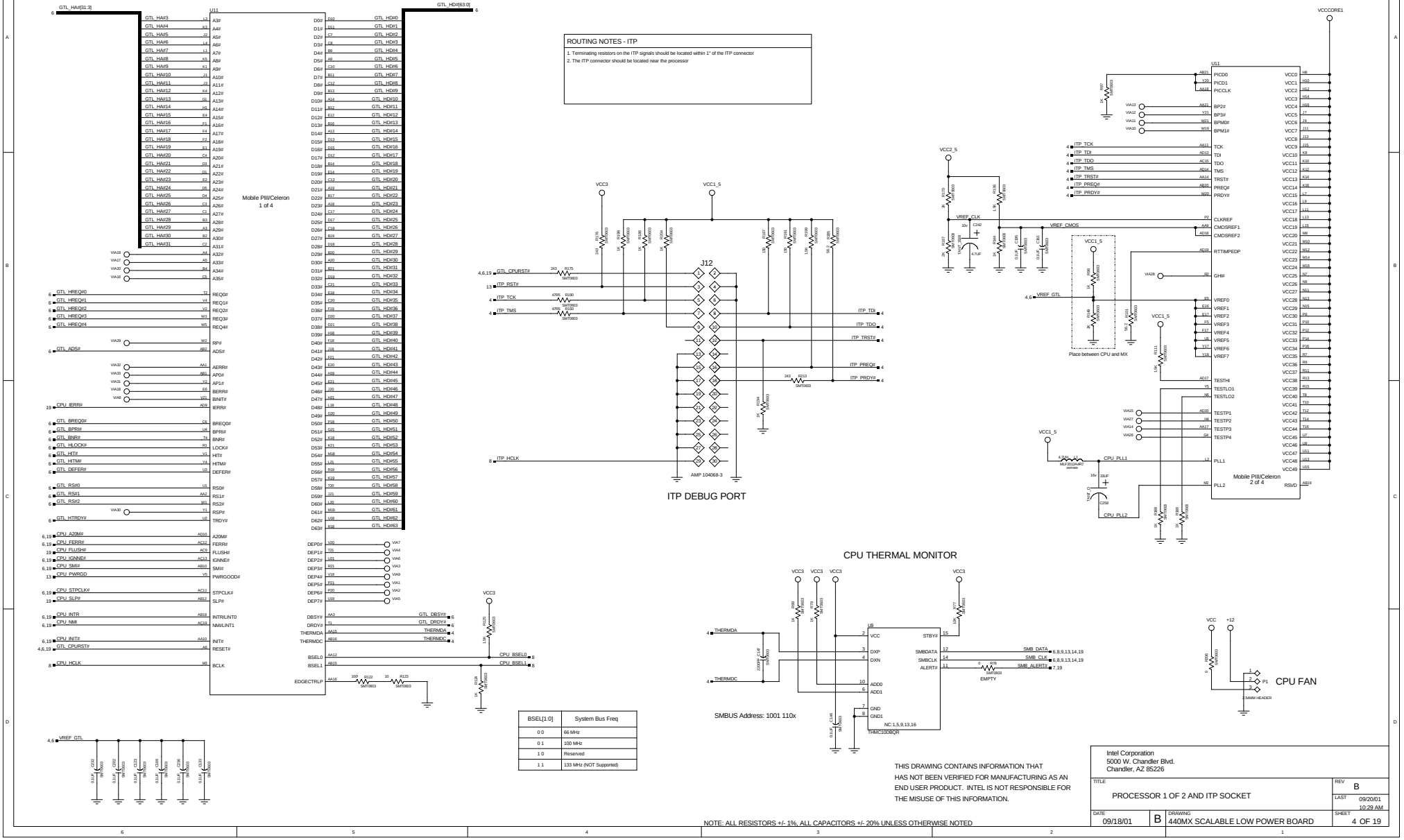
ROUTING NOTES - ITP
1. Terminating resistors on the ITP signals should be located within 1" of the ITP connector
2. The ITP connector should be located near the processor
Mobile PIII/Celeron
1 of 4
Mobile PIII/Celeron
2 of 4
ITP DEBUG PORT
AMP 104068-3
CPU THERMAL MONITOR
SMBUS Address: 1001 110x
CPU FAN
Place between CPU and MX
EMPTY
NC:1,5,9,13,16
THMC10DBQR
BSEL[1:0] | System Bus Freq
0 0 | 66 MHz
0 1 | 100 MHz
1 0 | Reserved
1 1 | 133 MHz (NOT Supported)
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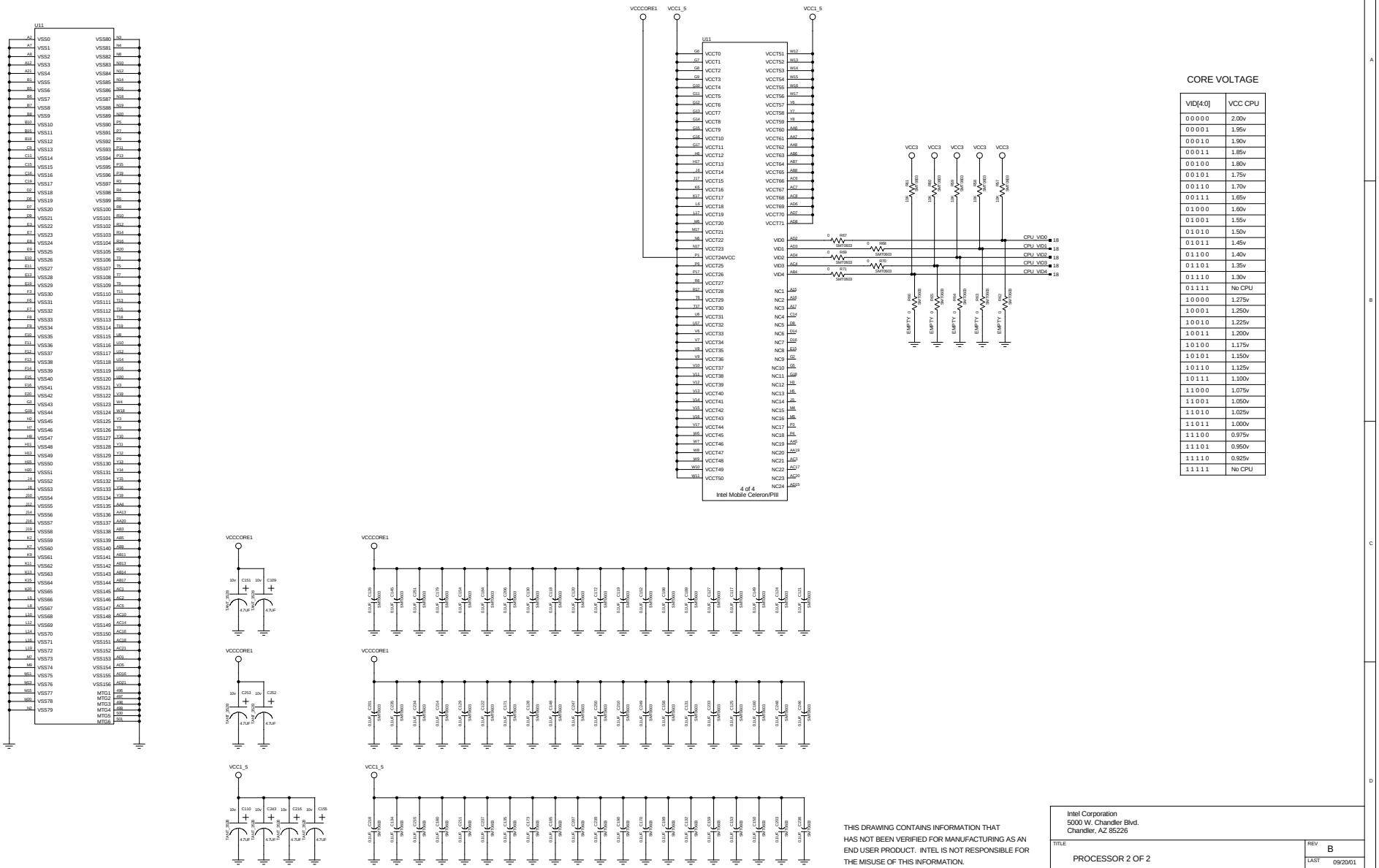
TITLE
PROCESSOR 1 OF 2 AND ITP SOCKET
REV B
LAST 09/20/01 10:29 AM
DATE 09/18/01
B
DRAWING 440MX SCALABLE LOW POWER BOARD
SHEET 4 OF 19



CORE VOLTAGE

VID[4:0]	VCC CPU
0 0 0 0 0	2.00v
0 0 0 0 1	1.95v
0 0 0 1 0	1.90v
0 0 0 1 1	1.85v
0 0 1 0 0	1.80v
0 0 1 0 1	1.75v
0 0 1 1 0	1.70v
0 0 1 1 1	1.65v
0 1 0 0 0	1.60v
0 1 0 0 1	1.55v
0 1 0 1 0	1.50v
0 1 0 1 1	1.45v
0 1 1 0 0	1.40v
0 1 1 0 1	1.35v
0 1 1 1 0	1.30v
0 1 1 1 1	No CPU
1 0 0 0 0	1.275v
1 0 0 0 1	1.250v
1 0 0 1 0	1.225v
1 0 0 1 1	1.200v
1 0 1 0 0	1.175v
1 0 1 0 1	1.150v
1 0 1 1 0	1.125v
1 0 1 1 1	1.100v
1 1 0 0 0	1.075v
1 1 0 0 1	1.050v
1 1 0 1 0	1.025v
1 1 0 1 1	1.000v
1 1 1 0 0	0.975v
1 1 1 0 1	0.950v
1 1 1 1 0	0.925v
1 1 1 1 1	No CPU

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TITLE: PROCESSOR 2 OF 2		REV: B	
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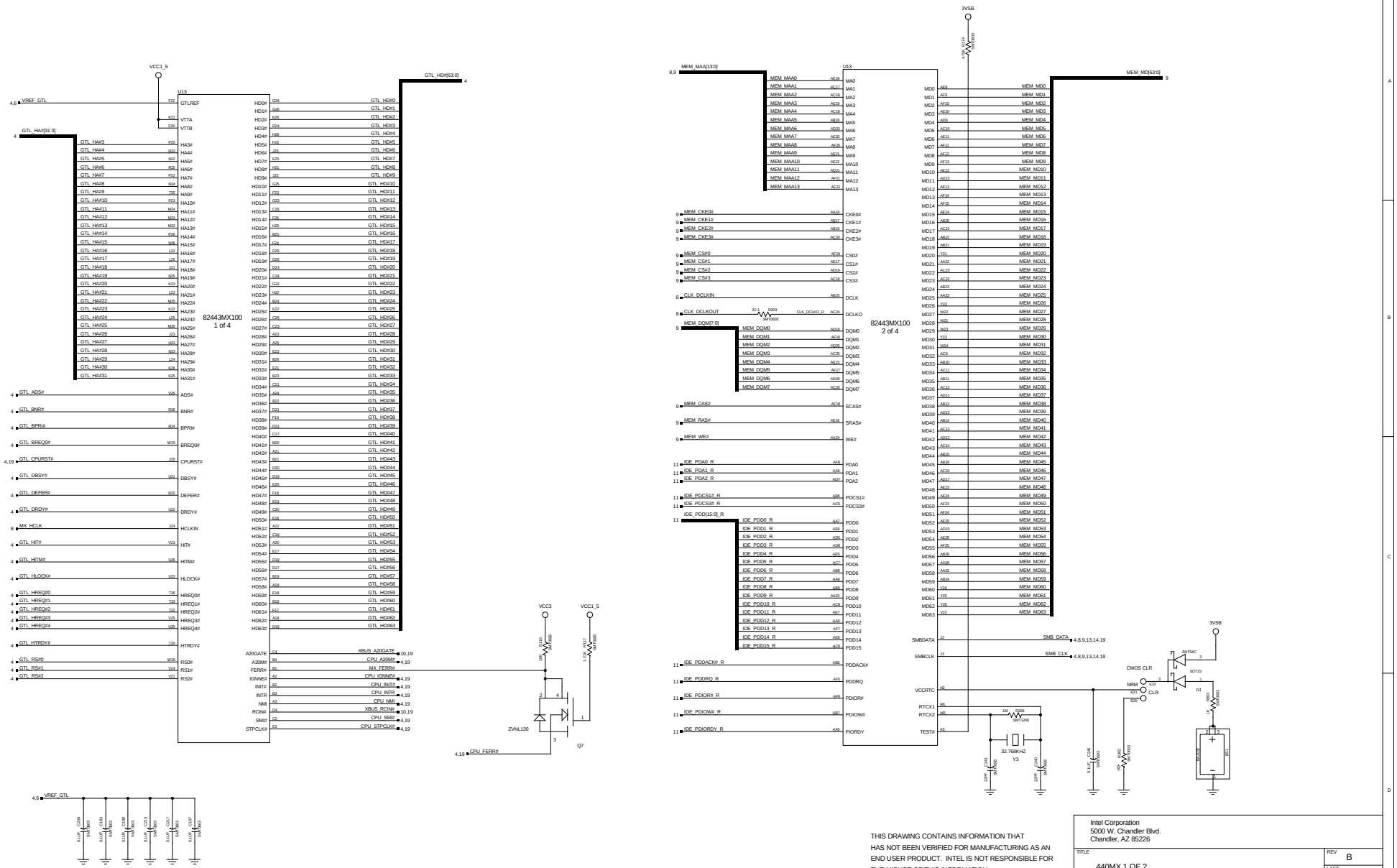

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TITLE	440MX 1 OF 2	REV	B
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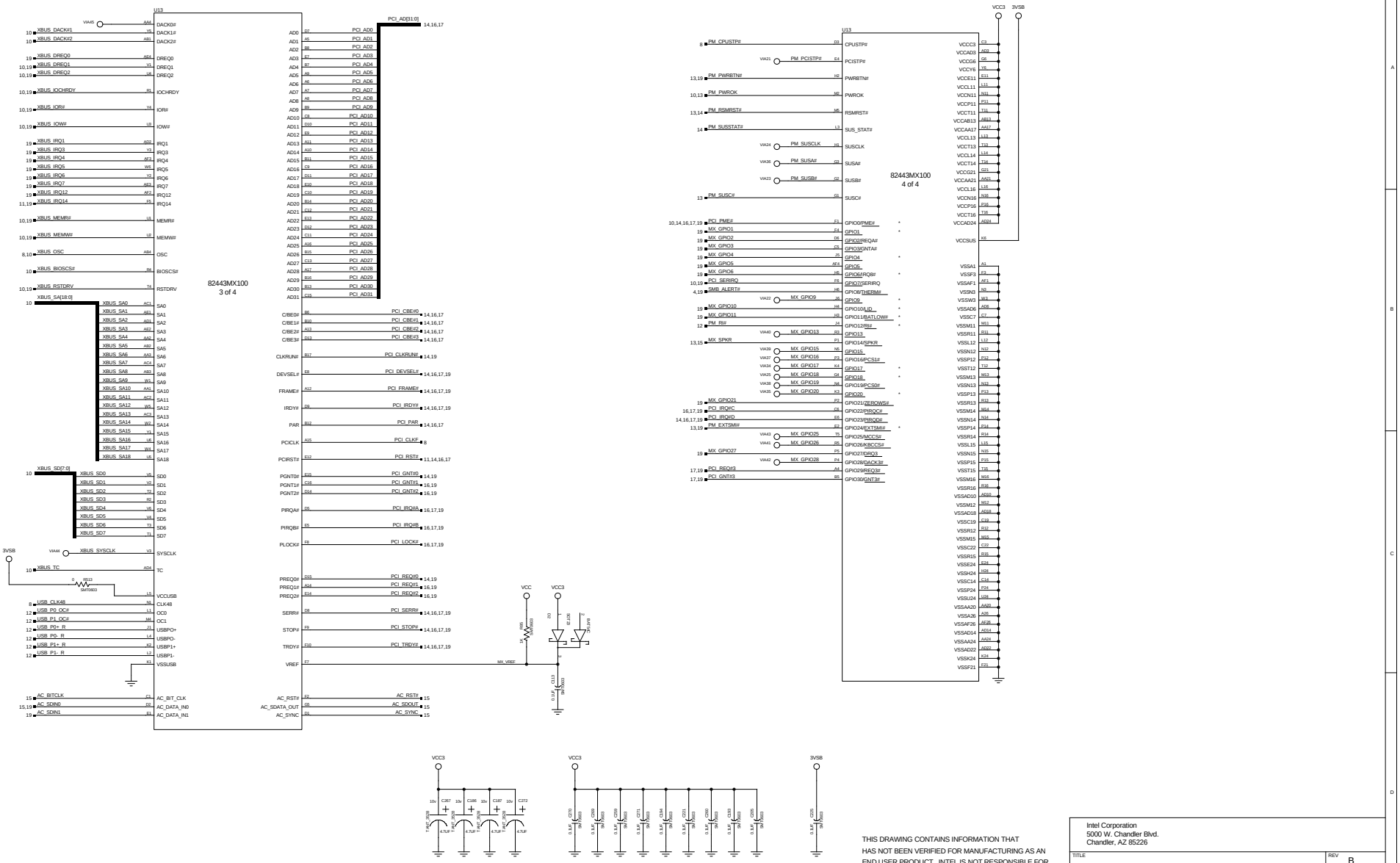
U13
82443MX100
3 of 4
82443MX100
4 of 4
PCI_AD[31:0]
XBUS_SD[7:0]
XBUS_SA[18:0]
VCC3
3VSB
VCC
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TITLE
440MX 2 OF 2
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B
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440MX SCALABLE LOW POWER BOARD
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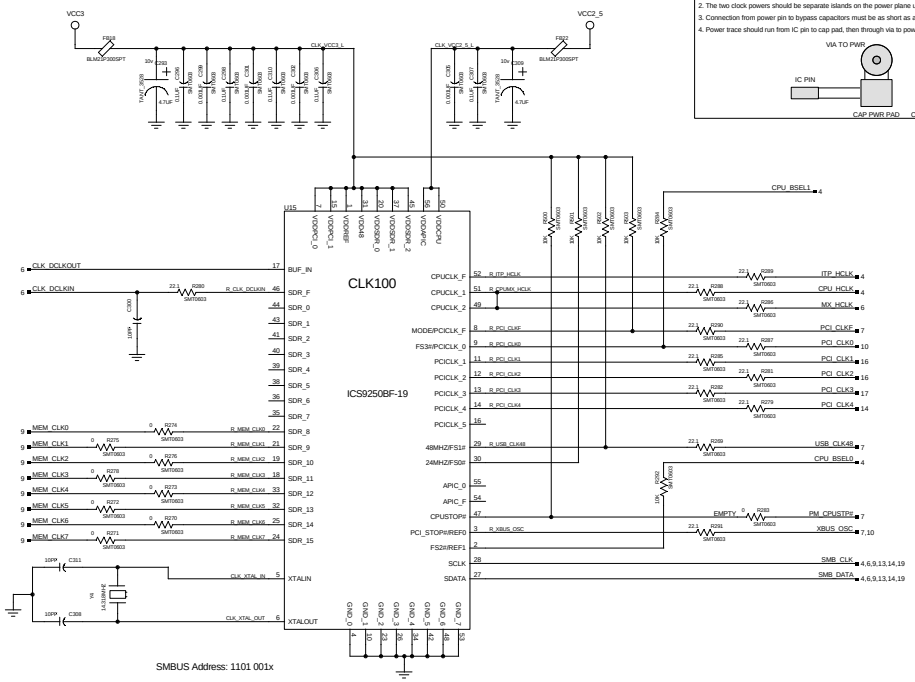


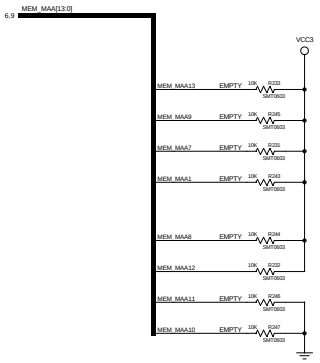
ROUTING NOTES - SYSTEM CLOCK

1. Place a copper area under the clock IC body on the component side, and connect it to GND through several vias
2. The two clock powers should be separate islands on the power plane under the corresponding pins of the IC
3. Connection from power pin to bypass capacitors must be as short as and wide as possible.
4. Power trace should run from IC pin to cap pad, then through via to power island as shown

JUMPER DEFINITION TABLE

JUMPER	FUNCTION	JUMPER INSTALLATION OPTIONS	
CMOS CLR	Clear the RTC CMOS	CLR = Clear	**NRM = Normal**
BIOS UNLOCK	Install to Reprogram the BIOS	**Installed = Unlocked**	Not Installed = Locked
CF MASTER	Install to Set the CompactFlash as Master	Installed = CF Master	Not Installed = CF Slave
ENET ENA/DIS	Enable or Disable the Ethernet Controller	**ENA = Enabled**	DIS = Disabled

Bold = Indicates Default Jumper Location



STRAPPING OPTIONS

SIGNAL	FUNCTION	PULLDOWN	PULLUP	440MX DEFAULT
MA13	Processor Core/Bus Ratio Select (not used)	**NMI Low**	NMI High	PULLDOWN
MA9	Processor Core/Bus Ratio Select (not used)	**INTR Low**	INTR High	PULLDOWN
MA7	Processor Core/Bus Ratio Select (not used)	**IGNNE# Low**	IGNNE# High	PULLDOWN
MA1	Processor Core/Bus Ratio Select (not used)	**A20M# Low**	A20M# High	PULLDOWN
MA12	Host Frequency Select	66MHz	**100MHz**	PULLDOWN
MA11	In-Order Queue Depth Enable	One	**Max**	PULLUP
MA10	Quick Start Select	Disable	**Enable**	PULLUP
MA8	Reserved	**Default**	Reserved	PULLDOWN

Board Stuffing Default

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TITLE	SYSTEM CLOCK & STRAPPING OPTIONS	REV	B
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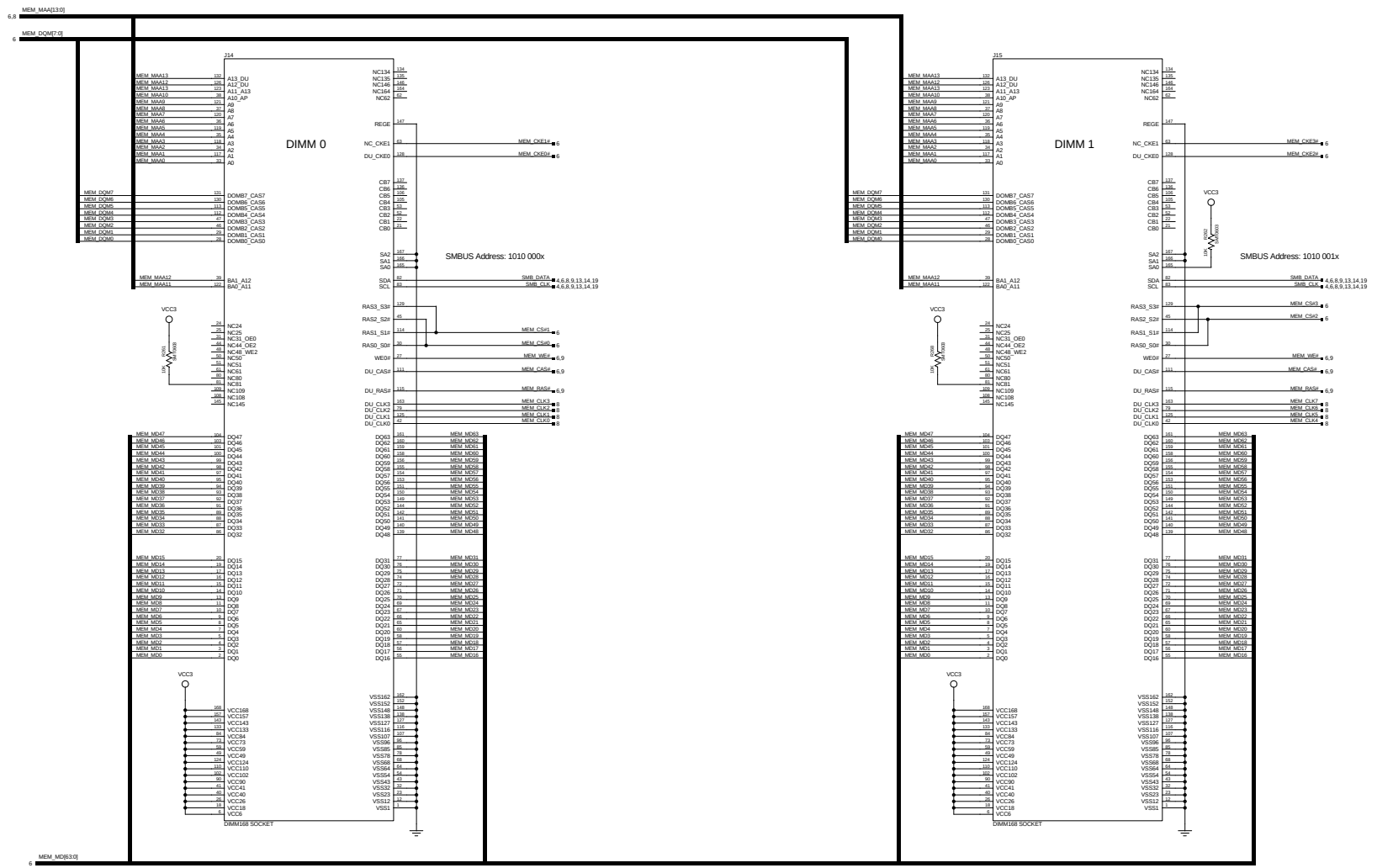

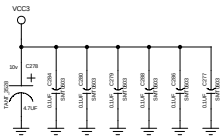

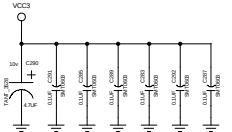

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TITLE: DIMM SOCKETS		REV: B	
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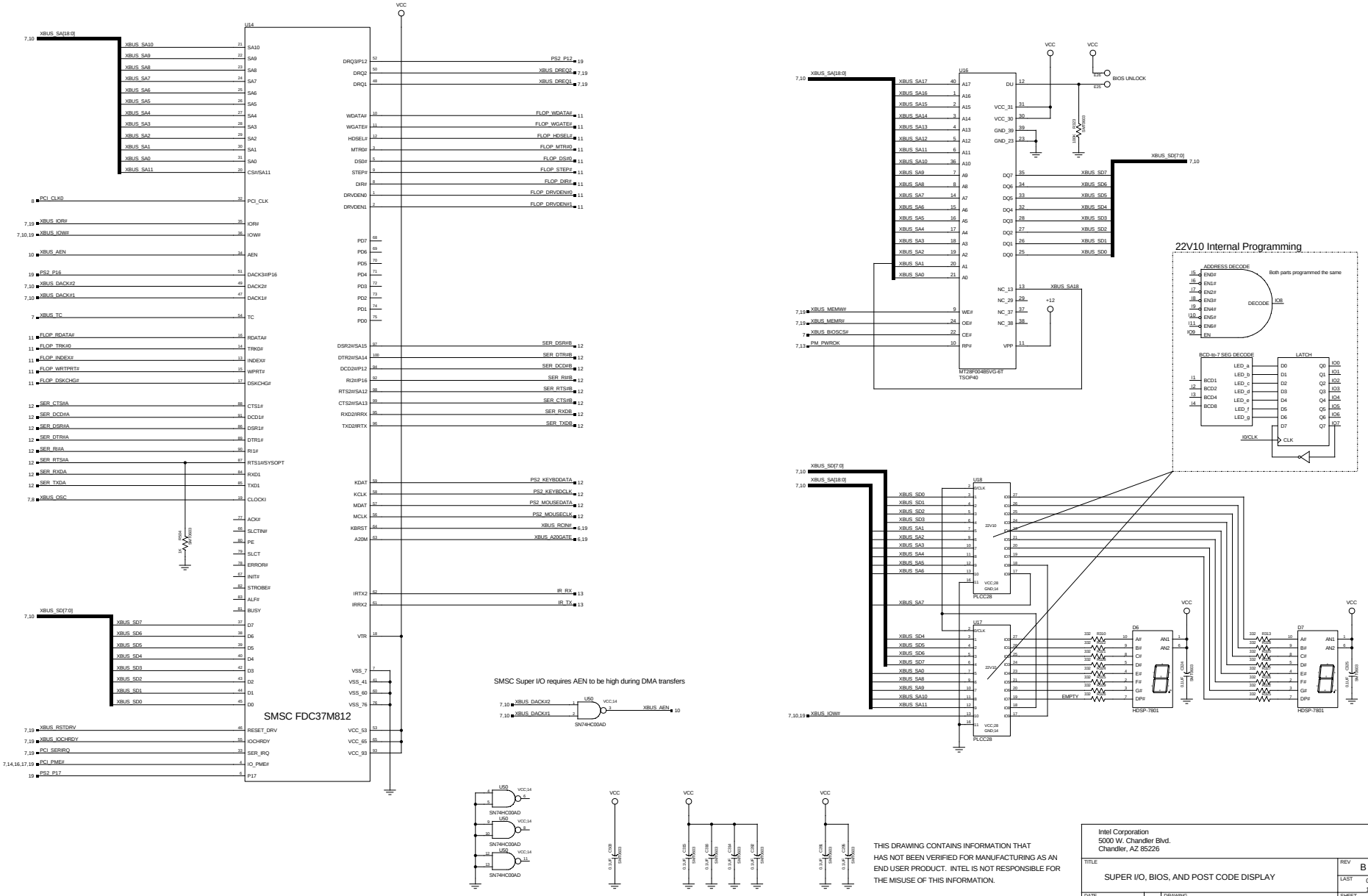
SMSC FDC37M812
SMSC Super I/O requires AEN to be high during DMA transfers
22V10 Internal Programming
BIOS UNLOCK
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SUPER I/O, BIOS, AND POST CODE DISPLAY
REV B
LAST 09/20/01 10:29 AM
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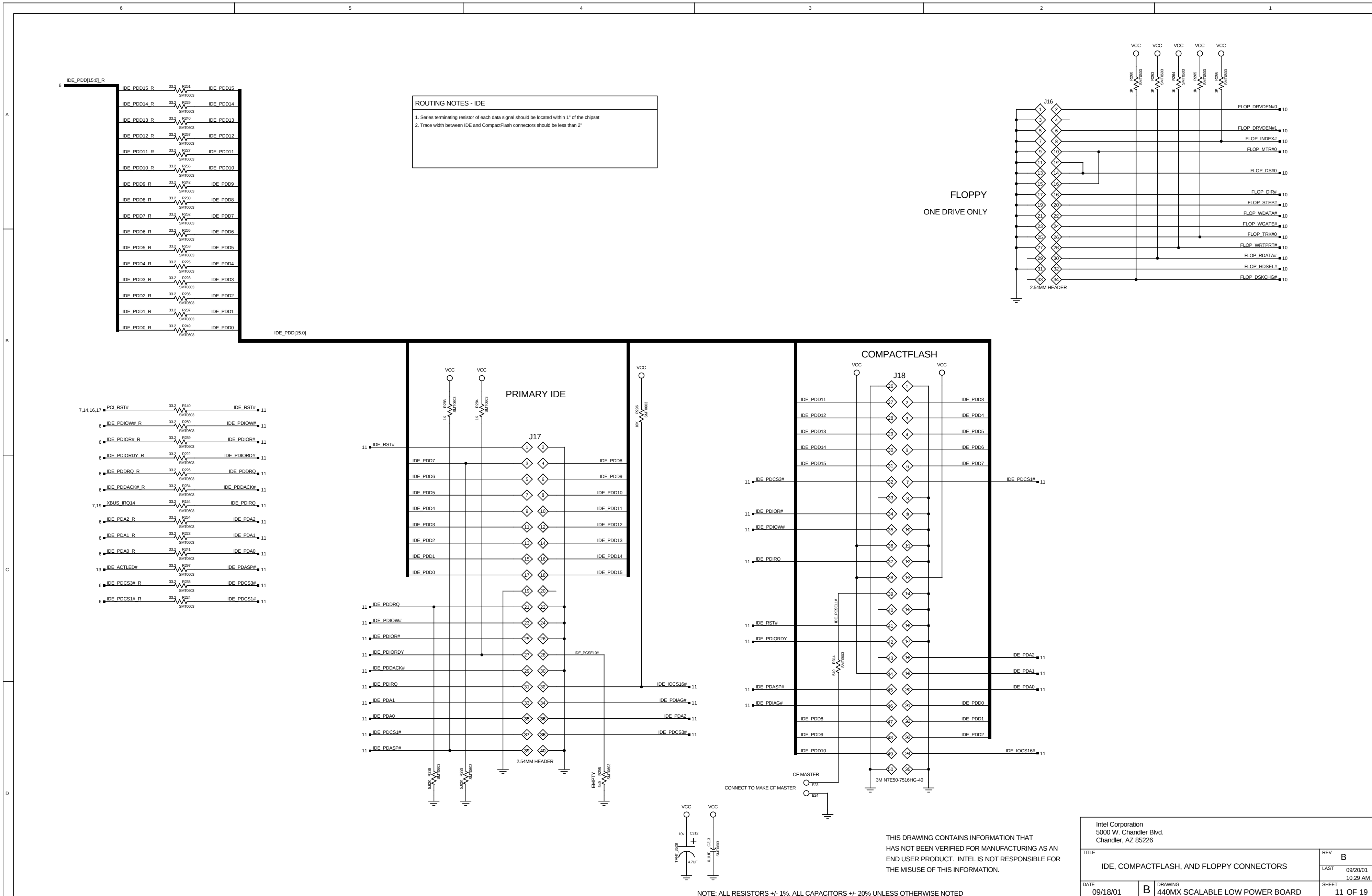
B
DRAWING 440MX SCALABLE LOW POWER BOARD
SHEET 10 OF 19


IDE_PDD[15:0]_R
IDE_PDD[15:0]
PRIMARY IDE
J17
2.54MM HEADER
COMPACTFLASH
J18
3M N7E50-7516HG-40
FLOPPY
ONE DRIVE ONLY
J16
2.54MM HEADER
CF MASTER
CONNECT TO MAKE CF MASTER
VCC
PCI_RST#
IDE_RST#
IDE_PDIOW#_R
IDE_PDIOW#
IDE_PDIOR#_R
IDE_PDIOR#
IDE_PDIORDY_R
IDE_PDIORDY
IDE_PDDRQ_R
IDE_PDDRQ
IDE_PDDACK#_R
IDE_PDDACK#
XBUS_IRQ14
IDE_PDIRQ
IDE_PDA2_R
IDE_PDA2
IDE_PDA1_R
IDE_PDA1
IDE_PDA0_R
IDE_PDA0
IDE_ACTLED#
IDE_PDASP#
IDE_PDCS3#_R
IDE_PDCS3#
IDE_PDCS1#_R
IDE_PDCS1#
IDE_PCSEL0#
IDE_IOCS16#
IDE_PDIAG#
FLOP_DRVDEN#0
FLOP_DRVDEN#1
FLOP_INDEX#
FLOP_MTR#0
FLOP_DS#0
FLOP_DIR#
FLOP_STEP#
FLOP_WDATA#
FLOP_WGATE#
FLOP_TRK#0
FLOP_WRTPRT#
FLOP_RDATA#
FLOP_HDSEL#
FLOP_DSKCHG#
EMPTY

ROUTING NOTES - IDE

1. Series terminating resistor of each data signal should be located within 1" of the chipset
2. Trace width between IDE and CompactFlash connectors should be less than 2"

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TITLE	IDE, COMPACTFLASH, AND FLOPPY CONNECTORS	REV	B
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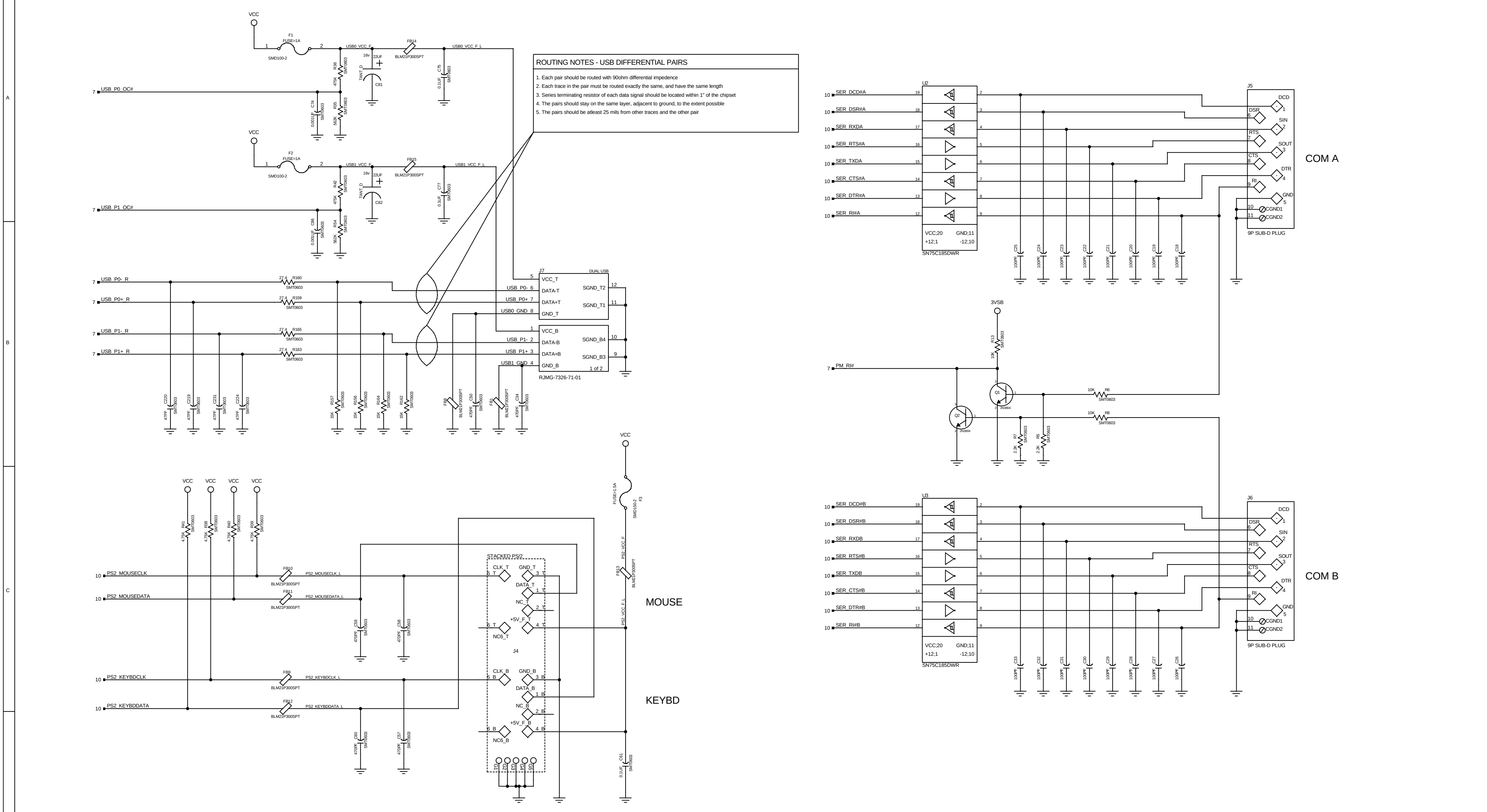
VCC
F1
FUSE=1A
SM0100-2
USB0_VCC_F
FB14
BLM21P300SPT
USB0_VCC_F_L
USB_P0_OC#
F2
FUSE=1A
USB1_VCC_F
FB15
USB1_VCC_F_L
USB_P1_OC#
USB_P0-_R
USB_P0+_R
USB_P1-_R
USB_P1+_R
J7
DUAL USB
VCC_T
DATA-T
DATA+T
GND_T
SGND_T2
SGND_T1
VCC_B
DATA-B
DATA+B
GND_B
SGND_B4
SGND_B3
1 of 2
RJMG-7326-71-01
USB_P0-
USB_P0+
USB0_GND
USB_P1-
USB_P1+
USB1_GND
PS2_MOUSECLK
PS2_MOUSEDATA
PS2_KEYBDCLK
PS2_KEYBDDATA
STACKED PS/2
J4
MOUSE
KEYBD
SER_DCD#A
SER_DSR#A
SER_RXDA
SER_RTS#A
SER_TXDA
SER_CTS#A
SER_DTR#A
SER_RI#A
U2
SN75C185DWR
J5
9P SUB-D PLUG
COM A
3VSB
PM_RI#
Q1
Q2
SER_DCD#B
SER_DSR#B
SER_RXDB
SER_RTS#B
SER_TXDB
SER_CTS#B
SER_DTR#B
SER_RI#B
U3
SN75C185DWR
J6
9P SUB-D PLUG
COM B
VCC
+12
-12

ROUTING NOTES - USB DIFFERENTIAL PAIRS

1. Each pair should be routed with 90ohm differential impedence
2. Each trace in the pair must be routed exactly the same, and have the same length
3. Series terminating resistor of each data signal should be located within 1" of the chipset
4. The pairs should stay on the same layer, adjacent to ground, to the extent possible
5. The pairs should be atleast 25 mils from other traces and the other pair

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TITLE	SERIAL, KEYBOARD, MOUSE, USB CONNECTORS		REV B
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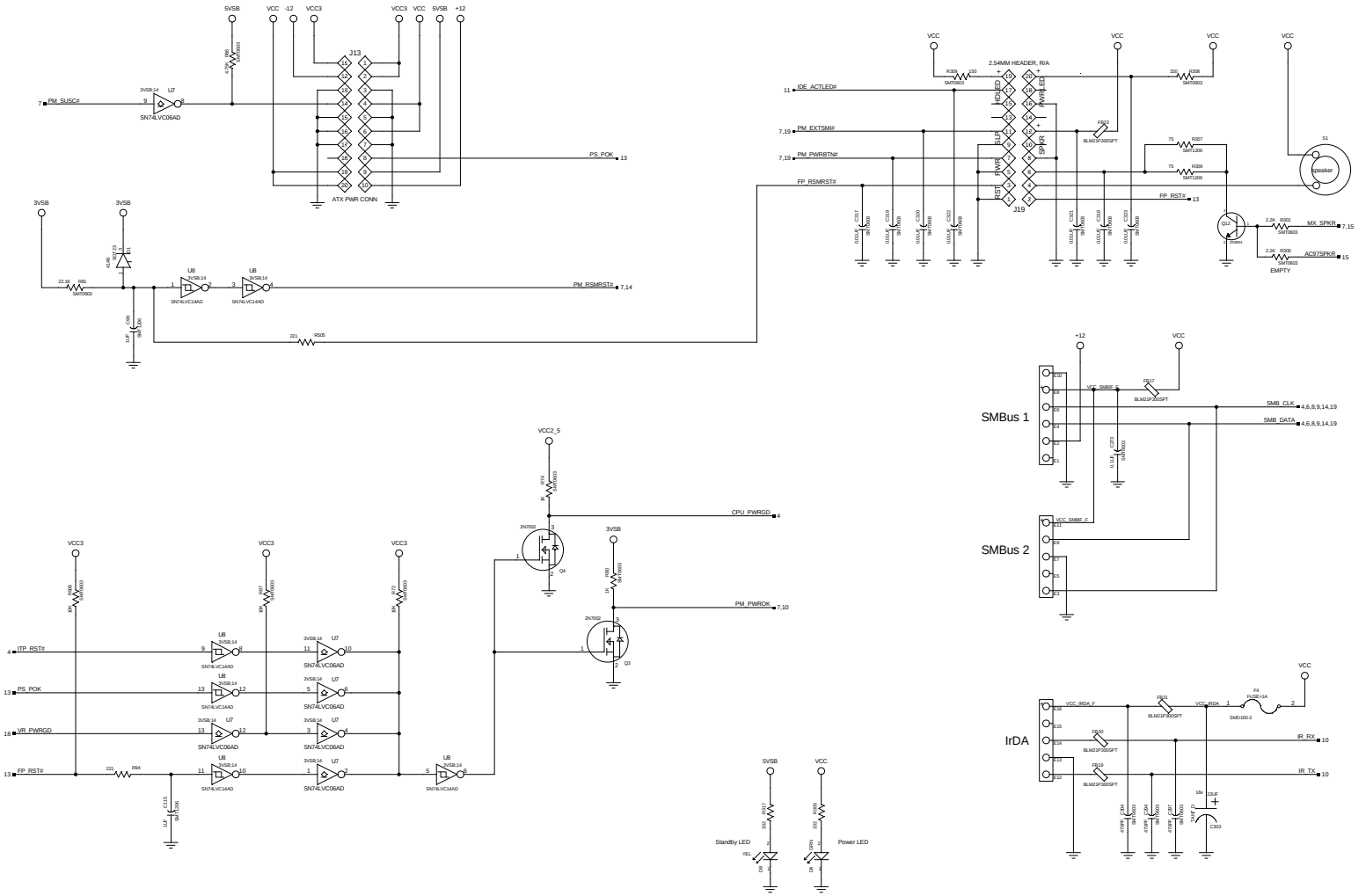

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TITLE: POWER AND FRONT PANEL CONNECTORS		REV: B	
		LAST: 09/20/01 10:29 AM	
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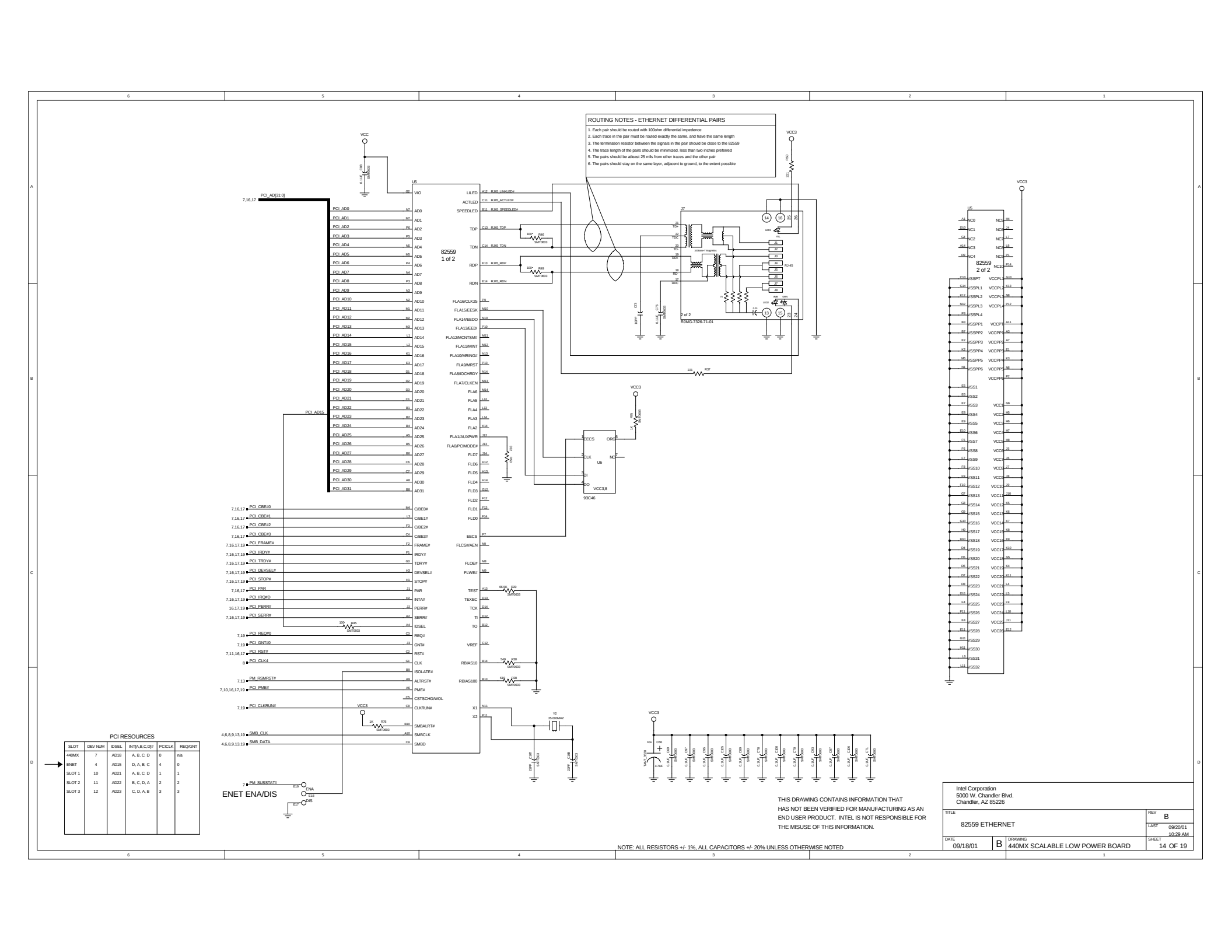
ROUTING NOTES - ETHERNET DIFFERENTIAL PAIRS
1. Each pair should be routed with 100ohm differential impedence
2. Each trace in the pair must be routed exactly the same, and have the same length
3. The termination resistor between the signals in the pair should be close to the 82559
4. The trace length of the pairs should be minimized, less than two inches preferred
5. The pairs should be atleast 25 mils from other traces and the other pair
6. The pairs should stay on the same layer, adjacent to ground, to the extent possible
82559
1 of 2
82559
2 of 2
RJMG-7326-71-01
93C46
ENET ENA/DIS
PCI RESOURCES
SLOT | DEV NUM | IDSEL | INT[A,B,C,D]# | PCICLK | REQ/GNT
440MX | 7 | AD18 | A, B, C, D | 0 | n/a
ENET | 4 | AD15 | D, A, B, C | 4 | 0
SLOT 1 | 10 | AD21 | A, B, C, D | 1 | 1
SLOT 2 | 11 | AD22 | B, C, D, A | 2 | 2
SLOT 3 | 12 | AD23 | C, D, A, B | 3 | 3
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TITLE
82559 ETHERNET
REV B
LAST 09/20/01 10:29 AM
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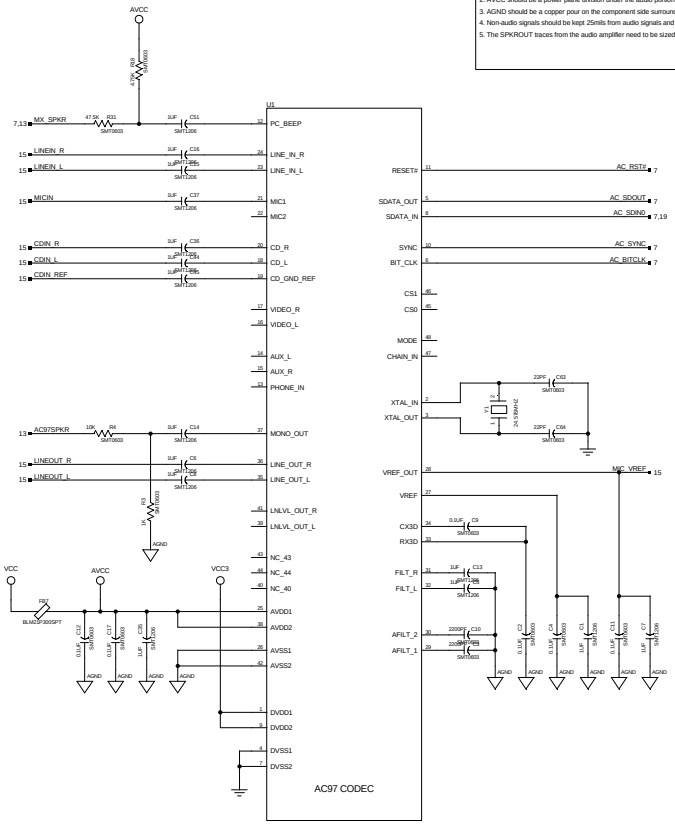
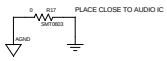
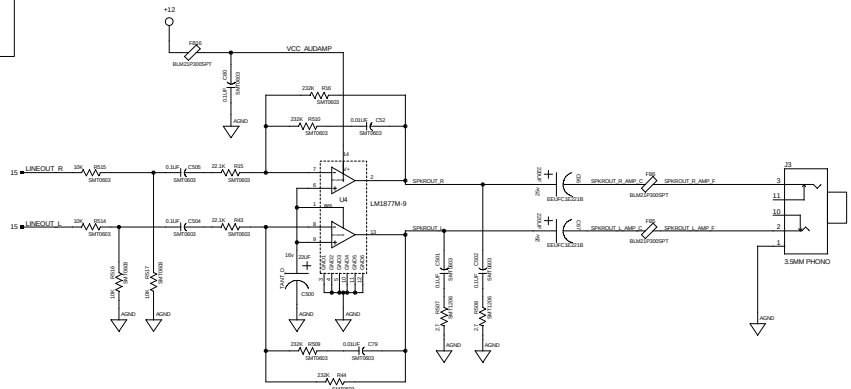
SHEET 14 OF 19

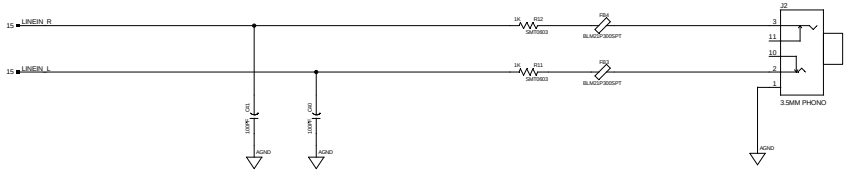
ROUTING NOTES - AUDIO SIGNALS

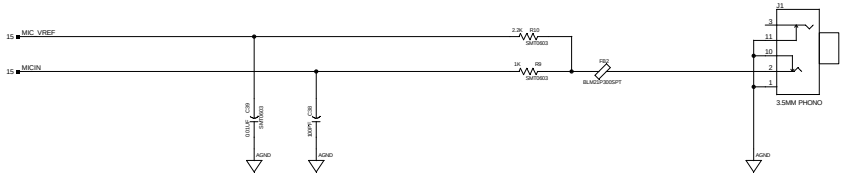
1. The audio portion of the codec includes all signals coming from pins 13 thru 44 of the codec
2. AVCC should be a power plane division under the audio portion of the IC and all audio traces and components
3. AGND should be a copper pour on the component side surrounding the audio traces and components
4. Non-audio signals should be kept 25mils from audio signals and also AGND
5. The SPKROUT traces from the audio amplifier need to be sized to handle 1A each

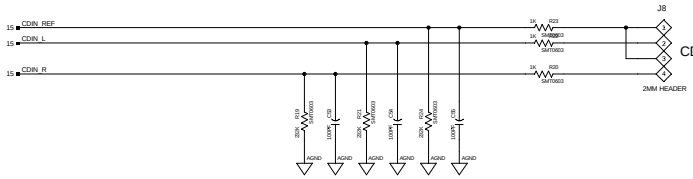


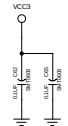












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NOTE: ALL RESISTORS +/- 1%, ALL CAPACITORS +/- 20% UNLESS OTHERWISE NOTED

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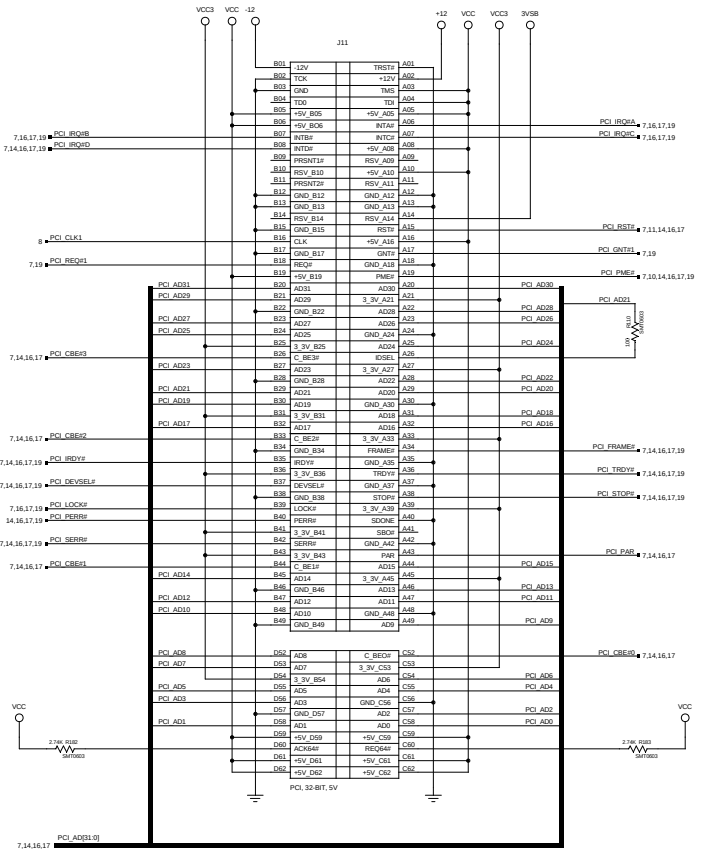
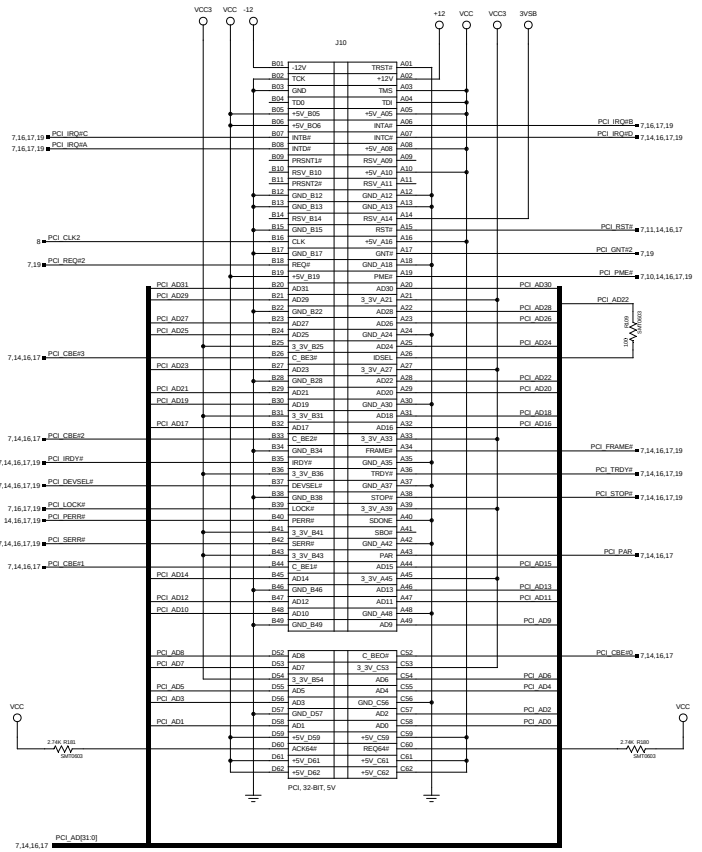
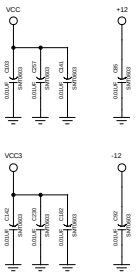
TITLE: AC97 AUDIO		REV: B	
		LAST: 09/20/01 10:29 AM	
DATE: 09/18/01	B	DRAWING: 440MX SCALABLE LOW POWER BOARD	SHEET: 15 OF 19





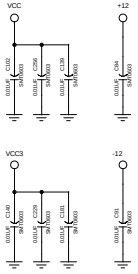
PCI RESOURCES

SLOT	DEV NUM	IDSEL	INT[A,B,C,D]#	PCICLK	REQ/GNT
440MX	7	AD18	A, B, C, D	0	n/a
ENET	4	AD15	D, A, B, C	4	0
SLOT 1	10	AD21	A, B, C, D	1	1
SLOT 2	11	AD22	B, C, D, A	2	2
SLOT 3	12	AD23	C, D, A, B	3	3



PCI RESOURCES

SLOT	DEV NUM	IDSEL	INT[A,B,C,D]#	PCICLK	REQ/GNT
440MX	7	AD18	A, B, C, D	0	n/a
ENET	4	AD15	D, A, B, C	4	0
SLOT 1	10	AD21	A, B, C, D	1	1
SLOT 2	11	AD22	B, C, D, A	2	2
SLOT 3	12	AD23	C, D, A, B	3	3



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TITLE: PCI CONNECTORS 1 AND 2

REV: B

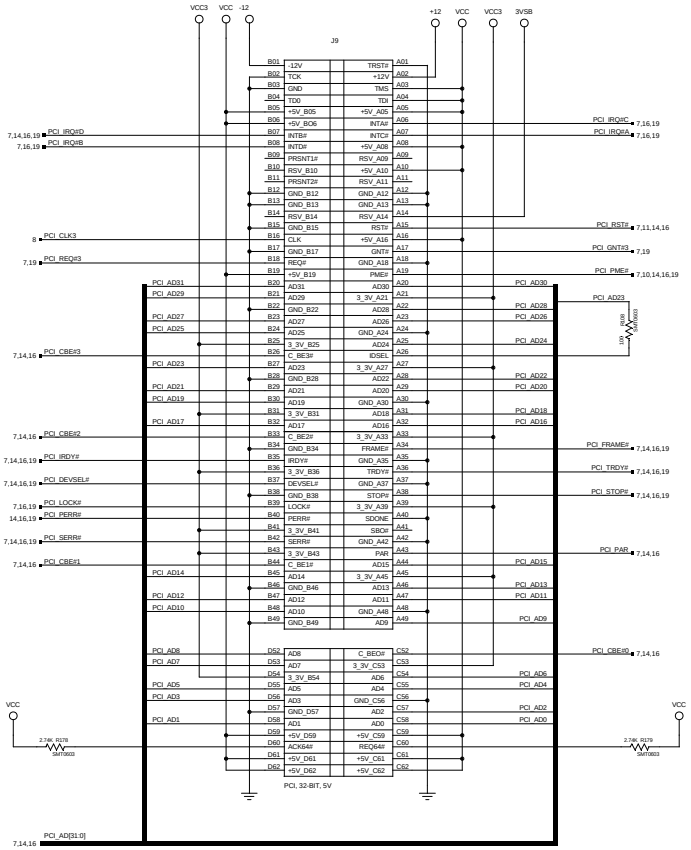
LAST: 09/20/01 10:29 AM

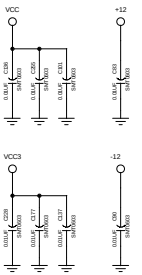
DATE: 09/18/01

B

DRAWING: 440MX SCALABLE LOW POWER BOARD

SHEET: 16 OF 19





PCI RESOURCES

SLOT	DEV NUM	IDSEL	INT[A,B,C,D]#	PCICLK	REQ/GNT
440MX	7	AD18	A, B, C, D	0	n/a
ENET	4	AD15	D, A, B, C	4	0
SLOT 1	10	AD21	A, B, C, D	1	1
SLOT 2	11	AD22	B, C, D, A	2	2
SLOT 3	12	AD23	C, D, A, B	3	3

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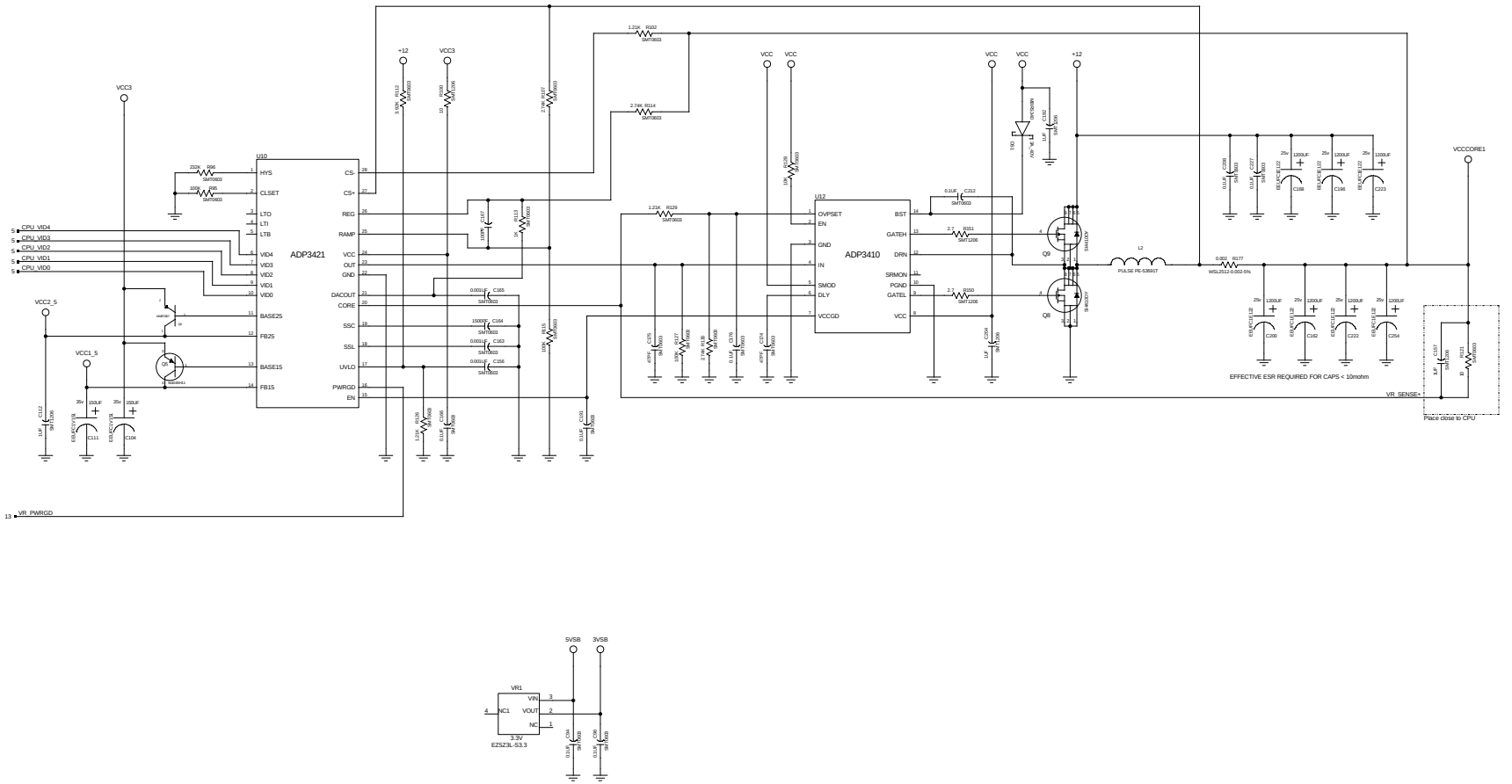
TITLE: PCI CONNECTOR 3		REV: B	LAST: 09/20/01 10:29 AM
DATE: 09/18/01	B	DRAWING: 440MX SCALABLE LOW POWER BOARD	SHEET: 17 OF 19

ROUTING NOTES - POWER SUPPLY

1. Distance from MOSFETs to driver IC should be as small as placement allows
2. Connection between components in the high current path must be sized to handle 25A
3. Add multiple vias where high current traces switch layers to reduce resistance and inductance and improve heat dissipation
4. Avoid routing any signals, including power supply control signals, over the switching power path loop
5. The core voltage sense resistor and parallel capacitor must be located close to the CPU, but far from the switcher



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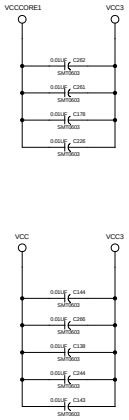
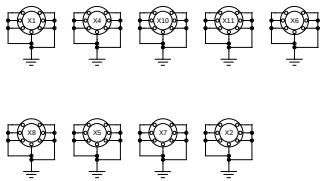
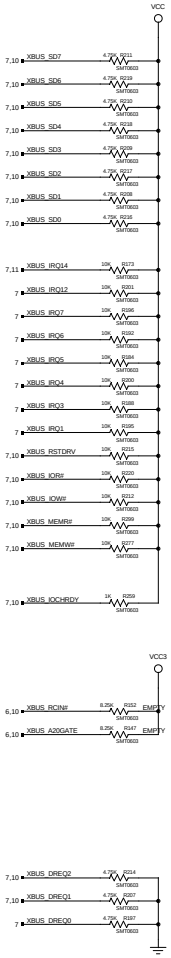
TITLE: VOLTAGE REGULATORS		REV: B	
		LAST: 09/20/01 10:29 AM	
DATE: 09/18/01	B	DRAWING: 440MX SCALABLE LOW POWER BOARD	SHEET: 18 OF 19

POWER PLANE DECOUPLING

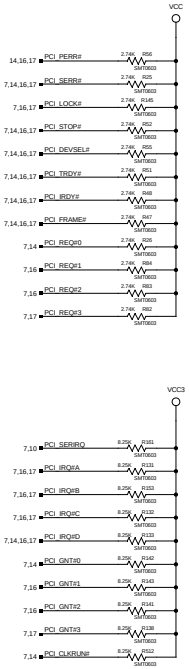




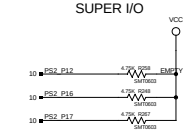
XBUS



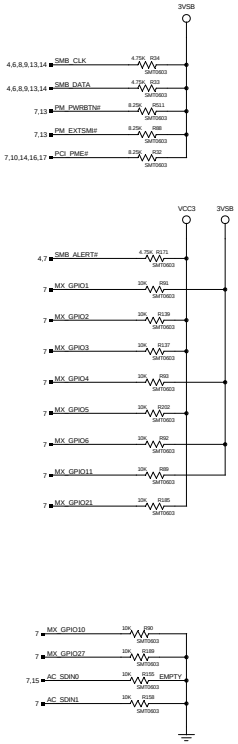
PCI BUS



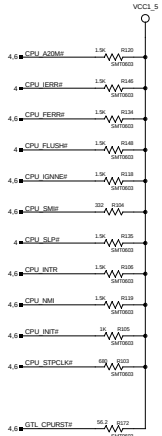
SUPER I/O



MX CHIPSET



GTL+ BUS



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TITLE: PULLUP/PULLDOWN RESISTORS		REV: B	
		LAST: 09/20/01 10:29 AM	
DATE: 09/18/01	B	DRAWING: 440MX SCALABLE LOW POWER BOARD	SHEET: 19 OF 19