



# ***Intel<sup>®</sup> Pentium<sup>®</sup> 4 Processor-M and Intel<sup>®</sup> 845E Chipset Platform Design Guide***

**Addendum for Embedded Applications**

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***April 2003***

Order Number: [251319-002](#)





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## Revision History

Date	Revision	Description
April 2003	002	Add Scalable VRD Schematic.
June 2002	001	Initial release of this document.

## 1.0 Introduction

This document is an addendum to the *Intel® Pentium® 4 Processor in 478-Pin Package and 845E Chipset Platform for DDR Design Guide*. It is targeted for:

- Customers designing with the Intel® Pentium® 4 Processor-M for Applied Computing and Intel® 845E Chipset, and for
- Customers designing a scalable Intel 845E chipset platform, compatible with both the Intel Pentium 4 Processor for Applied Computing and the Intel Pentium 4 Processor-M for Applied Computing.

Designers should refer to the *Intel® Pentium® 4 Processor in 478-Pin Package and Intel® 845E Chipset Platform Design Guide* for the majority of their design. However, for any information pertinent to designing a scalable platform, or for combining the Intel Pentium 4 Processor-M with the Intel 845E chipset, designers should refer to this document. Design issues such as thermal considerations should be addressed using specific design guides or application notes for the processors or chipset, some of which are listed in [Section 1.2, “Related Documents”](#).

These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues. The design information provided in this document falls into one of the two categories:

- *Design Recommendations* are items based on Intel’s simulations and lab experience to date and are strongly recommended, if not necessary, to meet timing and signal quality specifications.
- *Design Considerations* are suggestions for platform design that provide one way to meet the design recommendations. They are based on the reference platforms designed by Intel. They should be used as examples, but may not be applicable to particular designs.

**Note:** The guidelines recommended in this document are based on experience and preliminary simulation work performed at Intel while developing the Intel Pentium 4 processor, Pentium 4 Processor-M and 845E chipset based systems. This work is ongoing, and the recommendations and considerations are subject to change.

## 1.1 Content Overview

[Section 2.0, “Intel® Pentium® 4 Processor-M for Applied Computing Transition Guidelines”](#) contains design guidelines and BIOS guidelines for transitioning the Intel Pentium 4 Processor-M to maximum performance mode at reset.

[Section 3.0, “Voltage Regulator Design Guidelines”](#) contains design guidelines for designing in two separate voltage regulator modules (VRMs) or a single voltage regular-down (VRD) in a scalable platform.

[Appendix A, “High Frequency Transition Sample Schematic”](#) and [Appendix C, “Reference Design Schematics”](#) are references for board designers. While the schematics may cover a specific design, the core schematics will remain the same for most platforms. The schematic set provides a reference schematic for each platform component as well as common motherboard options. The schematics also include the mobile processor transition and voltage regulator design considerations contained herein. Additional flexibility is possible through other permutations of these options and components.

## 1.2 Related Documents

Reference the following documents for more information. All Intel issued documentation revision numbers are subject to change, and the latest revision should be used. Contact your Intel field representative for information on how to obtain Intel issued documentation.

**Table 1. Related Documentation**

Related Documents	Order Number
<i>Intel® Pentium® 4 Processor in 478-Pin Package and 845E Chipset Platform for DDR Design Guide</i>	298652
<i>Mobile Intel® Pentium® 4 Processor - M Datasheet</i>	250686
<i>Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 <math>\mu</math> Process at 2 GHz, 2.20 GHz, 2.26 GHz, 2.40 GHz, and 2.53 GHz Datasheet</i>	298643
<i>Intel® 845E Chipset: Intel® 82845 Memory Controller Hub (MCH) for DDR Datasheet</i>	290742
<i>Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet</i>	290744
<i>Mobile Intel® Pentium® 4 Processor-M Thermal Design Guide for Embedded Applications</i>	273729
<i>Intel® Pentium® 4 Processor for Embedded Applications Thermal Design Guide</i>	273704
<i>VRM 9.0 DC-DC Converter Design Guidelines</i>	249205
<i>Intel® Pentium® 4 Processor VR-Down Design Guidelines</i>	249891

Please refer to the *Intel® Pentium® 4 Processor in 478-Pin Package and 845E Chipset Platform for DDR Design Guide* for the most complete, up-to-date list of related documentation.

## 1.3 Conventions and Terminology

This section defines conventions and terminology that are used throughout this document.

**Table 2. Conventions and Terminology**

Convention/Terminology	Definition
Intel® Pentium® 4 Processor-M for Applied Computing; mobile processor	This part is identical to the Mobile Intel® Pentium® 4 Processor-M.
Intel® Pentium® 4 Processor for Applied Computing; desktop processor, or processor	This part is identical to the Intel® Pentium® 4 Processor.
Chipset	Intel® 845E Chipset
Scalable	As in “scalable platform”, “scalable board”, etc. Used to describe a system that is designed to accommodate either the Intel Pentium 4 processor or the Intel Pentium 4 Processor-M.
MPM	Maximum Performance Mode (enhanced Intel® SpeedStep® technology mode)
BOM	Battery Optimized Mode (enhanced Intel SpeedStep technology mode)
VID	Voltage Identification
VRD	Voltage Regulator-Down
VRM	Voltage Regulator Module

## 2.0 Intel® Pentium® 4 Processor-M for Applied Computing Transition Guidelines

This section contains design guidelines for transitioning the Intel® Pentium® 4 Processor-M for Applied Computing to maximum performance mode at reset.

### 2.1 Background

The Mobile Intel Pentium 4 Processor-M features enhanced Intel SpeedStep® technology, which allows the processor to switch between two core frequencies. The mobile processor operates in two modes, the high frequency Maximum Performance Mode (MPM) or the low frequency Battery Optimized Mode (BOM). By default, the mobile processor will boot to the lower frequency. Certain mobile chipsets, such as the mobile Intel® 845MZ or 845MP chipset, can control the transition between the two modes; however, the Intel® 845E chipset is not capable of controlling the transition. Therefore, when designing a system based on the Intel 845E chipset, additional logic is required to transition the mobile processor from BOM to MPM.

The design guidelines in this section should be used for Intel Pentium 4 Processor-M / Intel 845E chipset based platforms, as well as for scalable platforms. The BIOS guidelines provided in [Section 2.5, “BIOS Enabling”](#) specify provisions for detecting the presence of either a desktop processor or mobile processor, and only initiating transition sequence when a mobile processor is present.

**Note:** The Embedded Intel Architecture Group, which supports the combination of the Intel Pentium 4 Processor-M for Applied Computing and Intel 845E Chipset, does not provide full support for enhanced Intel SpeedStep technology. The only supported aspect of this feature is the transition from battery optimized mode to maximum performance mode at reset. Designers are encouraged to follow the guidelines in this document to ensure proper product support.

## 2.2 Enabling the Mobile Processor Transition

Figure 1 depicts a block diagram for enabling the transition of the mobile processor from BOM to MPM. The additional logic, external to the processor and chipset, required to accomplish this transition is depicted as the shaded block labeled External Logic.

Figure 1. Mobile Processor Transition Block Diagram

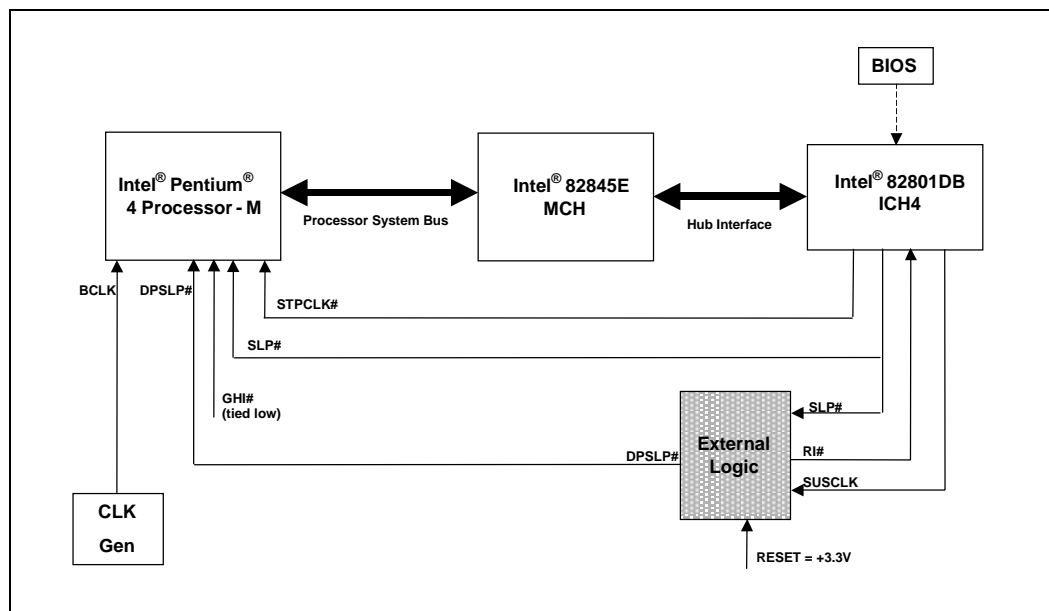


Table 3 explains the various signals involved with the mobile processor transition. Additional details on these signals and the transition sequence follow in later sections.

Table 3. Frequency Transition Signal Overview (Sheet 1 of 2)

Signal	Component(s)/Pin(s)	Definition/Usage
GHI#	CPU (pin A6)	At the transition, GHI# is sampled to determine the mode of the processor. GHI# high = Battery Optimized Mode; GHI# low = Maximum Performance Mode. GHI# must be tied low to correctly transition to MPM. (On the desktop processor, pin A6 is called TESTHI11.)
STPCLK#	CPU (pin Y4) ICH4 (ball V23)	After the BIOS initiates the process, the ICH4 asserts this signal. As a result, the CPU enters Stop Grant state.
SLP# / CPUSLP#	CPU (SLP#, pin AB26) ICH4 (CPUSLP#, ball U21) External logic input	After the CPU is in Stop Grant state, the ICH4 asserts SLP#. As a result, the CPU enters Sleep state. The external logic intercepts this signal as a trigger to continue the transition sequence.
DPSP#	CPU (AD25) External logic output	After the CPU is in Sleep state, the external logic asserts DPSP#. As a result, the CPU enters Deep Sleep state. After a specified length of time, the external logic de-asserts DPSP# and the CPU re-enters Sleep state. (On the desktop processor, pin AD25 is called TESTHI12.)



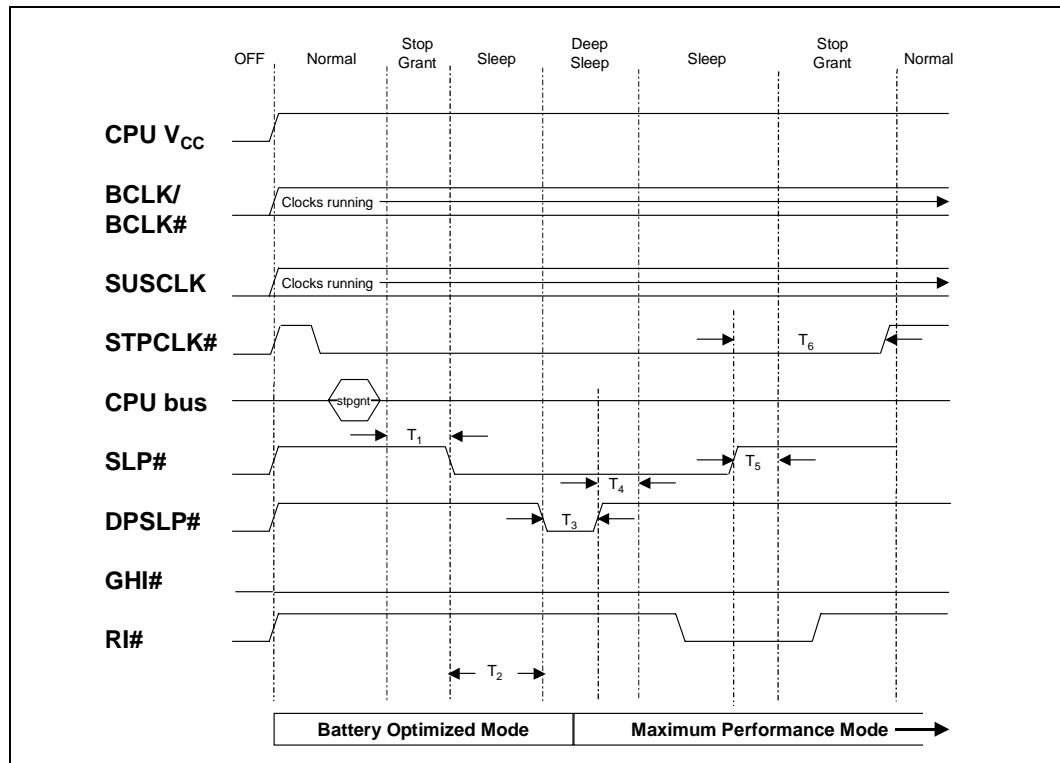
**Table 3. Frequency Transition Signal Overview (Sheet 2 of 2)**

Signal	Component(s)/Pin(s)	Definition/Usage
RI#	ICH4 (ball Y1) External logic output	The external logic asserts RI# (ring indicator) to wake the ICH4. From that point, the ICH4 controls the return of the system to Normal state.
SUSCLK	ICH4 (ball AA4) External logic input	This is the 32.7 KHz clock used to synchronize the external logic.
BCLK	CPU (pins AF22, AF23) Clock generator	The differential BCLK (bus clock) determines the system bus frequency.

## 2.3 Frequency Transition Sequence

Figure 2 depicts the timing diagram for the mobile processor frequency transition sequence from BOM to MPM.

**Figure 2. Transition Sequence Timing Diagram**



The steps in the mobile processor frequency transition sequence are as follows:

- From Normal to Stop Grant** (in-sync with BCLK) – The BIOS enables S1 sleep state. The ICH4 asserts STPCLK#, which causes the processor to initiate a special bus cycle, Stop Grant Acknowledge. 20 BCLKs after the response phase of Stop Grant Acknowledge, the processor enters Stop Grant state.
- From Stop Grant to Sleep** (in-sync with BCLK) – The ICH4 asserts SLP#, which places the processor in Sleep state. SLP# is also an input to the external transition logic, and the assertion

of SLP# triggers the transition logic to begin its execution. Note that the external logic is synchronized with SUSCLK.

3. **From Sleep to Deep Sleep and back to Sleep** (in-sync with SUSCLK) – The external logic asserts DPSLP# after T2. After T3, the external logic deasserts DPSLP#. The system enters Sleep state after T4. Because GHI# is tied low, the mobile processor will transition to MPM and the high frequency.
4. **From Sleep to Stop Grant** (in-sync with SUSCLK, BCLK) – The external logic asserts RI# (ring indicator) to the ICH4, which will take over from here for the wake portion of the sequence. The external logic deasserts RI# in the next SUSCLK cycle. The ICH4 deasserts SLP#, and after T5, the system enters Stop Grant state.
5. **From Stop Grant to Normal** (in-sync with BCLK) – The ICH4 deasserts STPCLK#, and the system enters Normal state.

Table 4 provides timing details for the timings noted in Figure 2.

**Table 4. Timing Details**

T#	Description	Min	Max	Unit
T1	Input signals stable to SLP# assertion requirement	10		BCLKs
T2	SLP# to DPSLP# assertion	10		BCLKs
T3	DPSLP# hold time	1		BCLKs
T4	Deep Sleep PLL lock latency, time required to enter Sleep state after DPSLP# has been deasserted. External logic can assert RI# anytime after this.	0	30	us
T5	Input signal hold time from SLP# deassertion, time required to enter Stop Grant state after SLP has been deasserted	10		BCLKs
T6	STPCLK# hold time from SLP# deassertion	10		BCLKs

**Note:** To avoid compromising signal integrity, the DPSLP# input to the CPU must not sink more than 4mA. In the schematic in Appendix A, “High Frequency Transition Sample Schematic”, the values of resistors R4 and R6 must be selected to properly translate the voltage of this signal, while meeting this sink requirement.

## 2.4 External Logic

System designers must select hardware to fulfill the requirements of the external logic, as stated above. The external logic must accommodate three inputs (SLP#, RESET, SUSCLK) and two outputs (DPSLP#, RI#). Designers may select a PLD, FPGA, or other logic device of their choice and use the state diagram in Figure 3, the simulation timing diagram in Figure 4, and logic diagram and equations shown in Figure 5.

Figure 3. External Logic State Diagram

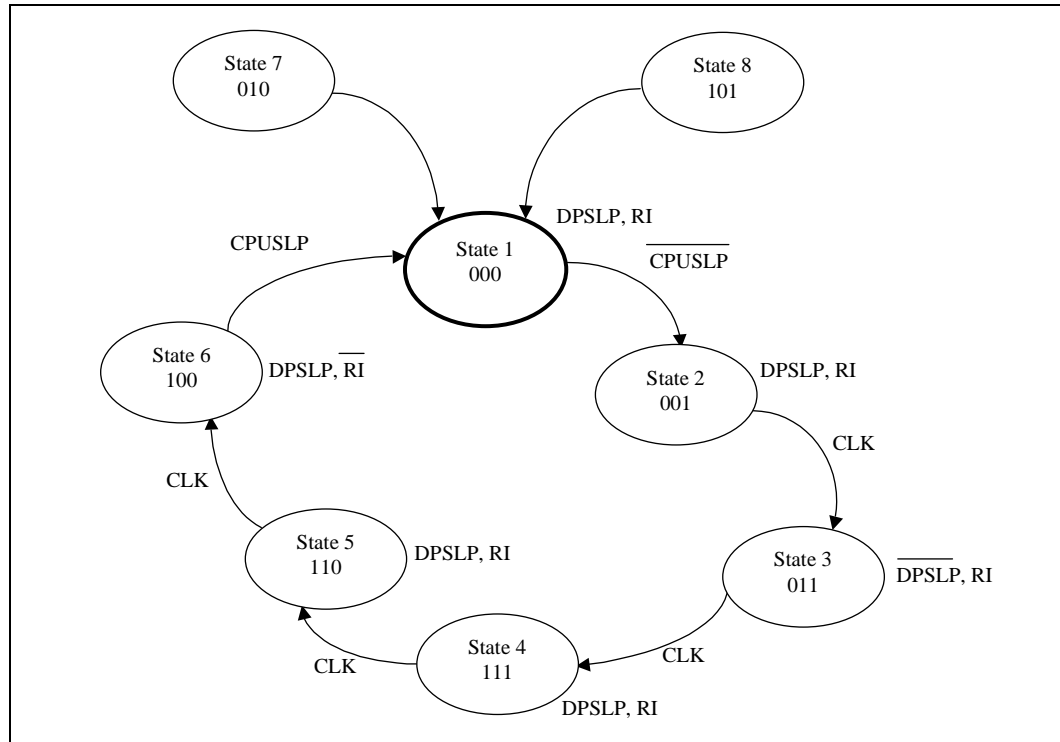


Figure 4. External Logic Timing Diagram

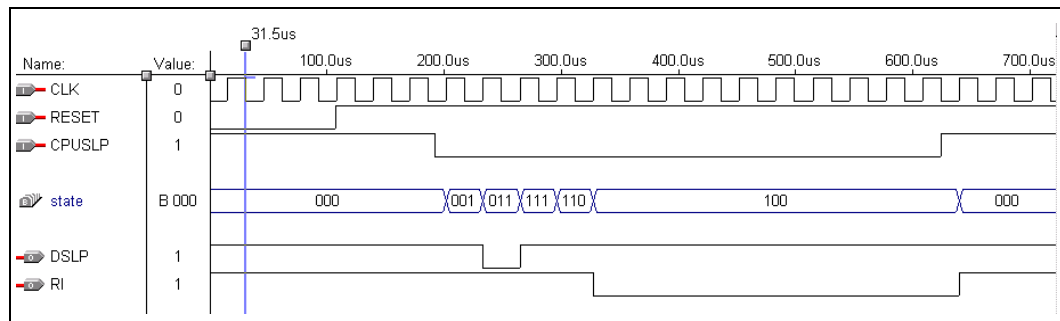
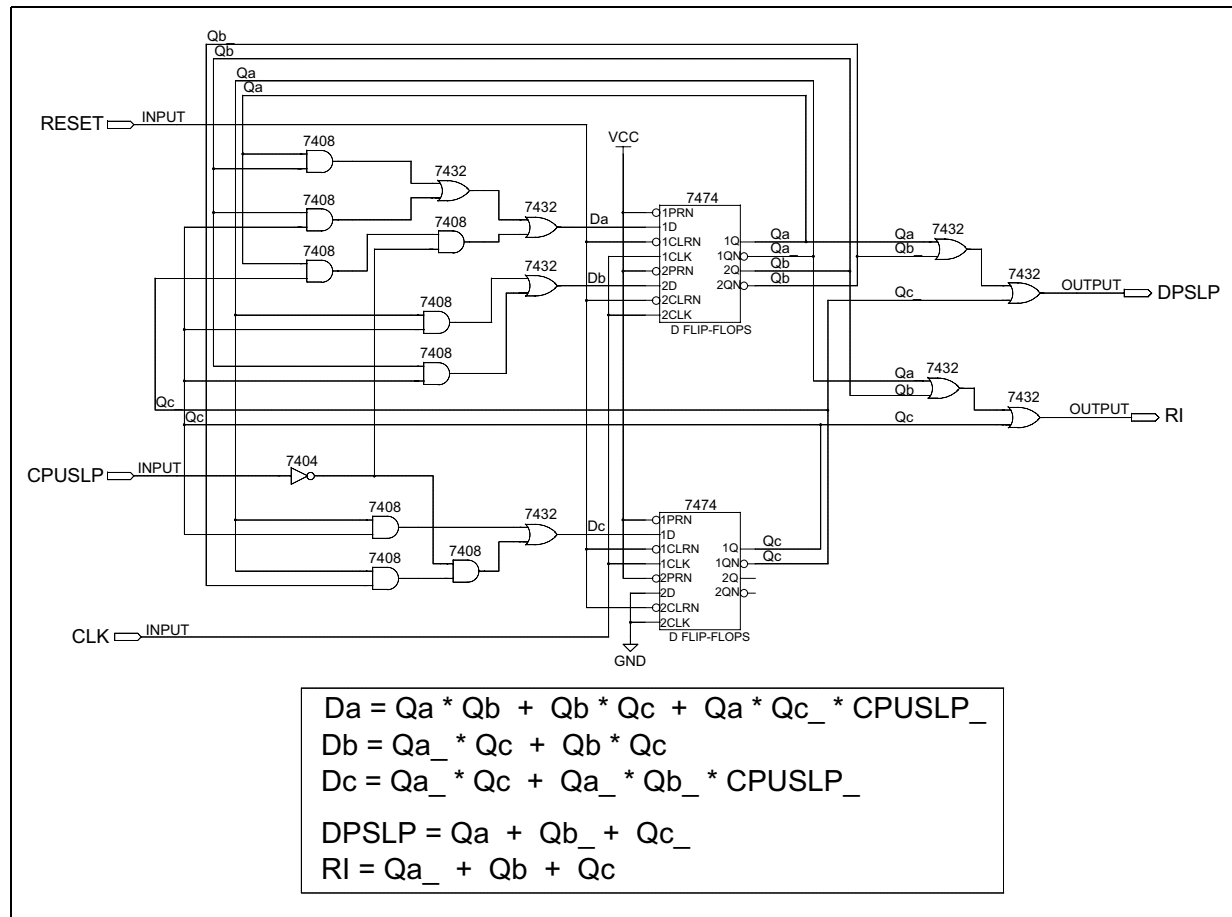


Figure 5. External Logic Diagram



In addition, designers may utilize the following VHDL code to program their external logic device:

```

library ieee;
use ieee.std_logic_1164.all;
entity speed_transition is port(
    clk, rst: in std_logic;
    cpuslp: in std_logic;

    dslp: out std_logic;
    ri: out std_logic
);
end speed_transition;

architecture speed of speed_transition is

signal state: std_logic_vector(2 downto 0);
-- State assignment is such that the logic is reduced
constant state1: std_logic_vector(2 downto 0) := "000";
constant state2: std_logic_vector(2 downto 0) := "001";
constant state3: std_logic_vector(2 downto 0) := "011";
constant state4: std_logic_vector(2 downto 0) := "111";
constant state5: std_logic_vector(2 downto 0) := "110";
constant state6: std_logic_vector(2 downto 0) := "100";
constant state7: std_logic_vector(2 downto 0) := "010";
constant state8: std_logic_vector(2 downto 0) := "101";

```



```
begin
-- If reset is low the state machine will be stable and in state1
process (clk, rst)
begin
if rst='0' then
state <= state1;
elseif (clk'event and clk='1') then
case state is
when state1 =>
if cpuslp = '0' then
state <= state2;
end if;
dslp <= '1';
ri <= '1';

when state2 =>
state <= state3;

when state3 =>
state <= state4;
dslp <= '0';

when state4 =>
state <= state5;
dslp <= '1';

when state5 =>
state <= state6;
ri <= '0';

when state6 =>
if cpuslp = '1' then
state <= state1;
else
state <= state6;
end if;

when others =>
state <= state1;

end case;
end if;
end process;

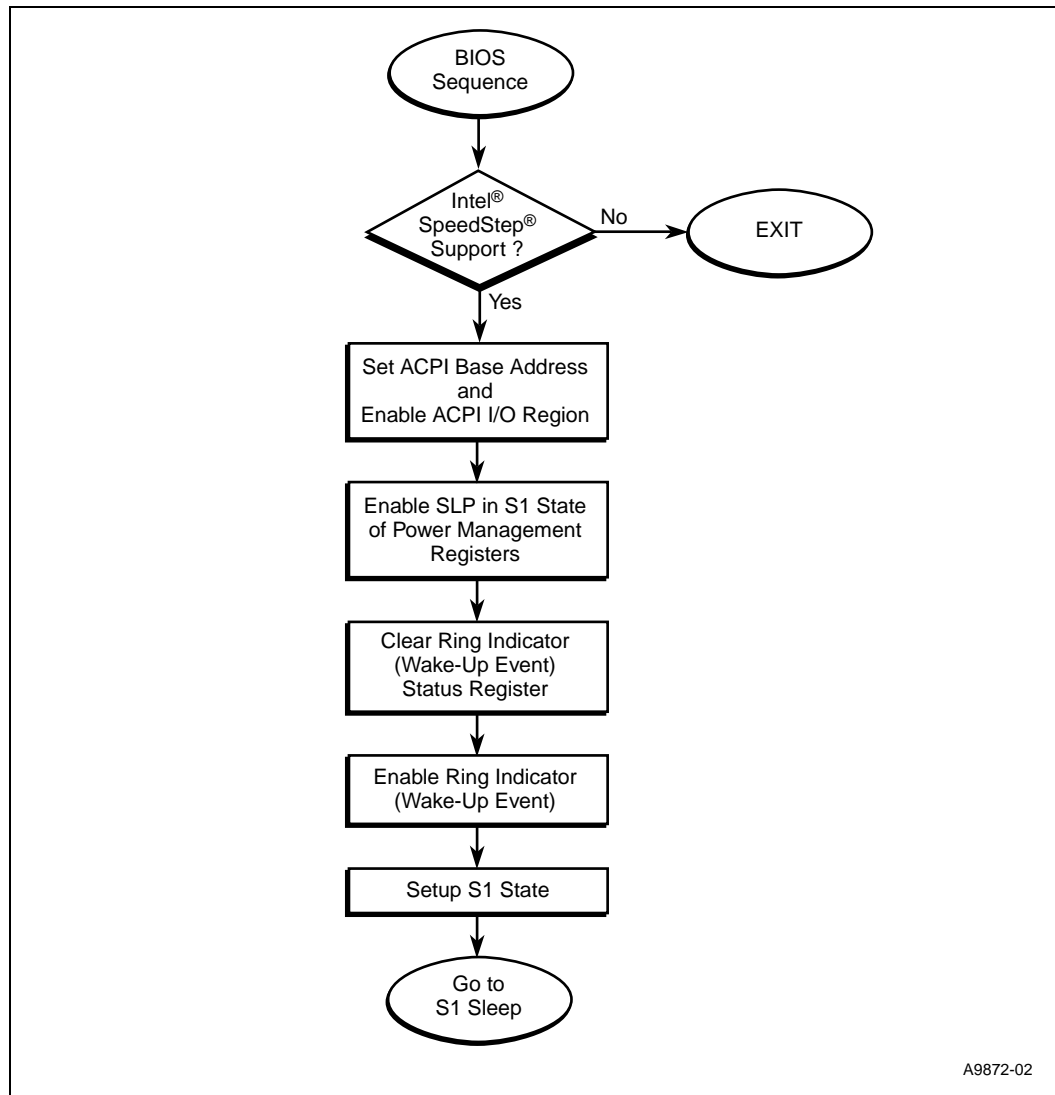
end speed;
```

## 2.5 BIOS Enabling

### 2.5.1 Initiating the Transition Sequence in BIOS

BIOS designers must follow the design guidelines referenced in the *Intel® Pentium® 4 Processor in 478-Pin Package and 845E Chipset Platform for DDR Design Guide*. However, additional BIOS modifications are required to initiate the transition sequence. Figure 6 depicts a flow chart of the required BIOS modifications.

Figure 6. Required BIOS Modifications



The “Intel® SpeedStep® Support?” step above controls whether or not the transition sequence actually takes place. If a desktop processor is present in the socket (as in the case of a scalable platform), the BIOS first checks the processor for enhanced Intel SpeedStep technology support. If enabled (as in a mobile processor), the transition sequence continues; if disabled (as in a desktop processor), the transition sequence does not execute.



The BIOS must run the equivalent of the following psuedo-code during POST, immediately following the initialization of the ICH4:

```
// Initiate an Intel(R) SpeedStep(R) technology sequence.
// This sequence is used to trigger the external logic on board.
// The external logic is triggered by CPUSLP# assertion.
// The external logic asserts the Wake event (Ring Indicator) to wake system.

IF ( SpeedStep-Supported )
{
    Ring Indicator Status, GPE0_STS[8] = Clear
    Ring Indicator Event, GPE0_EN[8] = Enable
    Mask Interrupts
    CPUSLP# signal assert in S1 Sleep, GEN_PMCON_1 [5] = Enable
    Sleep Type, PM1_CNT [12:10] = Desktop S1 State (001h)
    Sleep, PM1_CNT [13] = Enable
}
```

To obtain details on the register utilized to check whether Intel SpeedStep technology is supported, please contact your Intel field representative.

**Note:** The system must not contain an external bus master that could possibly interrupt the above sequence. If so, the BIOS must disable that external bus master.

## 2.5.2 Microcode Updates in BIOS

The Intel® Pentium® 4 processor and Intel® Pentium® 4 Processor-M contain different microcode. If the BIOS contains code to update the processor microcode, the BIOS must be modified to first detect which processor is present in the socket, and then load the appropriate microcode.

## 3.0 Voltage Regulator Design Guidelines

Because scalable platforms do not require advanced power management support, the primary differences between mobile and desktop requirements are the loadline specification and VID table translation. As such, for a scalable platform, Intel recommends one of the two following voltage regulator solutions:

- Design the board to accommodate two voltage regulator modules (VRMs), or
- Design the board with a scalable voltage regulator-down (VRD) on the board.

### 3.1 Scalable Platform Voltage Regulator Modules

For this solution, one connector should be designed onto the board to support either a desktop or mobile VRM. Refer to the *VRM 9.0 DC-DC Converter Design Guidelines* for specifications and design guidelines for the VRM connector. Intel has enabled third party vendors to manufacture the two VRMs. The vendors are listed in [Table 5](#).

**Table 5. VRM Vendors**

Mobile VRM Vendor	Desktop VRM Vendor
Powercube, A Natel Company 9340 Owensmouth Ave Chatsworth, California 91311 USA Contact: Mr. Shree Ramadas Tel: (818) 734-6500 Toll-free: (800) 866-3590 FAX: (818) 734-6540 Toll-free FAX: (800) 866-3589 Email: shree@powercube.com www.powercube.com  Powercube Part Number: VRMP-91-12-40  Sales representatives are located in Japan, China, India, Taiwan, Korea, UK, France, Germany, Norway, Sweden, Finland, Denmark, Austria, Italy, and Israel.	Celestica 4607 S.E. International Way Milwaukie, Oregon 97222 USA Tel: 971-206-2800 FAX: 503-786-5011 Email: power@celestica.com www.celestica.com  Celestica Part Number: 073-20816-01  Sales representatives are located in North America, Japan, Taiwan, and Malaysia.

**NOTE:** These vendors are listed by Intel Corporation as a convenience to Intel's general customer base. Intel does not make any representations or warranties whatsoever regarding quality, reliability, functionality, or compatibility of these devices. This list and/or these devices may be subject to change without notice.

**Caution:** The proper VRM must be plugged into the connector before powering on the board. If the processor and VRM do not match, the VRM will deliver an incorrect voltage level, which may cause damage to the board and components.

### 3.2 Scalable Platform Voltage Regulator Down

A reference design for a VRD for a scalable platform is included in [Appendix B, "Scalable Platform VRD Schematic"](#).





## **Appendix A High Frequency Transition Sample Schematic**

This appendix includes a schematic diagram for one example implementation of the Intel® Pentium® 4 Processor-M transition requirements.





## **Appendix B Scalable Platform VRD Schematic**

This appendix includes a reference schematic for a voltage regulator-down (VRD), compatible with both the Intel® Pentium® 4 processor and the Intel® Pentium® 4 Processor-M.

# APPENDIX B

VIN is the 12V input from ATX power supply before input inductor. It is the preferred way to power drivers.  
 Driver Vcc and PVCC can also be connected to 12V after input inductor if it's difficult to connect them to VIN in the layout.

VID voltage for Intel (R) Pentium(R) 4 Processor and Intel Pentium 4 Processor-M:  
 1). Even though the VID voltages for both Desktop and Mobile operation mode can be the same, the VID codes and the load lines are different.  
 2). To ensure that the same circuit can be used for both processors, a processor identification circuit and a VID code convention logic is needed.

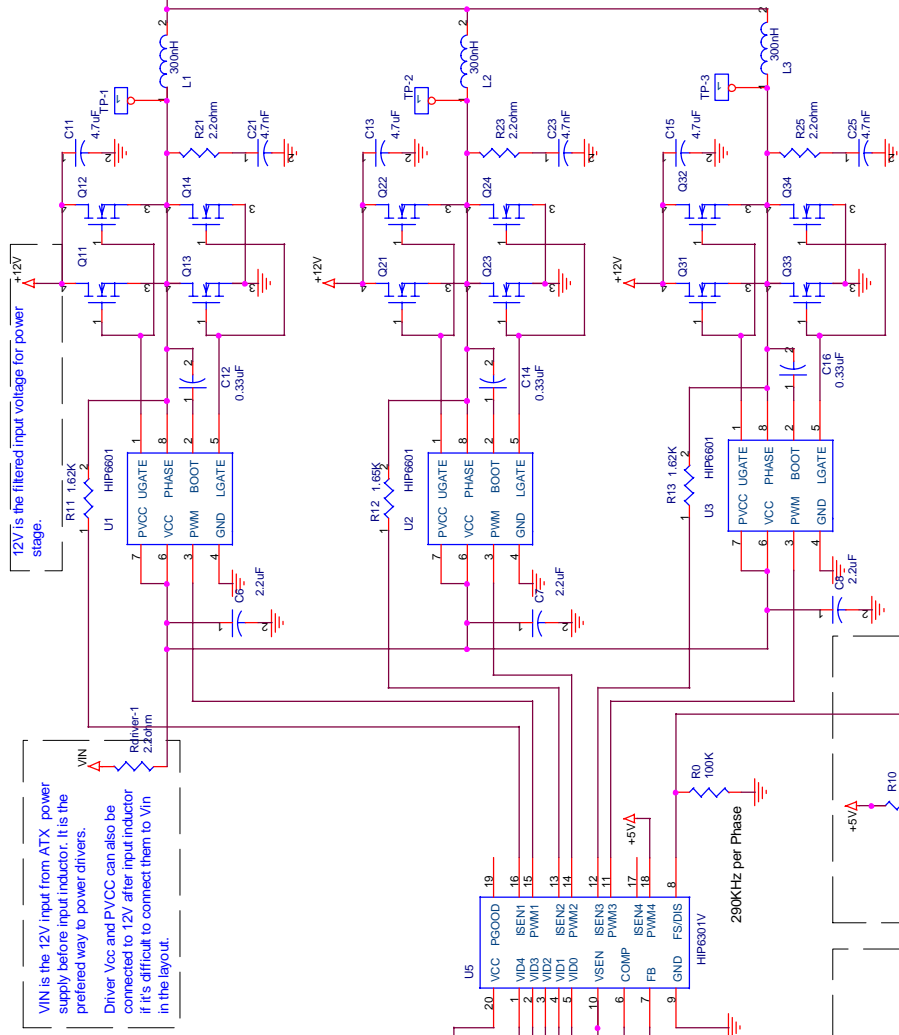
This regulator only uses the desktop VID map to set output voltage. Therefore, when using the mobile processor, glue logic will be needed to map the mobile VIDs to the desktop VIDs.

Optional type-3 compensation components, not needed for most cases

Desktop operation

VR enable circuit is for reference only. Please refer to reference design schematics.

Load-line switching circuit: When Desktop\_operation control signal is High, the VR will operate to the load line.  
 The equivalent resistor of R\_mobile in parallel with R\_desktop determines Desktop operation mode load line.



V\_CORE

Mosfet selection:  
 1). Use Dual-FETs for each switch for better efficiency and thermal performance in a no-fan environment.  
 2). Use Dpak FETs IRLR3714 for upper switch Q11,Q12,Q21,Q22,Q31,Q32  
 3). Use Dpak FETs IRRFR3711 for lower switch Q13,Q14,Q23,Q24,Q33,Q34

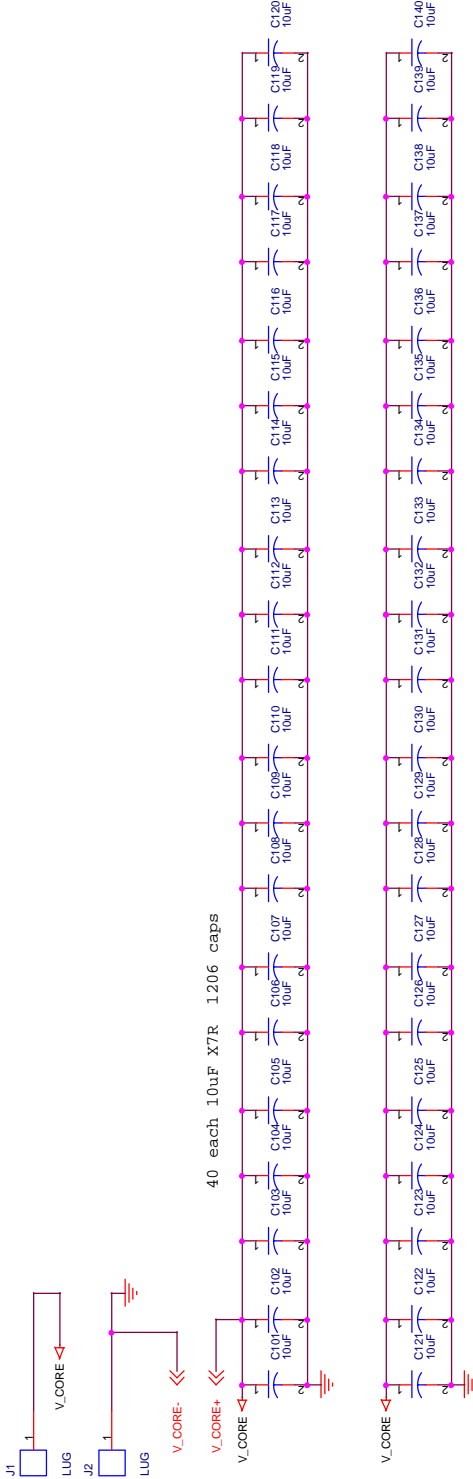
Current sensing and Droop setting:  
 1). Select current sensing resistor R11, R12, R13 based on desktop 70A output current, 5.2mohm Rds,on @ 25C and 65C temperature rise.  
 2). In mobile operation mode, the selection of droop resistor R\_mobile is based on 80mV voltage drop at 40A Maximum load.  
 3). In desktop operation mode, the selection of parallel droop resistor R\_desktop is based on 105mV voltage drop at 70A output.

No-load voltage offset:  
 1). No-load offset is not needed for Mobile operation mode.  
 2). No-load offset for desktop operation mode is -25mV. This offset is done by connection FB pin of HVP6301V to 5V through a 324kohm resistor.

Application Notes:  
 The parameters are for initial test purposes only. Refining the values of compensation network components and droop resistors are needed in order to ensure the actual board meets the spec.

Title		PWM Control and Power Stage	
Doc Number	Intel (R) Pentium (R) 4 Processor and Intel Pentium 4 Processor-M Scalable VIO	Rev	1.5
Sheet	1	of	2
Date:	Monday, April 21, 2003	Sheet	1

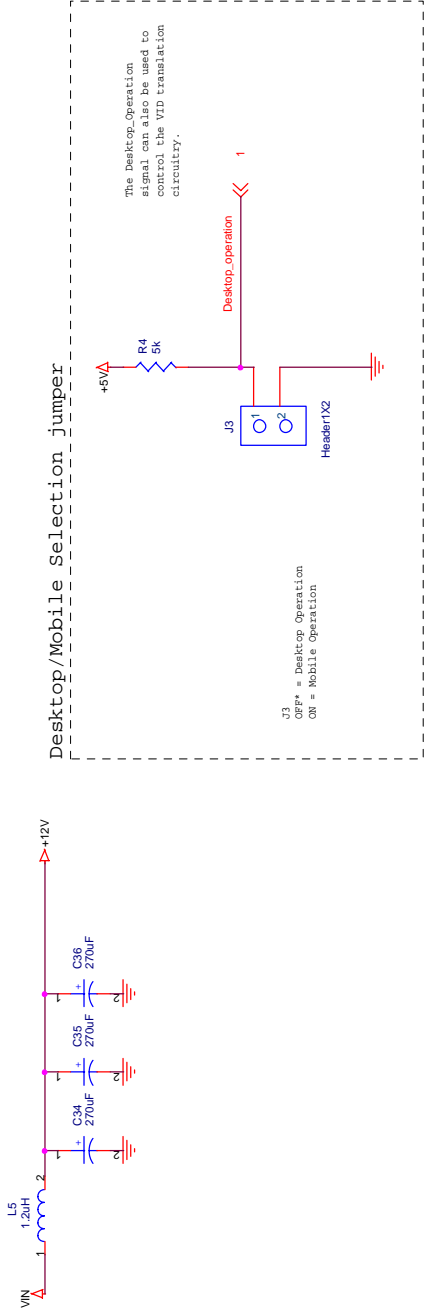
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Notes for output capacitor selection:

1). In Mobile operation mode, it may be necessary to reduce the number of output caps to reduce cost. However, it is important to have the space for 9 output bulk caps so that the same board can be used for both Mobile and Desktop applications.

2). The number of ceramic caps can also be reduced based on actual test results. It is preferred to use small 805 package 10uF caps if available.



Title		OUTPUT CAPACITORS and INPUT FILTER	
Docu	Number	Intel(R) Pentium(R) 4 Processor and Intel Pentium 4 Processor-M Scalable VFD	
Size	B	Sheet	2 of 2
Date:	Monday, April 21, 2003		



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## **Appendix C Reference Design Schematics**

This appendix includes a complete set of board schematics for a scalable Intel® 845E chipset platform, which supports both the Intel® Pentium® 4 processor and Intel® Pentium® 4 Processor-M.

# Intel (R) 845E Interactive Client Reference Design

Revision X2

Last Change : 2002-09-26

APPENDIX C

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34	DDR-POWER
35	POWER

Prefix	Netobject
A_	CRITICAL ANALOG TRACES
AC_	AC97 SIGNAL
APIC_	APIC SIGNAL
AUD_	ANALOG AUDIO SIGNAL
CK_	CLOCK SIGNAL
EEP_	SERIAL EEPROM LANn
EN_	ENABLE FOR POWER SOURCES
F_	FLOPPY DISK SIGNAL
FWH_	FIRMWARE HUB SIGNAL
G_	AGP BUS SIGNAL
GND_	GND SIGNAL DERIVED
GND	GND POWER
H_	P4 HOSTBUS SIGNAL
I2C_	I2C BUS SIGNAL
IDE_	IDE SIGNAL
INT_	INTERRUPT SIGNAL
KB_	KEYBOARD SIGNAL
L_	LPC BUS SIGNAL
LANn_	LAN CONTROLLER n SIGNAL
LP_	LPT1284 SIGNAL
M_	MEMORY BUS SIGNAL
MIDI_	MIDI SIGNAL
MS_	MOUSE SIGNAL
P_	PCI BUS SIGNAL
SPA_	SERIAL PORT n SIGNAL
USB_	USB PORT SIGNAL
V_	POWER
ZV_	ZV VIDRO PORT SIGNAL

	Changes from X1 to X2
1	All BAT54A (0-0031-1261) changed to BAT54 (0-0031-1104) due to wrong polarity
2	R712 changed from 10k to 15k to adjust voltage
3	PU R756 and R757 added @ U38.15 (PG_VDDR) and U38.16 (PG_VIV5)
4	Net on pins U3.54 and U3.55 separated (BSBL[0..1]) due to naming error
5	PU R758 added at CN34.7 (SYS_RESET#)
6	PU R759 added at U39.4 (VIDPWGRD)
7	C717 changed from 4u7 to 1u
8	R607 not populated
9	R571 and R572 not populated (FWH Test Pins)
10	R585 and R586 not populated (for LVDS 18 Bit)
11	R760 and C741 added to U7.50 to generate a V_3V3SB input delay for resume reset
12	R501 and R494 not populated due to PCI config of LAN 82540
13	U36 FWH symbol changed due to wrong pinout (Pin 23, 24 and 25)
14	R496 changed to 4k7 and set to GND (PD M66EN)
15	R525 and R499 is now populated
16	R530 not populated due to wrong V_2V5LAN voltage
17	U20.H4 is now 33R Pullup to V_3V3LAN
18	AC97 Fixup (AC_SDINO -> Changed to AC_SDIN2 on ICH4)
19	Swap ICH4 Pin N20 and P21 (H_HISTB+ / H_HISTB-) due to wrong info in yellow cover
20	LAN 82540 Fixup (R519 populated with 0R, R517 changed to 2K49 and R513 changed to 330R)
21	R615 changed to 4K32 due to Cougar Bug
22	HW Rev changed to 2 at Glue Logic
23	R373 is now populated with 10M
24	CN12.4 must be isolated cause of shortcut of AUD_MIC_BIAS to GND
25	PU R761-R765 added to VID[0:4]
26	PU R766 added to U23.15, PD R767 added to U23.14 (Panellink strapping options)
27	HD-LED-power connected to V_5V0 instead of V_5V0SB
28	PU R768 added to PS_ON
29	PU R769 added to U3.28 (PGOOD0408#)
30	PD R770, R771, R772 added to power enables (default off, if CPLD not configured)
31	PD R773-R776 added to serial port shut down pins
32	Splitted SMI# and PME# signals of SIO0 and SIO1 on ICH4-GPIOs
33	Removed R383, R384, R385
34	Added D25 to avoid crossvoltages from VGA Monitor
35	Added D26 to avoid crossvoltages LPT Port
36	Alternative population of L7 to L12 with resistors (0R)
37	PME# Signal of Cougar (PinB7) is set to V_3V3 via 0R
38	U29 (LP3965EMP) can be replaced by an OR_1206 to power 3V3 on Cougar
39	Possibility to PullDown Pin D6(MD24) on Cougar to enable SDRAM
40	CN41 (JUMPER 3x1) added to connect to MPCI Pins (TIP and RING)
41	V_5V0 input at V_DDR supply is now controlled by XILINK CPLD (Pin 25)
42	Delay of PWRGOOD# (LAN 82540EM Pin A9) to enable correct EEPROM detection
43	

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\* Other names and brands may be claimed as the property of others.

**General Note:**  
 All parts marked 'XXX1' will not be assembled in V1.  
 All parts marked 'XXX2' will not be assembled in V2.

Title		Intel (R) 845E Interactive Client Reference Design
Doc#		845E_Rev21_2002
Rev	Document Number	B444BW
2.00	Rev	
Sheet	of	35

COVER SHEET









DERIVED VOLTAGES -->			
V_12V0VERM	V_12V0VRMF	V_CORE	V_VCCA V_VCCIOPLL
V_12V0	V_FAN1 V_FAN1S V_FAN1SF V_FAN2 V_FAN2S V_FAN2SF V_12V0V8M V_12V0V8F V_12V0V8S V_12V0V8SF V_12V0V8S5 V_12V0V8SF5	V_12V0V8M V_12V0V8F V_12V0V8S V_12V0V8SF V_12V0V8S5 V_12V0V8SF5	
V_5V0S5B	V_3V3SB	V_3V3LAN V_3V3LAN0	V_1V5LAN V_2V5LAN
	V_1V5SB V_KB V_KBF		
	V_DDR	V_DDRREF	
V_5V0	V_USB0 V_USB1 V_USB1X V_USB2 V_USB2X V_USB3 V_USB3X V_USB4 V_USB4X V_USB5 V_USB5X	V_DDRVTT	
	V_1V5	V_1V5A1 V_1V5A2 V_1V5A22	V_HVDD V_ICHPPLL
	V_3V3AGP	V_2V5_LVD V_LVDD1 V_LVDD2 V_LVDD3	V_2V5_LVD1 V_2V5_LVD2 V_2V5_LVD3
		V_2V0_2V5 V_2V5_VDD V_VCC1 V_AVCC1 V_PVCC1 V_VREF_S11 V_DBL	V_VDD1 V_VDD2 V_VDD3
	V_5DV1 V_FIDE V_SIDE V_FIR V_IR	V_5V0CF V_5DV1F V_IOLAN V_GAME V_GAMEF	V_DL_CL V_DL_CLF V_AVDD V_FPVDD V_TVDD V_VPDD
V_3V3	V_1V2VID V_1V8 V_CLK		
V_3V3SB	V_RTC		
V_BAT	V_RTCEBIAS		
V_-12V0			
V_-5V0			

I2C DEVICES		
DEVICE	ADDRESS	BUS
CLOCK GENERATOR	1101001x	SM BUS
SO-DIMM0	1010000x	SM BUS
SO-DIMM1	1010001x	SM BUS
ICH4 SLAVE	1000100x	SM LINK
LAN CONTROLLER	N/A	SM LINK
LM87 HW MONITOR	0101110x	SM BUS

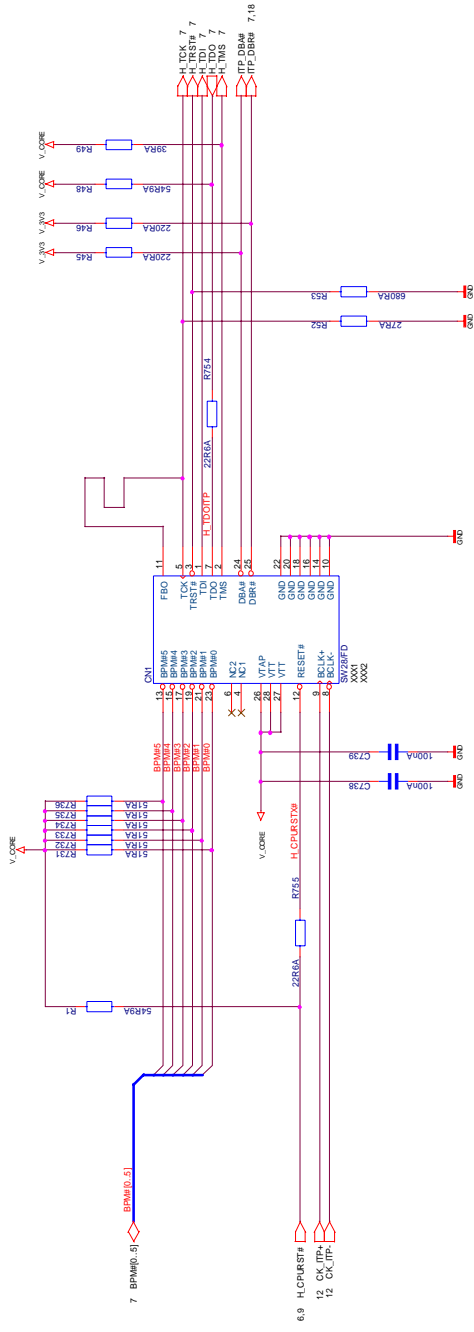
PCI/AGP DEVICES				
DEV	IDSEL	DEVICE	IRQ	REQ/GNT
00	AD16	SMT31 AGP	A	AGP
01	AD17	LAN10/100/1000T	G	4
02	AD18			
03	AD19			
04	AD20			
05	AD21			
06	AD22			
07	AD23	INTERNAL LAN	N/A	N/A
08	AD24	MINI PCI SLOT	E-F	3
09	AD25	STD PCI SLOT	A-B-C-D	0
10	AD26	RISER SLOT1	B-C-D-A	0
11	AD27			
12	AD28			
13	AD29	RISER SLOT2	C-D-A-B	1
14	AD30			
15	AD31	RISER SLOT3	D-A-B-C	2

ICH4 GPIOs		
GPIO	DEVICE	SIGNAL NAME
GPIO6	SUPER I/O 0	SIO0_SMI#
GPIO7	SUPER I/O 1	SIO1_SMI#
GPIO8	SUPER I/O 0	SIO0_PME#
GPIO11	SUPER I/O 1	SIO1_PME#
GPIO12	CPLD	XC_GPIO2
GPIO13	LAN0_KINERETH	LAN0_ENA
GPIO25	MINI PCI	MPCI_ACT#
GPIO27	CPLD	XC_GPIO1
GPIO28	PRIMARY IDE	IDE_FPD1AG#
GPIO32	SECONDARY IDE	IDE_SPD1AG#
GPIO33	POWERED USB	USB_PWR2ENA#
GPIO34	POWERED USB	USB_PWR3ENA#
GPIO35	FIRMWARE HUB	FWH_WF#
GPIO36	FIRMWARE HUB	FWH_TBL#
GPIO37	PCI RISER	RISER_ID1
GPIO38	PCI RISER	RISER_ID2
GPIO39	AUDIO AMPLIFIER	AMP_SHDN
GPIO40	PCI RISER	NOGO
GPIO41	PCI SLOT	P_PRSNT1#
GPIO42	PCI SLOT	P_PRSNT2#
GPIO43	PCI SLOT	

POWER STATES	
ON IN STATE	POWER PLANE
S5 (SOFT OFF)	V_*SB, V_KB, V_*LAN, V_USB*
S3 (SUS. TO RAM)	V_DDR, V_DDRREF
S0 (FULL ON)	OTHERS







Intel (R) 845E Interactive Client Reference Design	
Title	CPU-ITP
Size	Document Number B444B/W
Doc#	1.055624, 282.21.2030
Rev	2.00

6.02.15.17.10.00.00.06.20.33.35 V\_3V3 V\_CORE  
 4.6.7.11.7.33.35 V\_CORE  
 4.7.10.35 GND

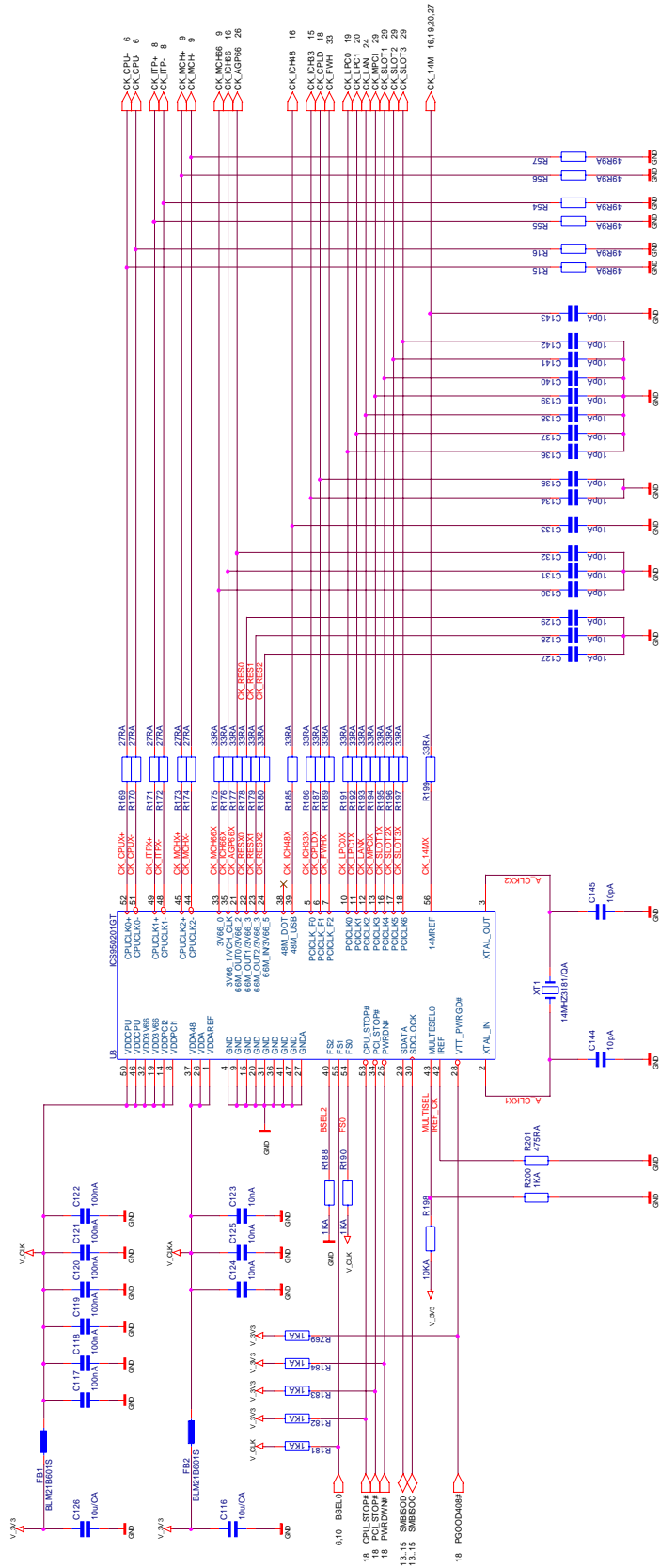










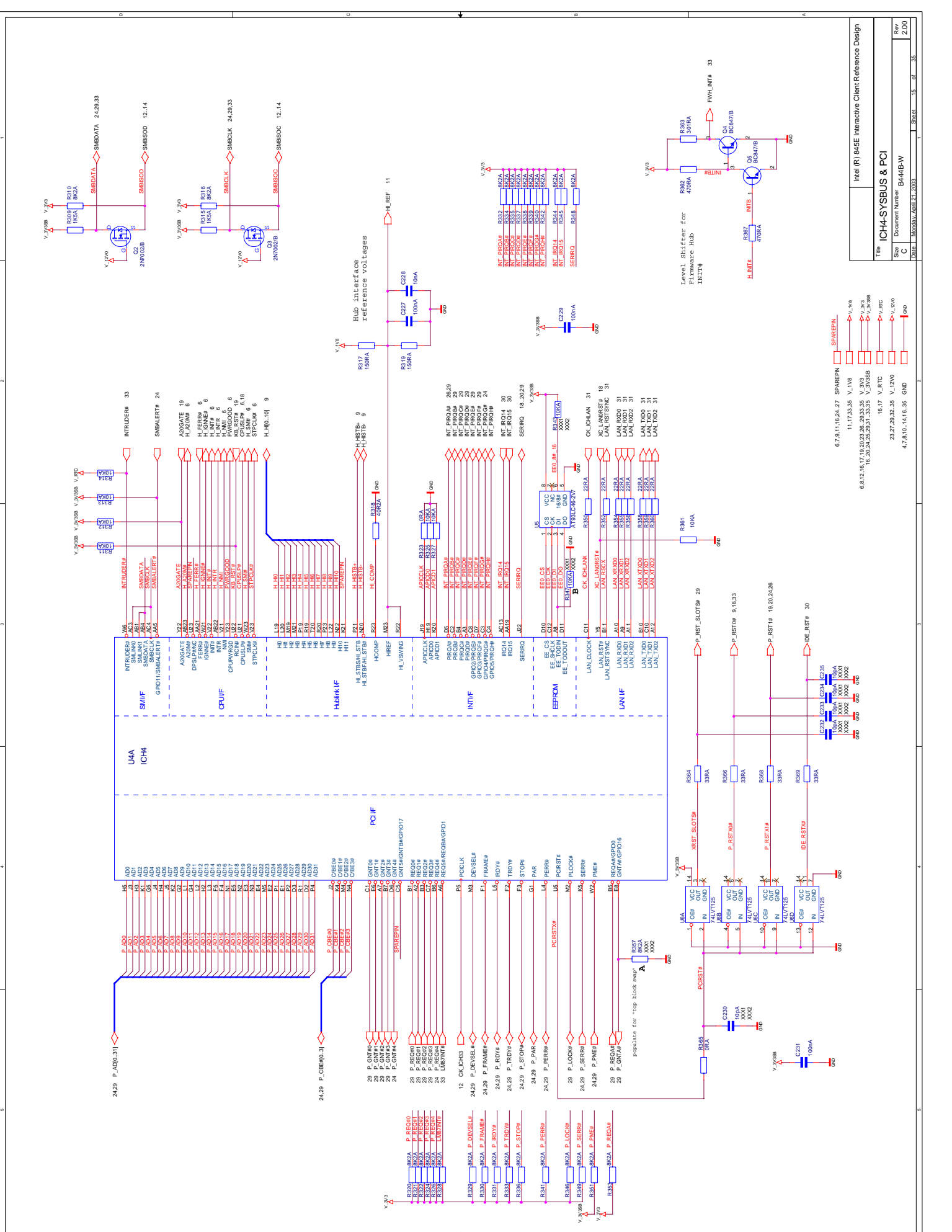


6.8,15,17,19,20,22,24,29,33,35 V\_3V3  
 4.7,8,10,11,35 GND

Intel (R) 845E Interactive Client Reference Design	
Title	CLK ICSS950201
Size	Document Number B444B/W
Rev	2.00
Date	1/25/2001, April 21, 2001

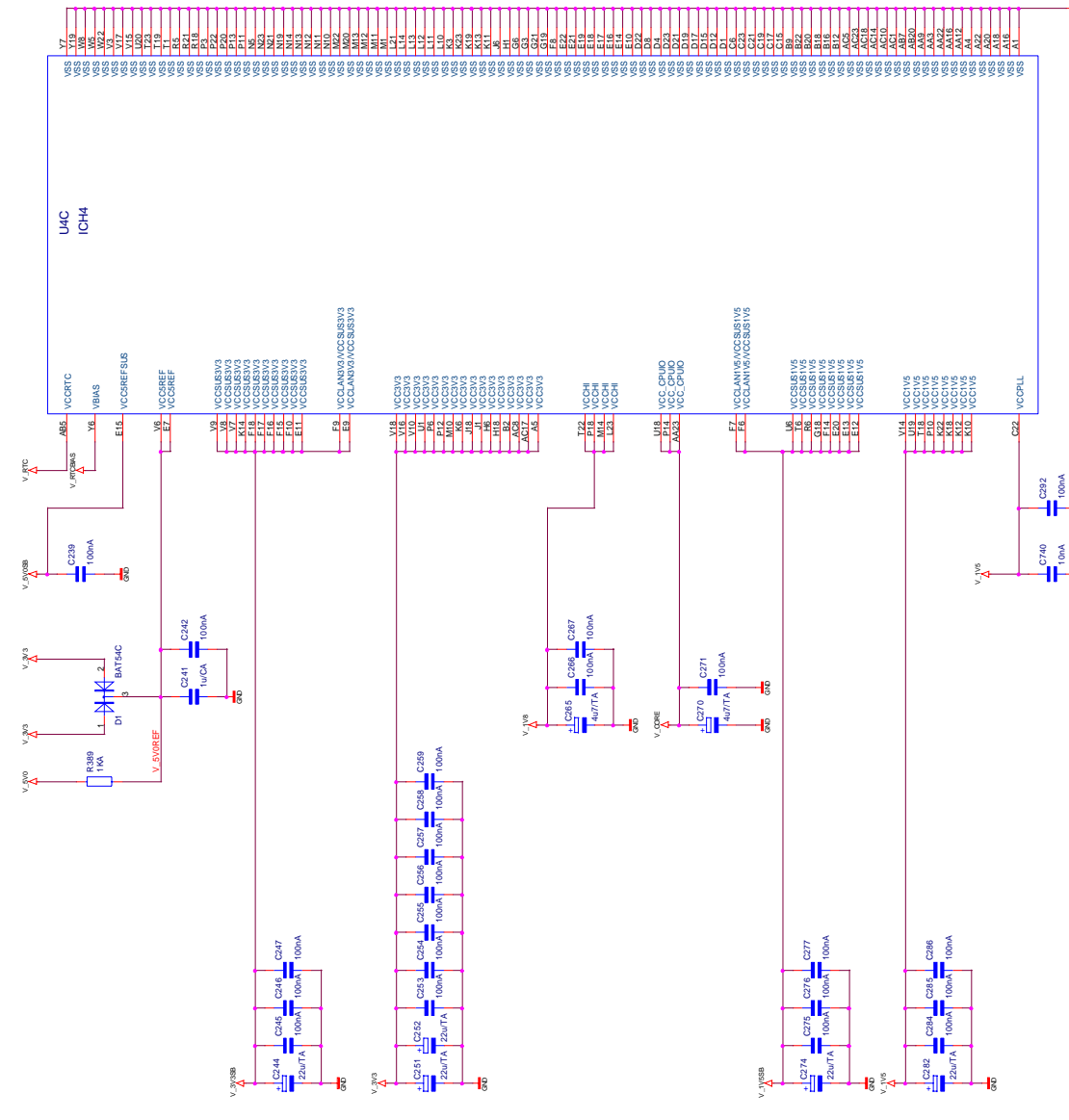
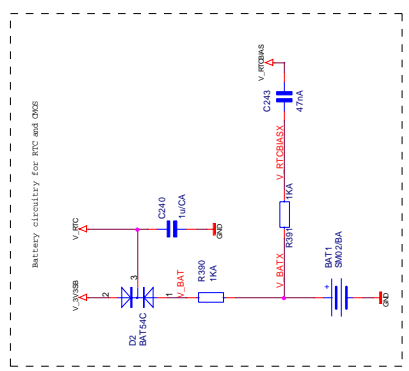






6.7.9.11.6.24.27	SPAREPN#	
11.17.33.35	V_1V8	
6.8.12.14.17.19.20.23.26.29.33.35	V_3V3	
16.20.24.25.29.31.33.35	V_3V3SB	
16.17	V_RTC	
20.27.29.32.35	V_12V0	
4.7.8.10.14.16.35	GND	

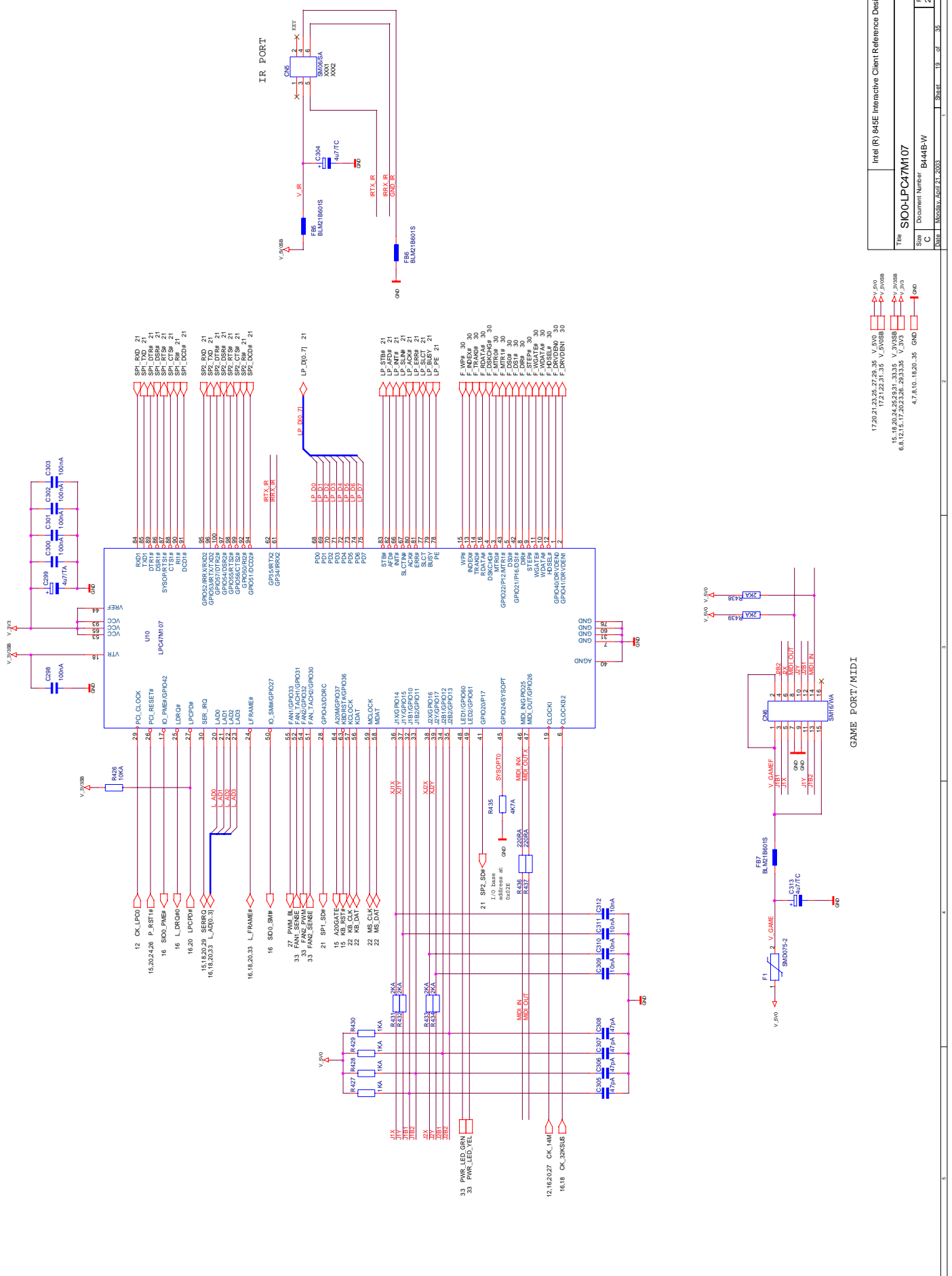




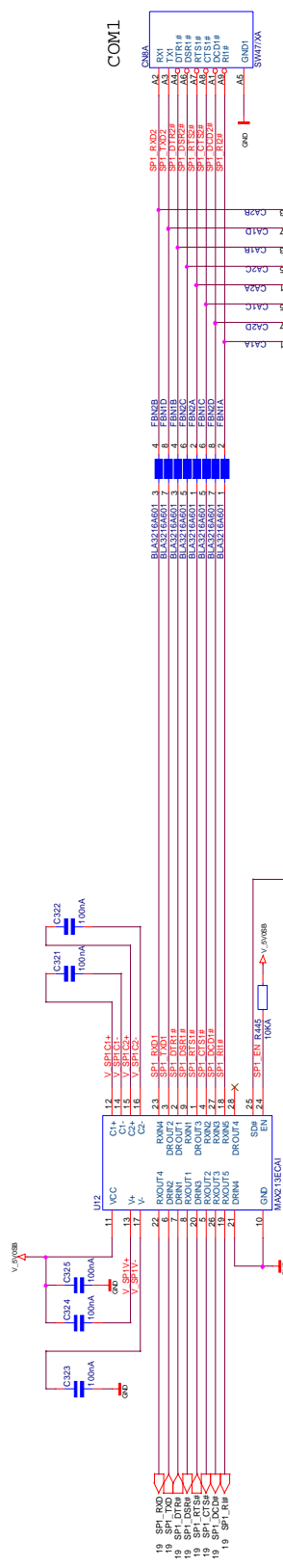
- V\_1V8B 35 V\_1V8B
- V\_1V8C 10.11,28,33,34 V\_1V8
- V\_1V8D 11,15,33,35 V\_1V8
- V\_3V3B 15,15,15,20,34,35,35,31,33,35 V\_3V3B
- V\_3V3C 6.8,12,15,15,19,20,23,26,26,33,35 V\_3V3
- V\_5V0B 19,21,22,31,35 V\_5V0B
- V\_5V0C 18,21,23,25,27,29,35 V\_5V0
- V\_CORE 4,6,8,11,33,35 V\_CORE
- V\_RTC 15,18 V\_RTC
- V\_1V8DMS 15,18 V\_1V8DMS
- 0V0 4,7,9,10,15,18,35 0V0



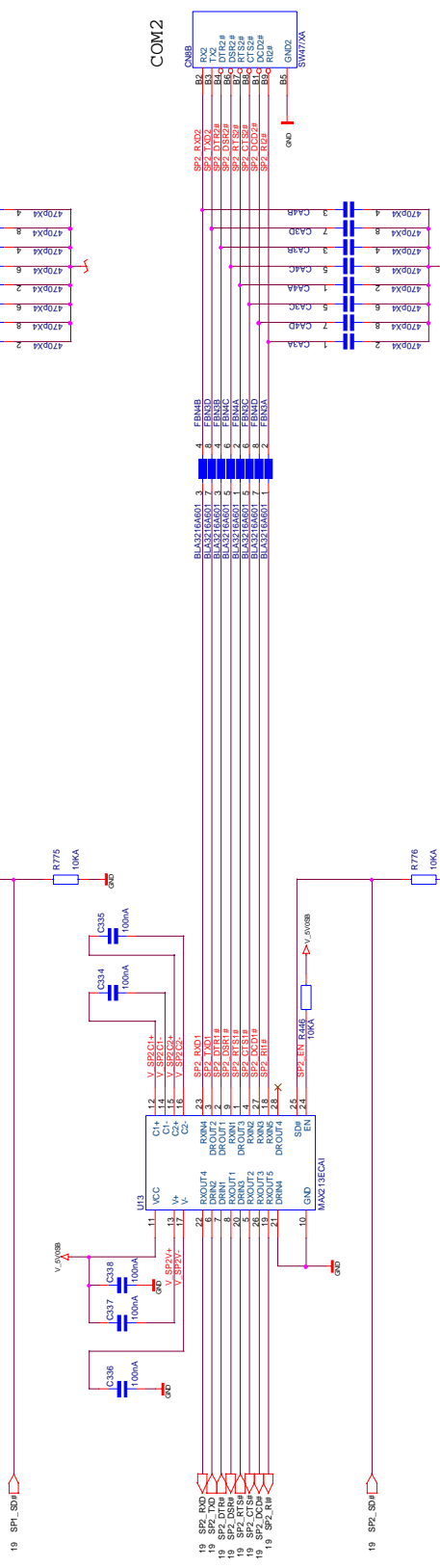




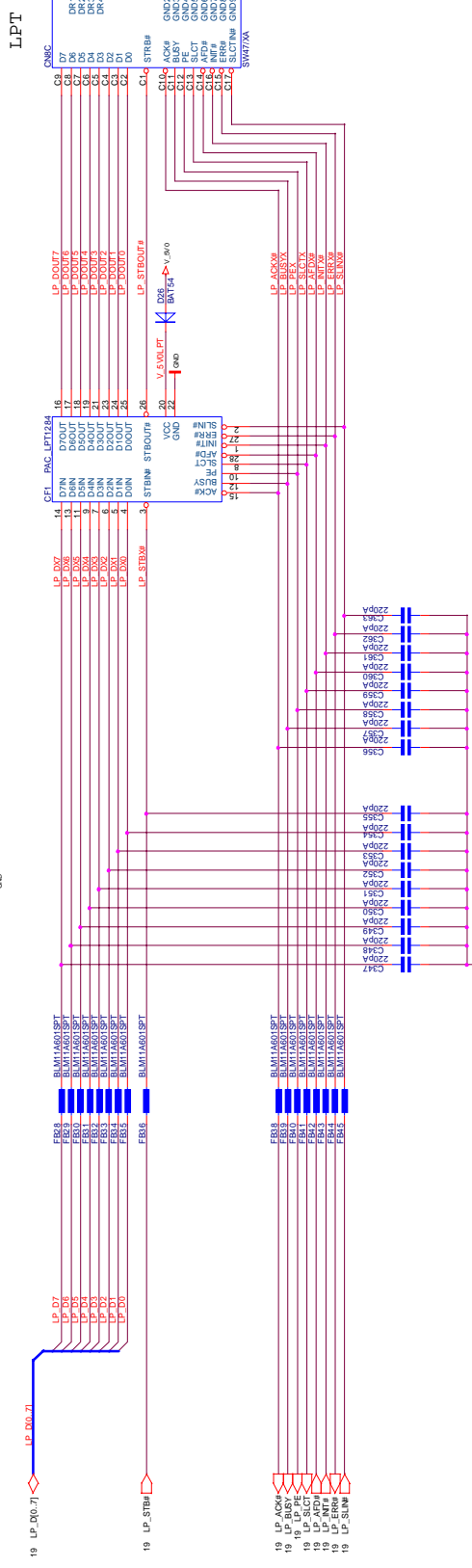




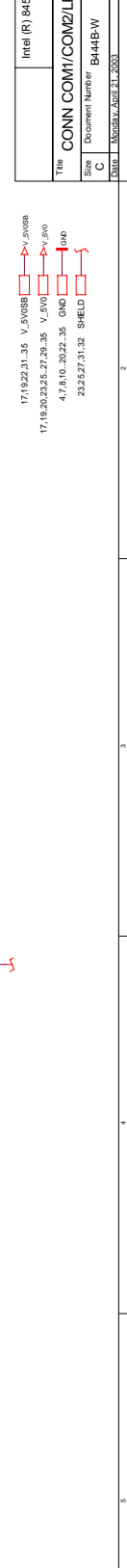
COM1



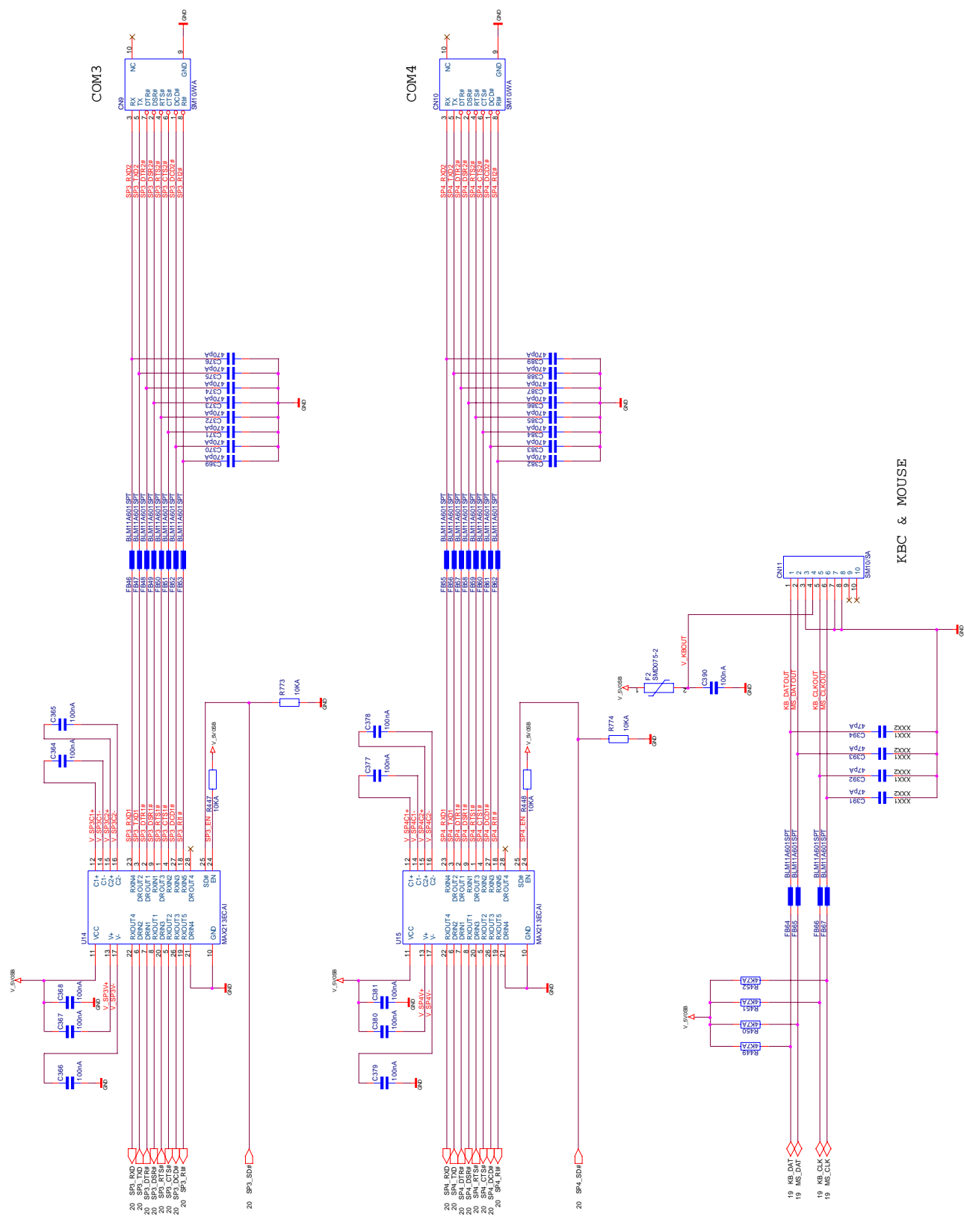
COM2



LPT



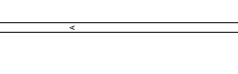
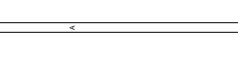
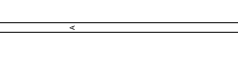
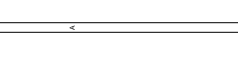
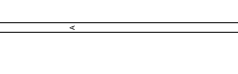
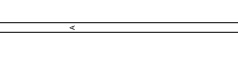
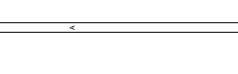
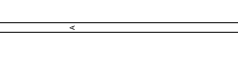
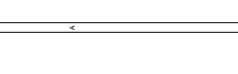
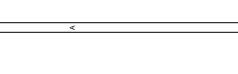
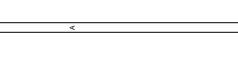
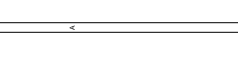
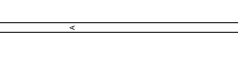
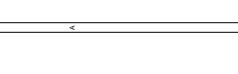
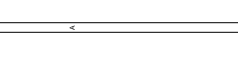
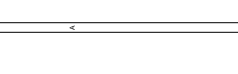
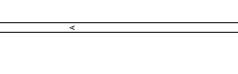
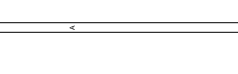
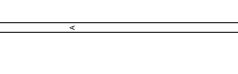
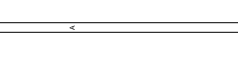
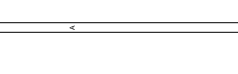
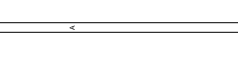
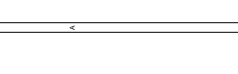
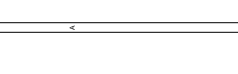
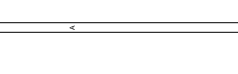
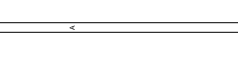
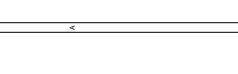
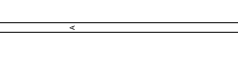
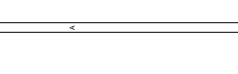
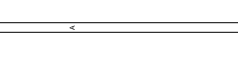
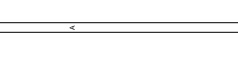
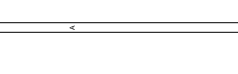
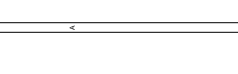
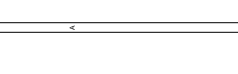
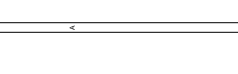
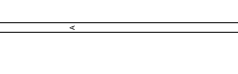
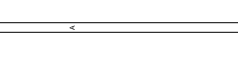
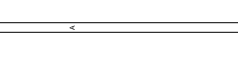
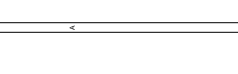
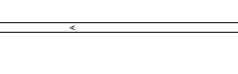
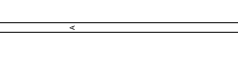
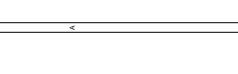
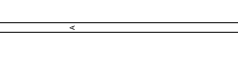
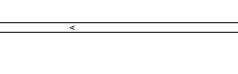
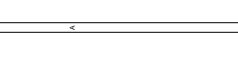
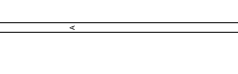
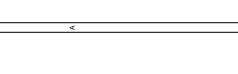
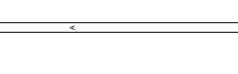
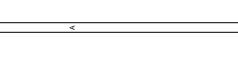
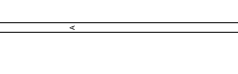
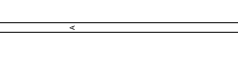
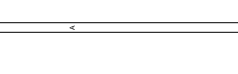
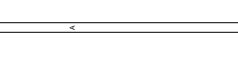
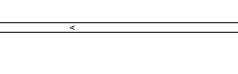
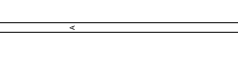
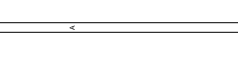
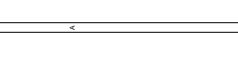
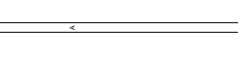
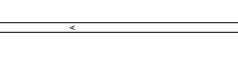
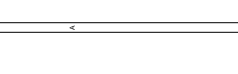
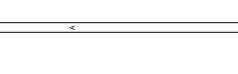
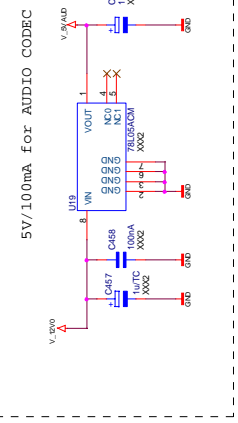
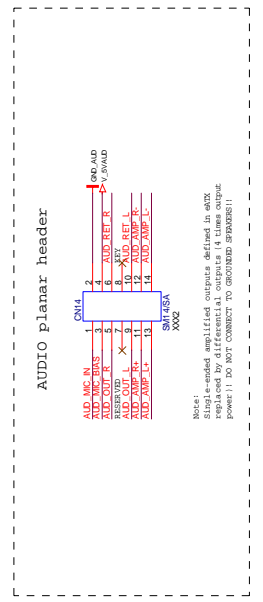
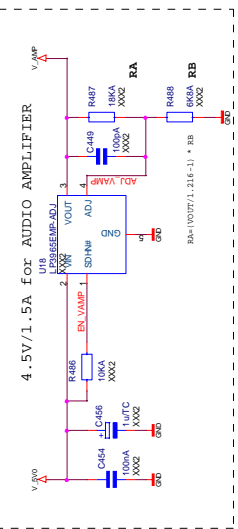
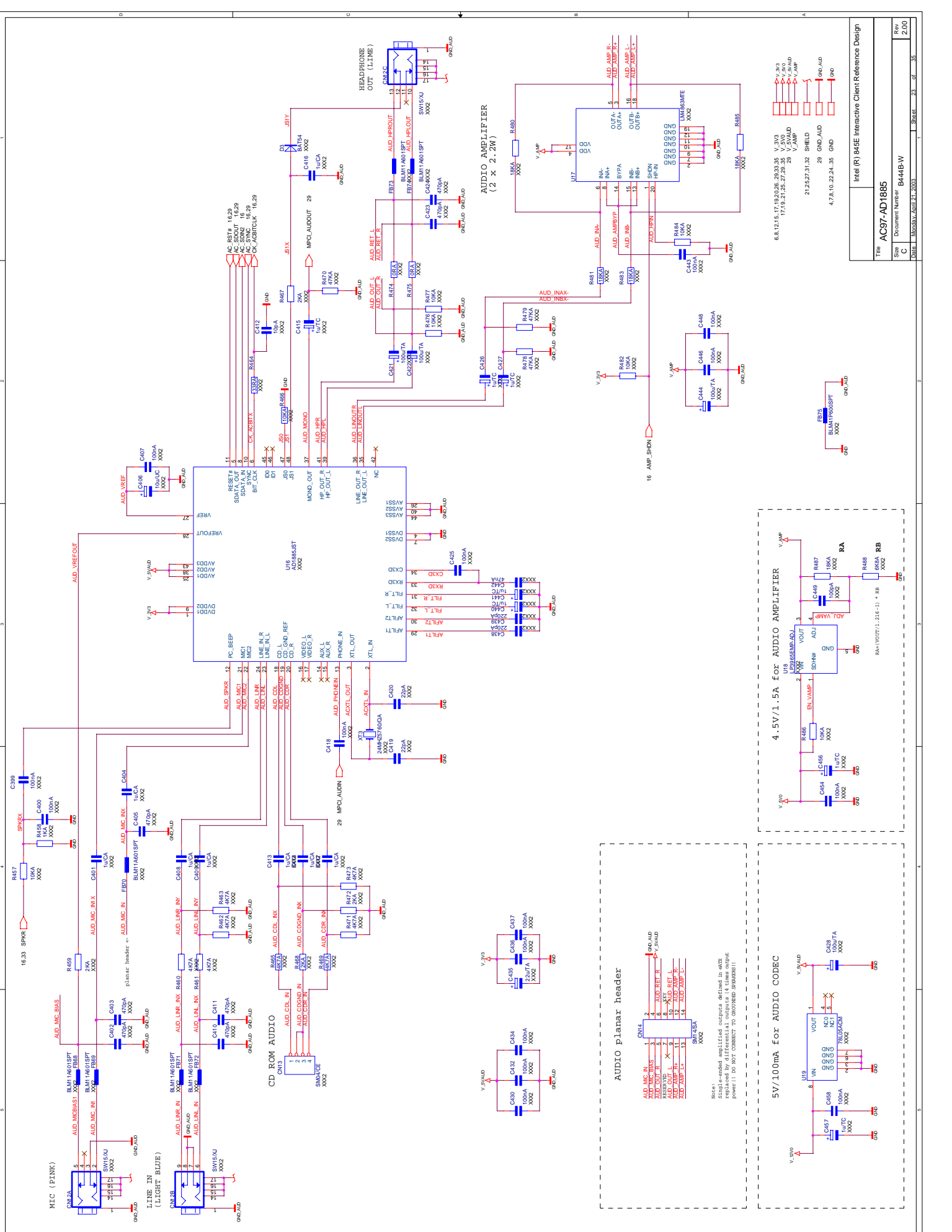
Intel (R) 845E Interactive Client Reference Design	
Title	CONN COM1/COM2/LPT
Size	Document Number B414B/W
Doc#	135555W, April 21, 2000
Sheet	21 of 35
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Intel (R) 845E Interactive Client Reference Design	
Title	CONN COM3/COM4/KBC
Size	Document Number B414B-W
Rev	2.00
Date	1/25/2001, 2/27/2001



KBC & MOUSE



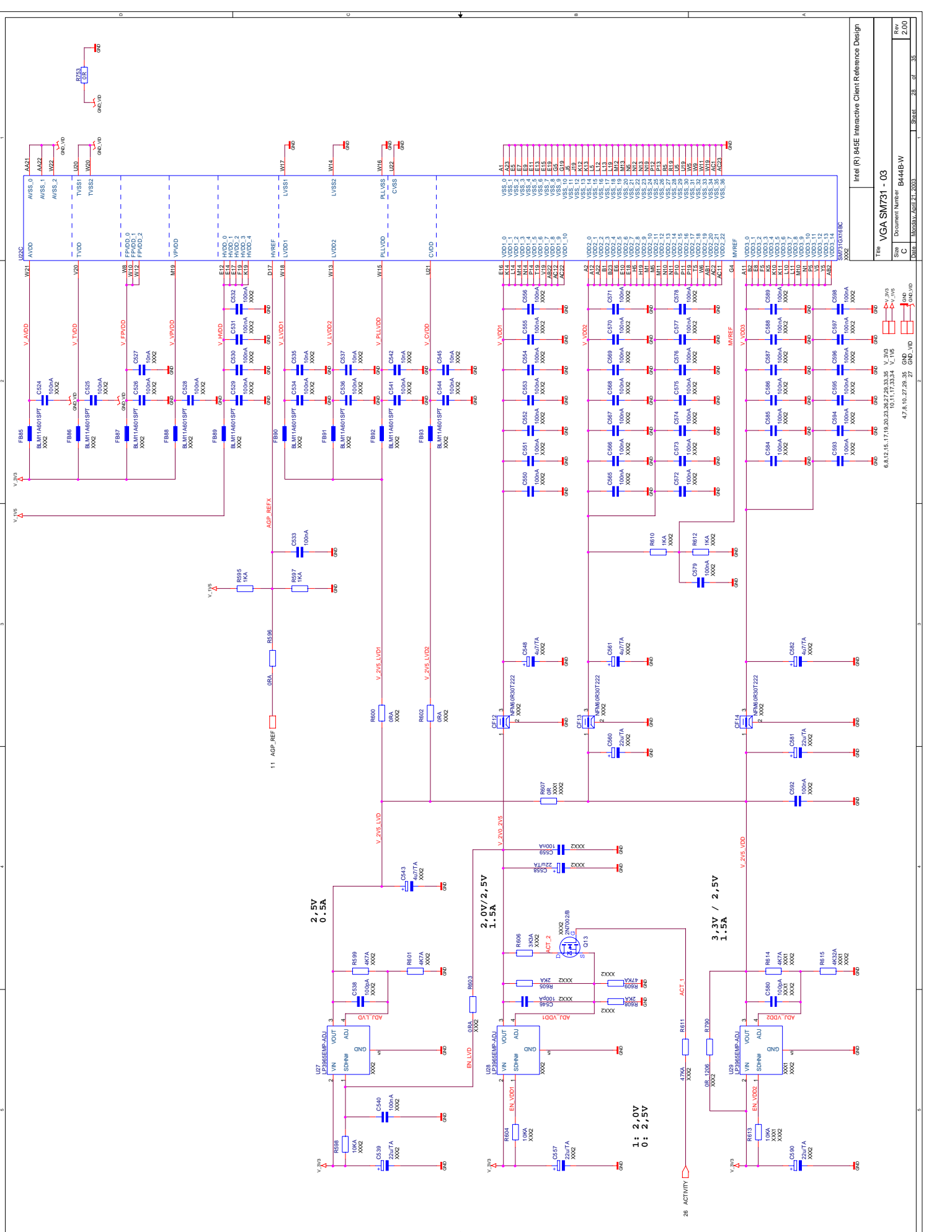












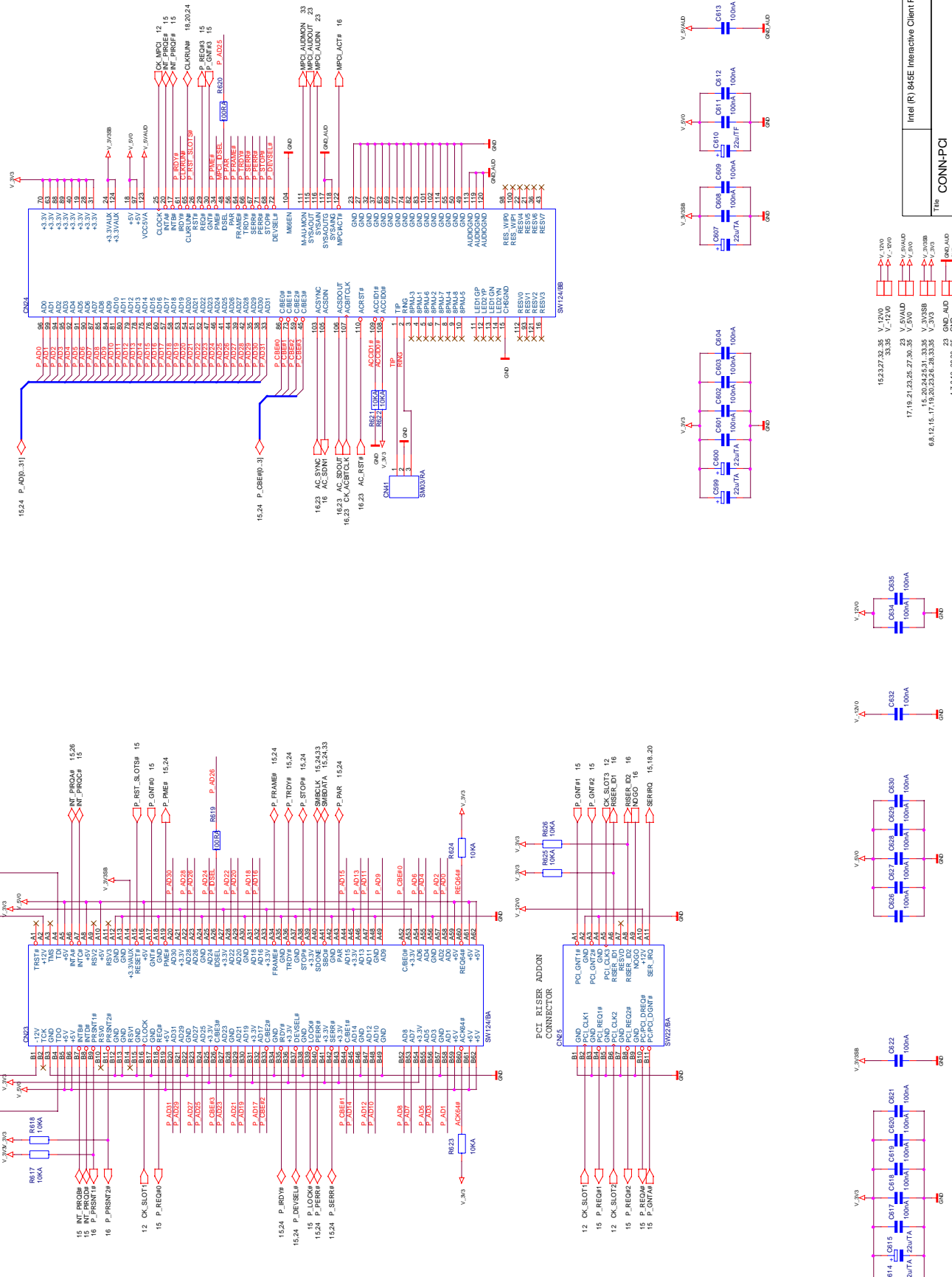
2.5V  
0.5A

2.0V / 2.5V  
1.5A

3.3V / 2.5V  
1.5A

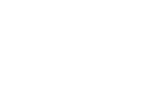
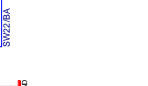
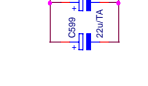
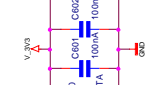
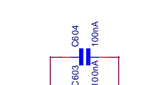
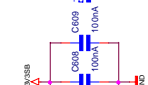
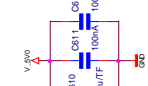
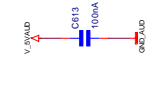
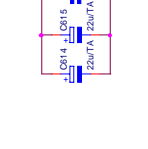
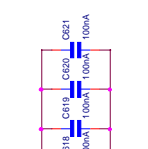
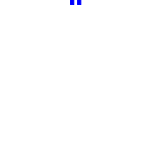
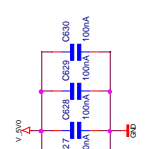
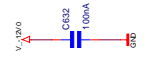
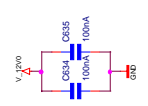
1: 2.0V  
0: 2.5V

VSS_0	A1
VSS_1	B5
VSS_2	E7
VSS_3	F4
VSS_4	E11
VSS_5	F8
VSS_6	E15
VSS_7	F2
VSS_8	E9
VSS_9	F6
VSS_10	E13
VSS_11	F0
VSS_12	E6
VSS_13	F3
VSS_14	E10
VSS_15	F7
VSS_16	E14
VSS_17	F1
VSS_18	E8
VSS_19	F5
VSS_20	E12
VSS_21	F9
VSS_22	E16
VSS_23	F3
VSS_24	E10
VSS_25	F7
VSS_26	E14
VSS_27	F1
VSS_28	E8
VSS_29	F5
VSS_30	E12
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VSS_33	F3
VSS_34	E10
VSS_35	F7
VSS_36	E14



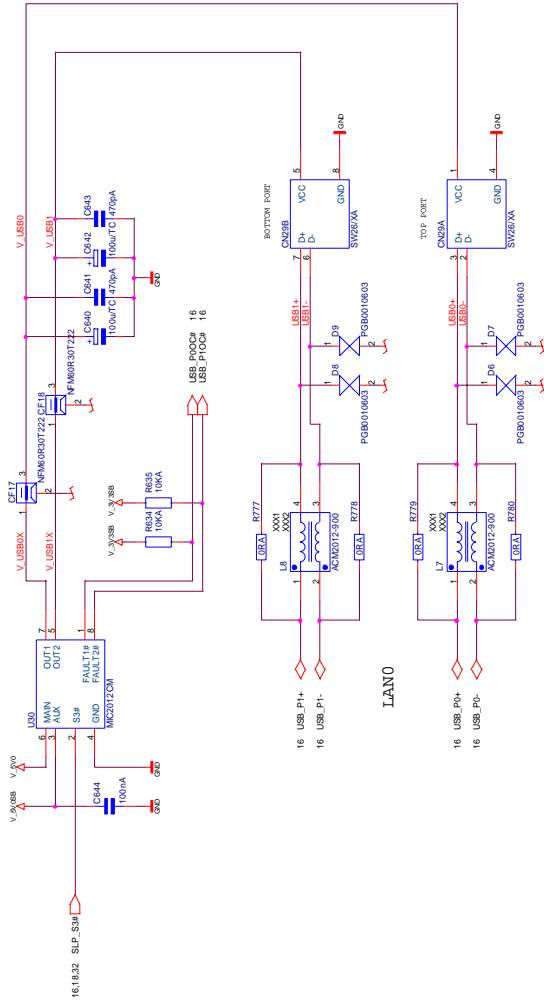
Intel (R) 845E Interactive Client Reference Design	
Title	CONN-PCI
Size	Document Number B444BW
Date	1/2002, Rev 2.00

15.23.27.32.35	V_12V0	15.23.27.32.35	V_12V0
33.35	V_12V0	23	V_5V0
17.19.21.23.25.27.30.35	V_5V0	15.20.24.25.31.33.35	V_3V3SB
6.8.12.15.17.19.20.22.26.28.33.35	V_3V3	23	GNP_AIO
4.7.8.10.28.30.35	GNP	23	GNP_AIO

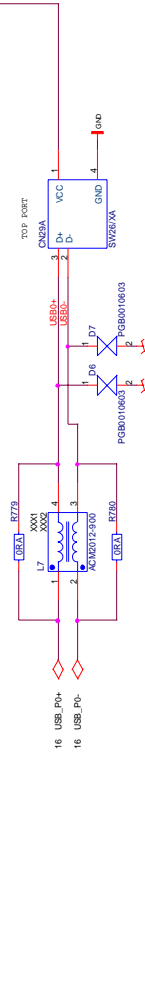




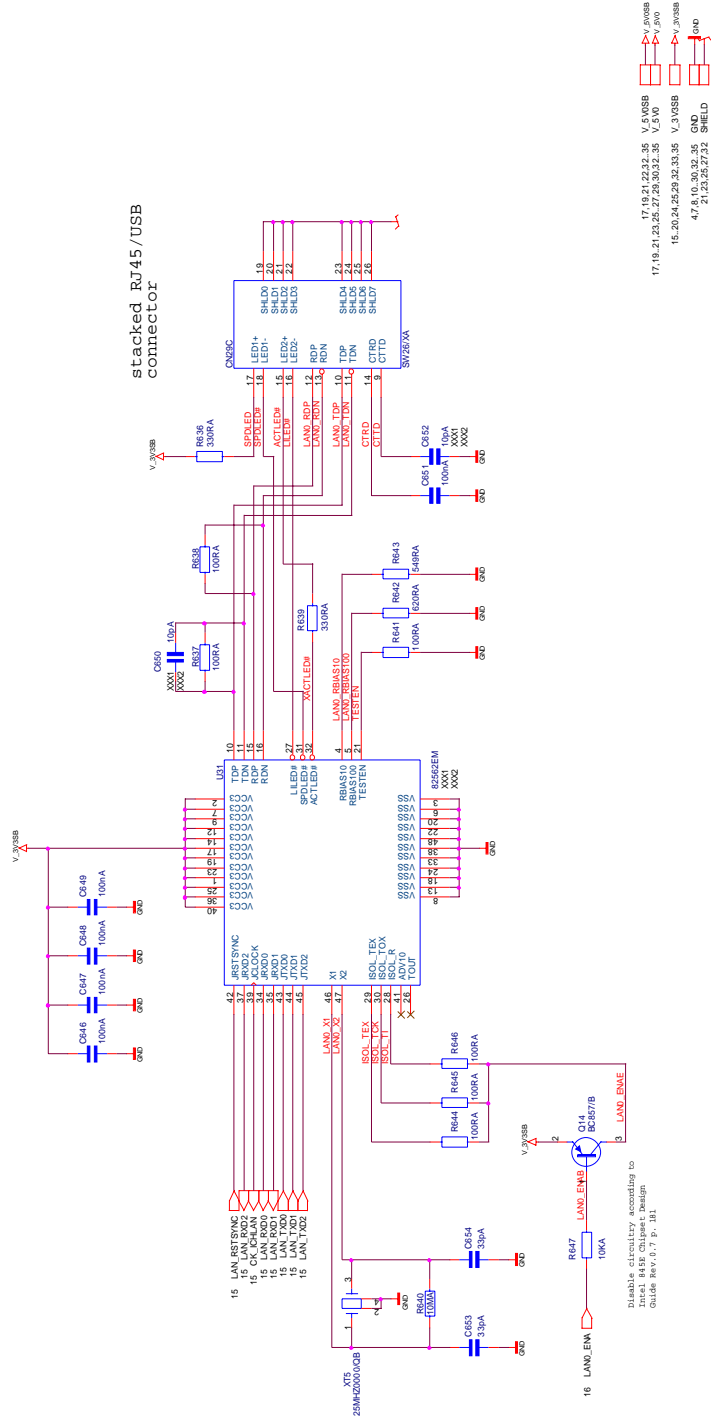
### USB0 & USB1



### LAN0

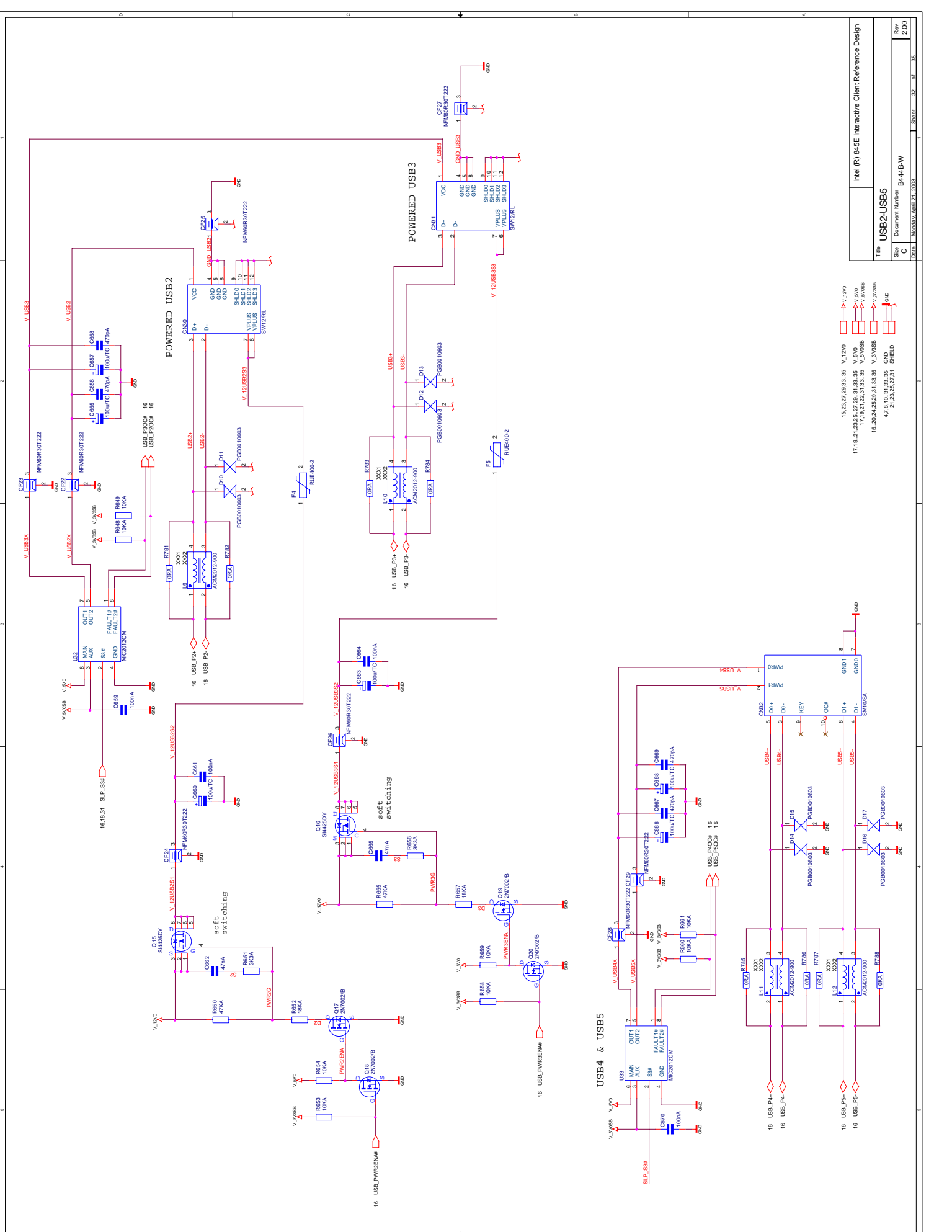


### stacked RJ45/USB connector



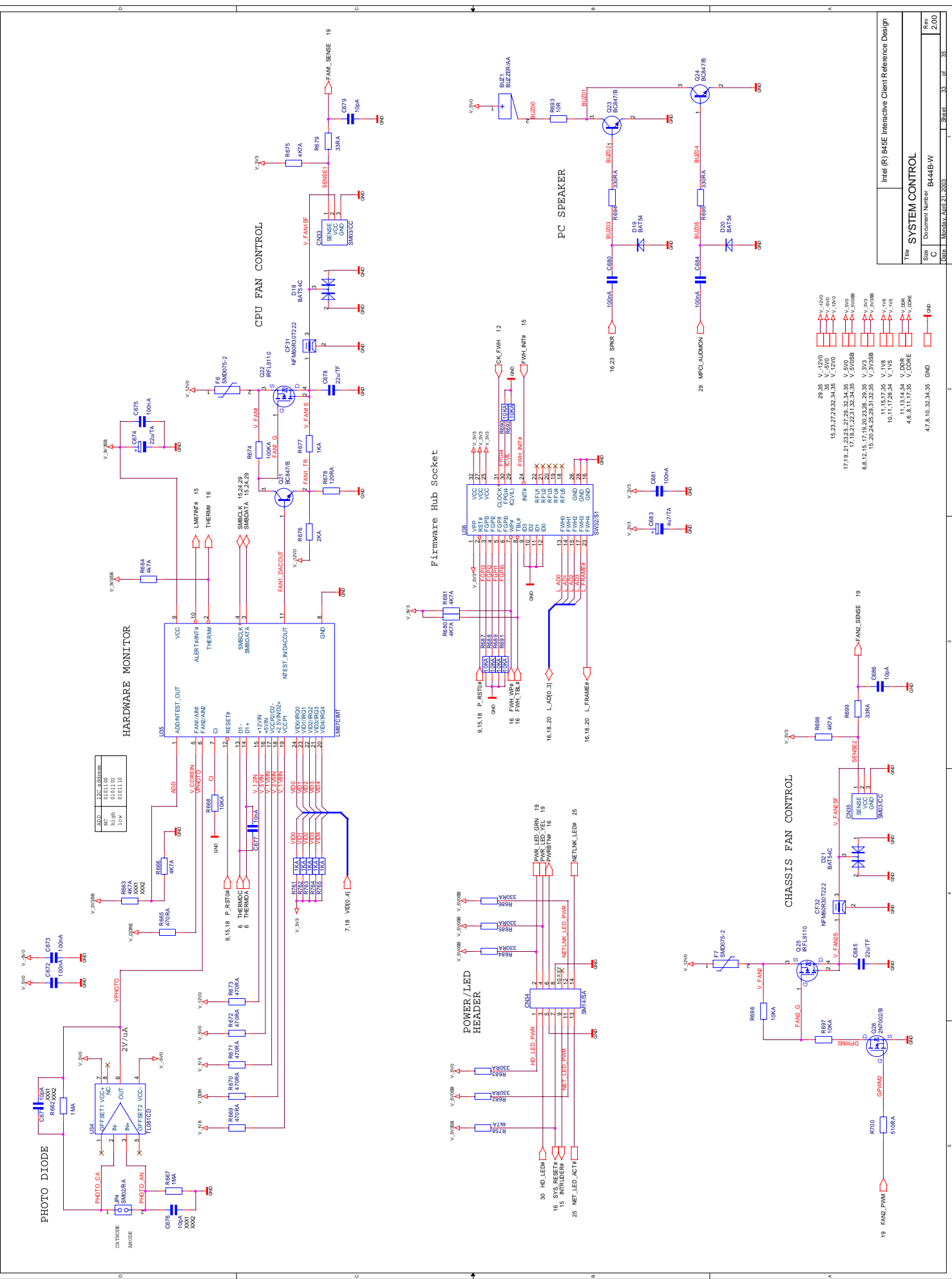
Disable circuitry according to the reference design. Guide Rev.0.7 P. 18.

17	18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34	V_3V3SB	SW25WA
18	19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34	V_2.5M	SW25WA
19	20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34	V_3V3SB	SW25WA
20	21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34	GND	SW25WA
21	22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34	SHIELD	SW25WA



- 15.23.27.2633.35 V\_L200
- 17.19.21.19.19.27.25.3133.35 V\_3VSSB
- 15.20.24.2529.3133.35 V\_3VSSB
- 47.5.10.10.10.33.35 GND
- 4.10.10.10.10.10.10 SHIELD

Intel (R) 845E Interactive Client Reference Design	
Title	USB2-USB5
Size	Document Number B414BW
Date	1/2004, Rev 2.00

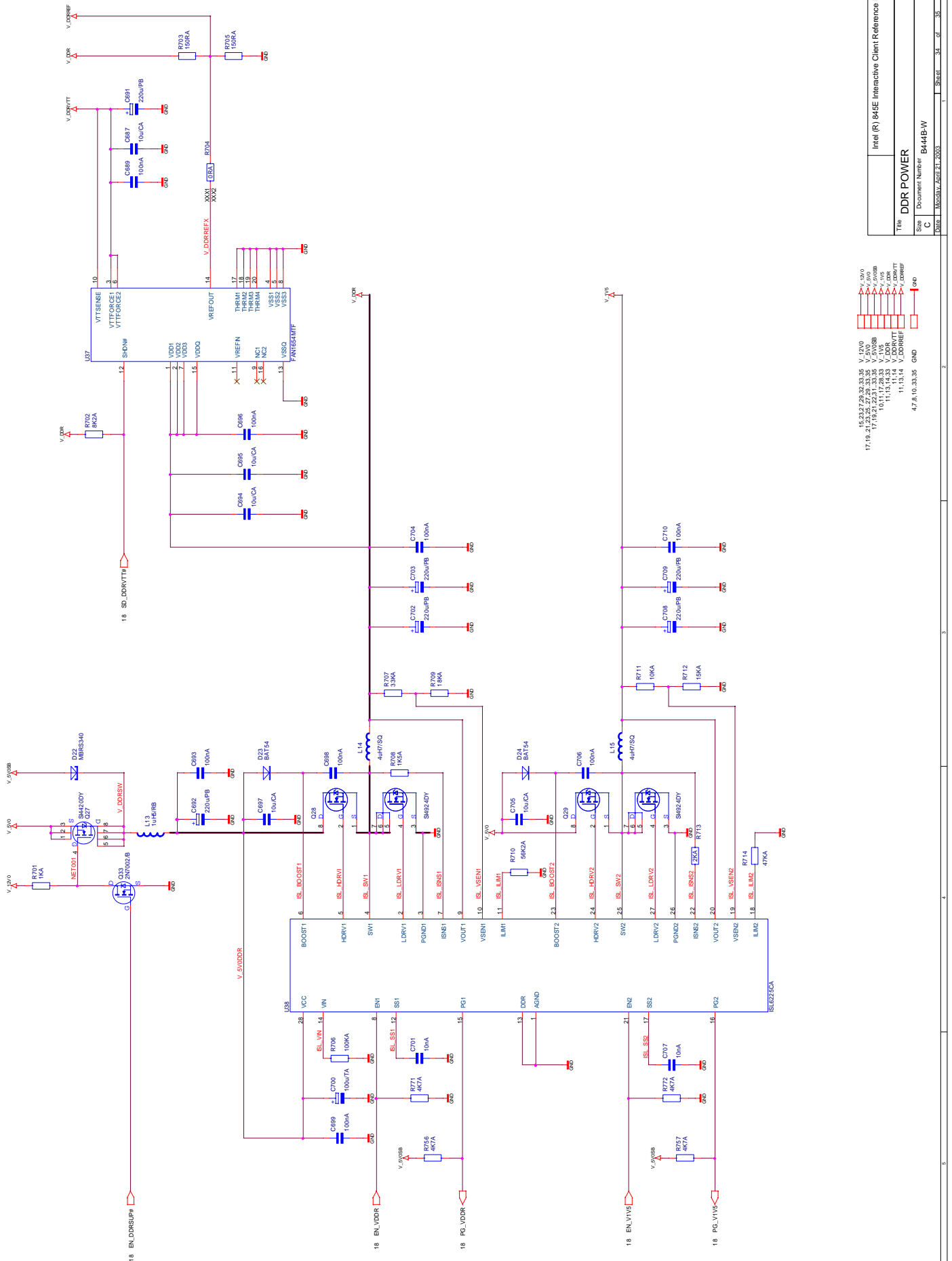


Title		Intel(R) 845E Interactive Client Reference Design
Size	Document Number	B444B/W
Date	Version	1/2000 Rev 2.00

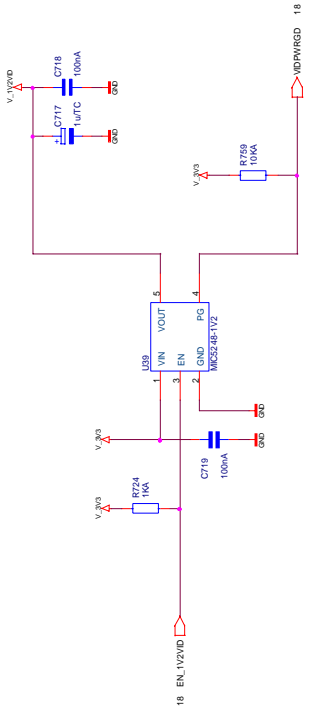
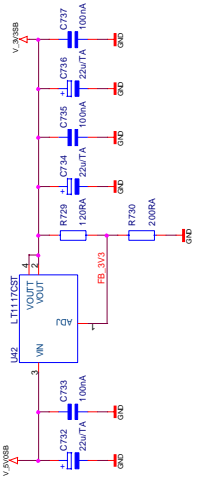
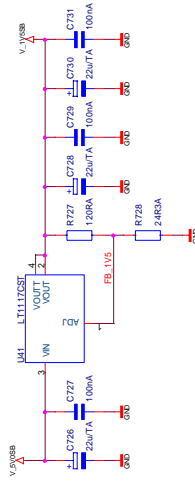
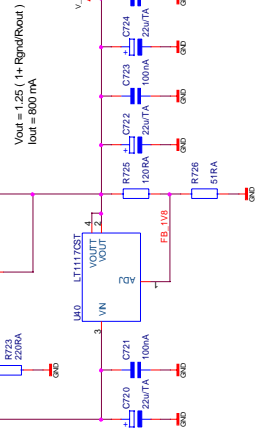
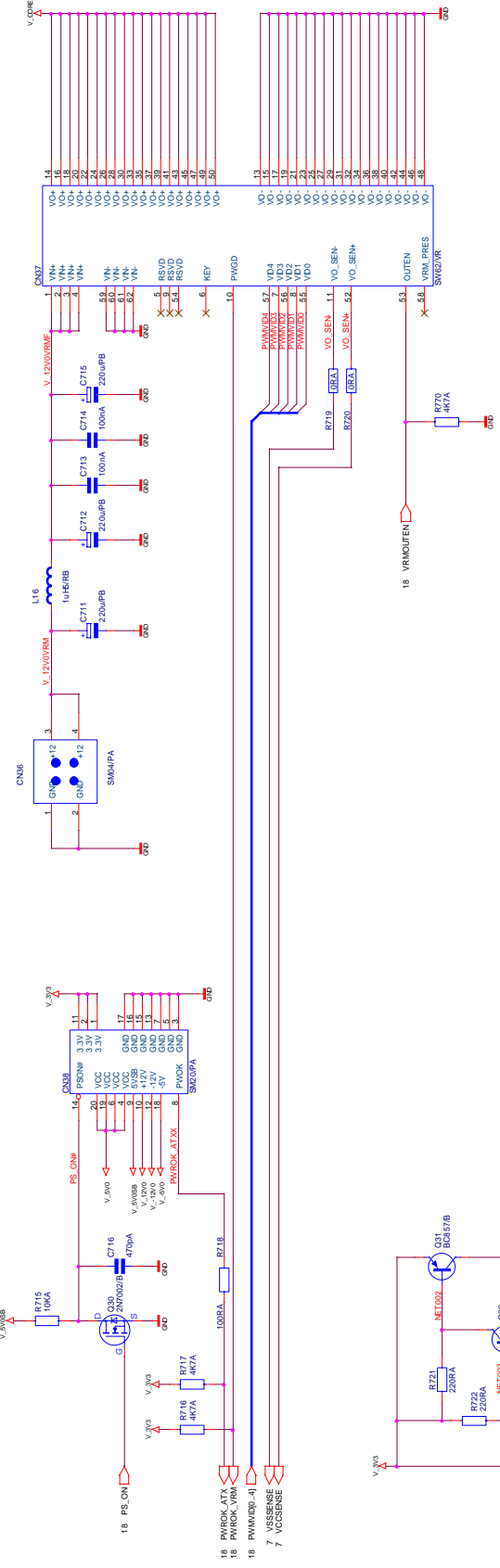
29.35	V <sub>3VSB</sub>	100nA	100nA
29.36	V <sub>5V0</sub>	100nA	100nA
16.23	V <sub>5V0</sub>	100nA	100nA
17.18	V <sub>5V0</sub>	100nA	100nA
17.19	V <sub>5V0</sub>	100nA	100nA
17.20	V <sub>5V0</sub>	100nA	100nA
17.21	V <sub>5V0</sub>	100nA	100nA
17.22	V <sub>5V0</sub>	100nA	100nA
17.23	V <sub>5V0</sub>	100nA	100nA
17.24	V <sub>5V0</sub>	100nA	100nA
17.25	V <sub>5V0</sub>	100nA	100nA
17.26	V <sub>5V0</sub>	100nA	100nA
17.27	V <sub>5V0</sub>	100nA	100nA
17.28	V <sub>5V0</sub>	100nA	100nA
17.29	V <sub>5V0</sub>	100nA	100nA
17.30	V <sub>5V0</sub>	100nA	100nA
17.31	V <sub>5V0</sub>	100nA	100nA
17.32	V <sub>5V0</sub>	100nA	100nA
17.33	V <sub>5V0</sub>	100nA	100nA
17.34	V <sub>5V0</sub>	100nA	100nA
17.35	V <sub>5V0</sub>	100nA	100nA
17.36	V <sub>5V0</sub>	100nA	100nA
17.37	V <sub>5V0</sub>	100nA	100nA
17.38	V <sub>5V0</sub>	100nA	100nA
17.39	V <sub>5V0</sub>	100nA	100nA
17.40	V <sub>5V0</sub>	100nA	100nA
17.41	V <sub>5V0</sub>	100nA	100nA
17.42	V <sub>5V0</sub>	100nA	100nA
17.43	V <sub>5V0</sub>	100nA	100nA
17.44	V <sub>5V0</sub>	100nA	100nA
17.45	V <sub>5V0</sub>	100nA	100nA
17.46	V <sub>5V0</sub>	100nA	100nA
17.47	V <sub>5V0</sub>	100nA	100nA
17.48	V <sub>5V0</sub>	100nA	100nA
17.49	V <sub>5V0</sub>	100nA	100nA
17.50	V <sub>5V0</sub>	100nA	100nA
17.51	V <sub>5V0</sub>	100nA	100nA
17.52	V <sub>5V0</sub>	100nA	100nA
17.53	V <sub>5V0</sub>	100nA	100nA
17.54	V <sub>5V0</sub>	100nA	100nA
17.55	V <sub>5V0</sub>	100nA	100nA
17.56	V <sub>5V0</sub>	100nA	100nA
17.57	V <sub>5V0</sub>	100nA	100nA
17.58	V <sub>5V0</sub>	100nA	100nA
17.59	V <sub>5V0</sub>	100nA	100nA
17.60	V <sub>5V0</sub>	100nA	100nA
17.61	V <sub>5V0</sub>	100nA	100nA
17.62	V <sub>5V0</sub>	100nA	100nA
17.63	V <sub>5V0</sub>	100nA	100nA
17.64	V <sub>5V0</sub>	100nA	100nA
17.65	V <sub>5V0</sub>	100nA	100nA
17.66	V <sub>5V0</sub>	100nA	100nA
17.67	V <sub>5V0</sub>	100nA	100nA
17.68	V <sub>5V0</sub>	100nA	100nA
17.69	V <sub>5V0</sub>	100nA	100nA
17.70	V <sub>5V0</sub>	100nA	100nA
17.71	V <sub>5V0</sub>	100nA	100nA
17.72	V <sub>5V0</sub>	100nA	100nA
17.73	V <sub>5V0</sub>	100nA	100nA
17.74	V <sub>5V0</sub>	100nA	100nA
17.75	V <sub>5V0</sub>	100nA	100nA
17.76	V <sub>5V0</sub>	100nA	100nA
17.77	V <sub>5V0</sub>	100nA	100nA
17.78	V <sub>5V0</sub>	100nA	100nA
17.79	V <sub>5V0</sub>	100nA	100nA
17.80	V <sub>5V0</sub>	100nA	100nA
17.81	V <sub>5V0</sub>	100nA	100nA
17.82	V <sub>5V0</sub>	100nA	100nA
17.83	V <sub>5V0</sub>	100nA	100nA
17.84	V <sub>5V0</sub>	100nA	100nA
17.85	V <sub>5V0</sub>	100nA	100nA
17.86	V <sub>5V0</sub>	100nA	100nA
17.87	V <sub>5V0</sub>	100nA	100nA
17.88	V <sub>5V0</sub>	100nA	100nA
17.89	V <sub>5V0</sub>	100nA	100nA
17.90	V <sub>5V0</sub>	100nA	100nA
17.91	V <sub>5V0</sub>	100nA	100nA
17.92	V <sub>5V0</sub>	100nA	100nA
17.93	V <sub>5V0</sub>	100nA	100nA
17.94	V <sub>5V0</sub>	100nA	100nA
17.95	V <sub>5V0</sub>	100nA	100nA
17.96	V <sub>5V0</sub>	100nA	100nA
17.97	V <sub>5V0</sub>	100nA	100nA
17.98	V <sub>5V0</sub>	100nA	100nA
17.99	V <sub>5V0</sub>	100nA	100nA
18.00	V <sub>5V0</sub>	100nA	100nA

4.7,8,10,32,34,35 GND





15, 27, 29, 33, 35 V<sub>DDQ</sub>  
 17, 19, 21, 23, 25, 27, 29, 33, 35 V<sub>DDO</sub>  
 17, 19, 21, 23, 25, 27, 29, 33, 35 V<sub>DDREFB</sub>  
 11, 13, 17, 19, 23, 33 V<sub>DDREFC</sub>  
 11, 13, 14, 33 V<sub>DDREFD</sub>  
 11, 13, 14, 33 V<sub>DDREFE</sub>  
 11, 13, 14 V<sub>DDREFG</sub>  
 11, 13, 14 V<sub>DDREFH</sub>  
 11, 13, 14 V<sub>DDREFI</sub>  
 11, 13, 14 V<sub>DDREFJ</sub>  
 11, 13, 14 V<sub>DDREFK</sub>  
 11, 13, 14 V<sub>DDREFL</sub>  
 11, 13, 14 V<sub>DDREFM</sub>  
 11, 13, 14 V<sub>DDREFN</sub>  
 11, 13, 14 V<sub>DDREFO</sub>  
 11, 13, 14 V<sub>DDREFP</sub>  
 11, 13, 14 V<sub>DDREFQ</sub>  
 11, 13, 14 V<sub>DDREFR</sub>  
 11, 13, 14 V<sub>DDREFS</sub>  
 11, 13, 14 V<sub>DDREFT</sub>  
 11, 13, 14 V<sub>DDREFU</sub>  
 11, 13, 14 V<sub>DDREFV</sub>  
 11, 13, 14 V<sub>DDREFW</sub>  
 11, 13, 14 V<sub>DDREFX</sub>  
 11, 13, 14 V<sub>DDREFY</sub>  
 11, 13, 14 V<sub>DDREFZ</sub>  
 47, 8, 10, 33, 35 GND



4.6, 8.11, 17.33	V_CODE	1
7	V_1V2V0	2
17	V_1V5S8	3
17, 18, 21, 22, 23, 24, 25, 26, 29, 33	V_3V3	4
15, 16, 20, 25, 26, 29, 31, 33	V_3V0S8	5
17, 18, 21, 22, 23, 24, 25, 27, 28, 34	V_3V0	6
17, 18, 21, 22, 23, 24, 25, 27, 28, 34	V_5V0S8	7
17, 18, 21, 22, 23, 24, 25, 27, 28, 34	V_5V0	8
17, 18, 21, 22, 23, 24, 25, 27, 28, 34	V_12V0	9
47, 8, 10, 34	GND	10