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Intel® Pentium® 4 Processor and Intel® 852GME Chipset

Platform Design Guide Addendum

For use with Intel® Celeron® D Processor in the 478-pin package

July 2004

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Revision History

Revision Number	Description	Revision Date
1.0	Initial Release	July 2004

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1   Introduction

This document describes the required changes to platforms utilizing the Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 micron process to support a migration to the Intel® Celeron® D Processor in the 478-pin package. The information in this document should be used in conjunction with specifications presented in the latest version of the *Intel® Celeron® D Processor 335, 330, 325 and 320 Datasheet* and *Intel®Pentium®4 Processor with 512-KB L2 Cache on 0.13 Micron Process Datasheet.*

This design guide addendum is applied as a supplement to the platform design guidelines listed in Section 1.2. This document highlights changes to the platform design guidelines for the purpose of adding Intel® Celeron® D Processor in the 478-pin package support to the platform. All other design implementation details from the platform design guidelines are applicable for Intel Celeron® D Processor in the 478-pin package support, given the limitations described in Section 2.

1.1   State of the Data

This document contains compatibility requirements between the Intel® Celeron® D Processor in the 478-pin Package and the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process with the 852GME chipset family based platforms.

The board-level electrical design changes (system bus routing recommendations, new signal definition, system bus termination recommendations, etc.) are the best-understood design details to date for the Intel Celeron D in the 478-pin package. This includes the pinout changes and their implementation in the "compatible platform." Refer to Section 1.3 for a definition of a compatible platform.

1.2   References

Material and concepts available in the following documents may be beneficial when reading this document:

Table 1. References

Document	Document Number
Intel® Celeron®D Processors 335, 330, 325, and 320 Datasheet	http://www.intel.com/design/celeron/datashts/302353.htm
Intel® Pentium® 4 Processor and Intel® 852GME Chipset Platform Design Guide	http://developer.intel.com/design
Intel® Pentium® 4 Processor with 512-KB L2 Cach on 0.13 Micron Process and Intel® Pentium® 4 Processor Extreme Edition Supporting HyperThreading Technology Datasheet	http://www.intel.com/design/Pentium4/datashts/298643.htm
Intel®Pentium®4 Processor in the 478-pin Package Thermal Design Guidelines	http://developer.intel.com/design
Intel® Celeron® D Processor for Embedded Applications Thermal Design Guide	http://www.intel.com/design/intarch/designgd/302647.htm
Intel®Pentium®4 Processor VR-Down Design Guidelines	http://developer.intel.com/design/ Pentium4/guides/249891.htm
Voltage Regulator-Down (VRD) 10.0 Power Delivery Design Guide	http://developer.intel.com/design/ Pentium4/guides/252885.htm
Intel® Architecture Software Developer's Manual	
Volume 1: Basic Architecture	http://www.intel.com/design/Pentium4/manuals/253665.htm
Volume 2A: Instruction Set Reference A-M	http://developer.intel.com/design/pentium4/manuals/253666.htm
Volume 2B: Instruction Set Reference N-Z	http://developer.intel.com/design/pentium4/manuals/253667.htm
Volume 3: System Programming Guide	http://developer.intel.com/design/pentium4/manuals/253668.htm
ITP700 Debug Port Design Guide	http://developer.intel.com/design/ Xeon/guides/249679.htm

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1.3   Definitions

- **Intel® Celeron® D Processor in the 478-pin Package** - Intel 32-bit microprocessor intended for desktop platforms. The Celeron D processor the 478-pin package, is based on a new 90 nm process and will include core frequency improvements, microarchitectural improvements and additional instructions. The Celeron D processor in the 478-pin package uses the 478-pin socket.

- **Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process** - The Pentium 4 processor with 512-KB L2 cache on 0.13 micron process is the second-generation processor based on Intel NetBurst microarchitecture. It is based on the 0.13 micron process and has a 512-KB L2 cache.

- **Compatible Platform** - For the purpose of this document, a compatible platform is an 852GME chipset-based design, originally built to support the Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 micron process, and has been modified to add support for the Intel® Celeron® D Processor in the 478-pin package. The compatible platform should implement the design guidelines listed in this document including VRD10.0 design requirements, changes in processor circuits, system bus pin changes, and support the Celeron D processor in the 478-pin package.

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2 Compatibility Overview

Implementing the changes outlined in this document will assist in making an Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 micron process-based system design compatible with the Intel® Celeron® processor on 90 nm process and in the 478-pin package. Compatibility will ultimately be limited by factors such as the ability of the system to supply the required current for the Intel® Celeron® D Processor, maintaining the processor power supply within the voltage tolerances specified for the Intel® Celeron® D Processor, and adequate system cooling capability. This design guideline is used as a supplement to the standard platform design guidelines and is used only when designing in support for the Intel® Celeron® D Processor in the 478-pin package.

Put reference of the EID design guide

2.1 Power Delivery

VRD 10.0 is recommended for the power delivery for the Intel® Celeron® D Processor in the 478-pin package.

2.2 System Bus Design

Supporting the Intel® Celeron® D processor in the 478-pin package will require some 478-pin socket signal definition changes as well. The changes will not interfere with the proper operation of the Pentium 4 processor with 512-KB L2 cache on 0.13micron process. Refer to Section 6.1 for the details on the pinout changes.

Bus lengths and routing strategies for the 533 MHz system bus should remain unchanged from the recommendations provided in the platform design guide.

2.3 Thermal - Mechanical Design

The same mechanical retention solution employed for a Pentium 4 processor with 512-KB L2 cache on 0.13 micron process will be appropriate for use with the Intel Celeron D processor in the 478-pin package at frequencies intended for the compatible design. Heatsinks designed to support the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process processor FMB2 requirements will support Intel® Celeron® D processor in the 478-pin package requirements. Refer to Section 7 for details on the thermal - mechanical design changes.

2.4 BIOS Support

There will be BIOS-level changes required to support the Intel® Celeron® D Processor in the 478-pin package. Please contact your local Intel Field Representative to get the latest micro code update.

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3 Power Delivery Changes

The compatible platform should meet the FMB2 requirements of the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process and the Intel® Celeron® D processors in the 478-pin package requirements. To support this feature the compatible platform should meet the requirements of the Voltage Regulator-Down 10.0 Design Guidelines. Designs will continue to utilize the power delivery guidelines outlined in the platform design guideline, along with the additional requirements recommended in this section. This includes layout and decoupling recommendations found in the platform design guidelines.

Table 2. Intel® Celeron® D Processor in the 478-Pin Package FMB Guideline

	Intel® Pentium® 4 Processor with 512 KB L2 cache on 0.13 Micron Process FMB2	Intel® Celeron® D processor in the 478-Pin Package
IccMax	70 A	73 A
VRD (Dual Loadline)	10.0	10.0
Icc Sustained	N/A	62A
Power (TDP)	82 W	73 W
Max T_C	70 °C	67 °C
Ta	42 C	42 C

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3.1 Decoupling Requirements

Table 3. Decoupling Requirements Table (for Intel® Celeron® D Processor in the 478-Pin Package)[3]

Capacitance	ESR (each)	ESL (each)	Filter	Notes
(10) AL Polymer 560 µF	5mW	4nH	Output	1
(40) 1206 pkg 22µF X5R	3.5mW	1.4nH	Output	1, 2
(4) AL Electrolytic 1200 µF 16V 2.1A Ripple	22mW	30nH	Input	1
(4) 1206 pkg 4.7µF	6mW	1.1nH	Input	1

NOTES:
1. The ESR, ESL, and ripple current values in this table are based on the values used in power delivery simulations used by Intel, and they are not vendor specifications.
2. The decoupling should be placed as close as possible to the processor pins. This table details the recommendation values. For placement details, please refer to Chapter 4 of the Pentium® 4 Processor and Intel® 852GME Chipset Platform Design Guide. The voltage regulator designer should ensure that an adequate amount of decoupling is present such that the circuit meets the processor specifications.
3. Supports both the Pentium 4 processor on 0.13 micron process and the Celeron D processor.

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4 Processor Circuits

The following chapter outlines all system bus pinout changes that are required for platforms intending to support the Intel® Pentium 4 processor with 512-KB L2 cache on 0.13 micron process processor as well as the Intel® Celeron® D processor.

4.1 Bi-Directional PROCHOT#

Intel recommends that the compatible system boards be designed to support the Intel® Celeron® D processor in the 478-pin package. These guidelines include an ICC_MAX and a VR_TDC (VR Thermal Design Current). The processor voltage regulator (VR) solution should be designed to support ICC_MAX electrically for brief time periods. The voltage regulator solution should also be designed to support a minimum of VR_TDC indefinitely within the envelope of operating conditions of the system. The VR_TDC limits of the system board are typically governed by the system board thermal limits. Intel recommends that system boards designed to the above guidelines implement a VR thermal monitor circuit.

Figure 1. Bi-Directional PROCHOT# Circuit
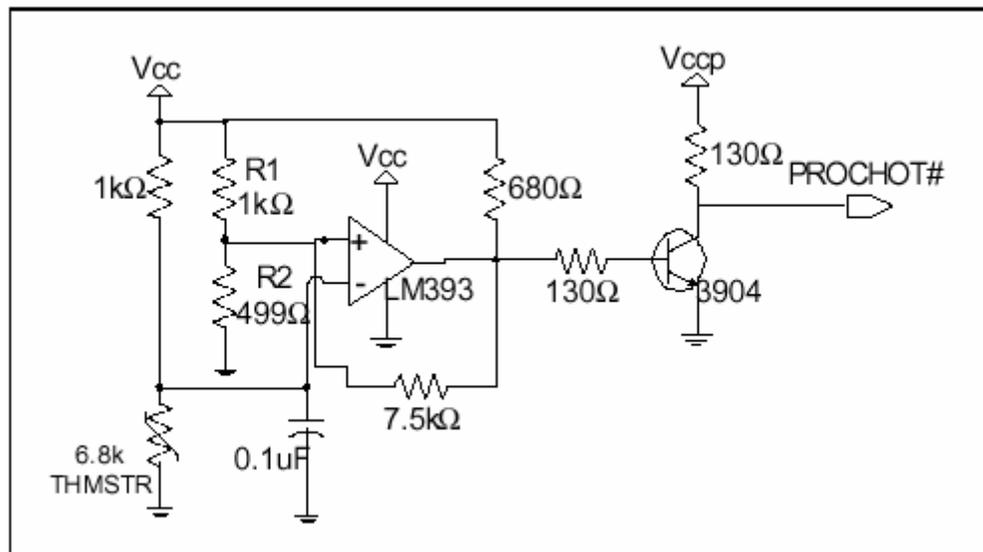
For this circuit implementation, the thermistor (THMSTR) should be placed in the hottest area of the VR. As the thermistor heats up, its resistance goes down. This creates an error voltage based on the resistance of the thermistor and the voltage reference provided by R1 and R2. The values of R1 and R2 should be adjusted to calibrate the circuit for a specific system board design so that it asserts PROCHOT# when the VR reaches its thermal limit. The values of R1 and R2 in Figure 2 are included as an example. The value of R2 is adjusted to calibrate the circuit so that PROCHOT# is asserted when the VR reaches its thermal limit in the system that it is intended to operate in. An adequate VR cooling solution should be implemented such that VR_TDC current levels can be maintained indefinitely.

4.2 Dual Loadline Implementation (VRD 10.0)

The Intel® Celeron® D processor in the 478-pin package and the Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 micron process have different loadline requirements. Therefore, the VRD 10.0 controller must switch feedback networks depending on which processor is installed. The BOOTSELECT signal is used by the VRD to detect whether an Intel® Celeron® D processor in the 478-pin package or Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 micron process is inserted into the processor socket and switches the feedback network. Figure 3 shows a diagram of the switching network, while Figure 4 shows an example of the switching circuit.

Figure 2. VRD Feedback Switching Diagram
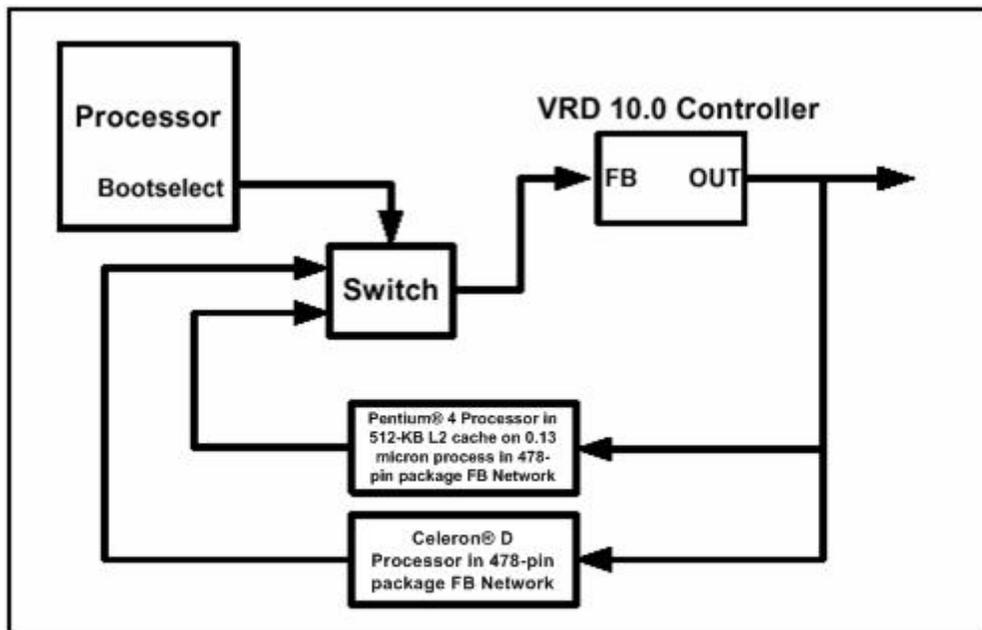
Figure 3. Routing Illustration for BOOTSELECT
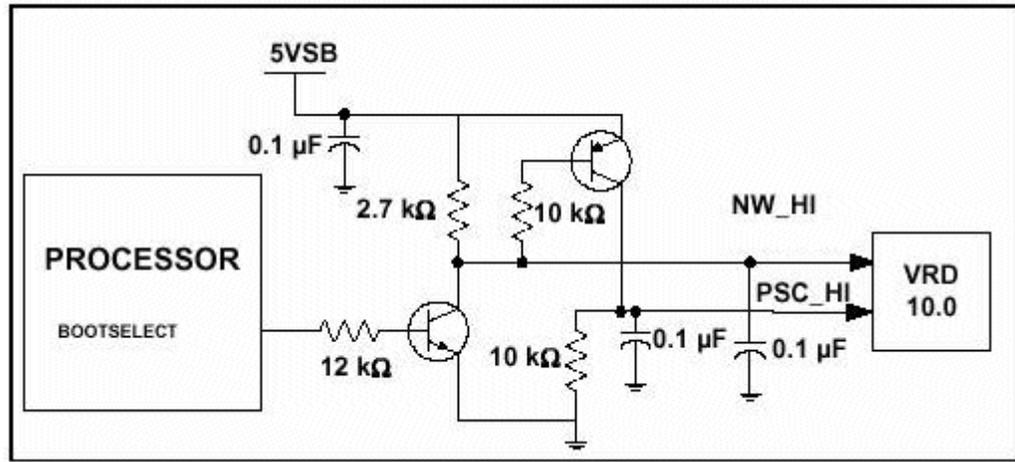
4.3 SYS_RESET# Timing Circuitry

If re-starting the system after a shutdown caused by a catastrophic thermal event (THERMTRIP# event) and in order to protect the Intel® Celeron® D processor in the 478-pin package during the reset state, there are two reset timing requirements, that have to be met; CPUPWRGD active to CPURST inactive, and VCC_CPU active to CPUPWRGD assertion.

The front panel reset switch (FP_RST #) is connected to SYS_RESET# to reset the whole system. The reset timing may violate the system stability conditions. To prevent this condition, the following two schematics are recommended to generate a 20 ms ± 20%, pulse reset signal.

Figure 4. Reset Timing Circuit - 1
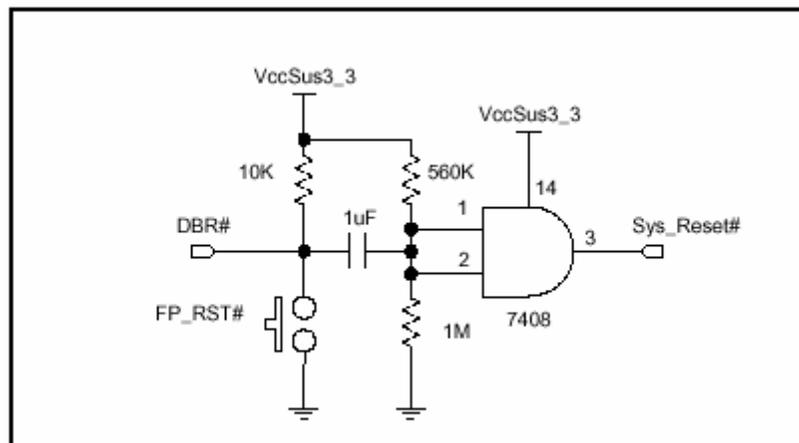
Figure 5. Reset Timing Circuit - 2
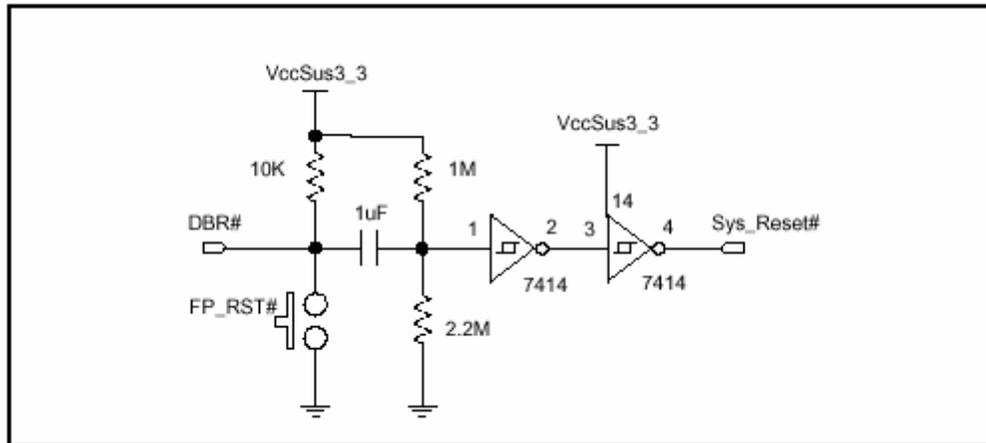
4.4 INIT# Signal Topology

The recommended logic circuit for level shifting the INIT# signal has changed. The lower processor VID has led to changes in the circuit and input resistor values.

Figure 6. Voltage Translation of INIT#
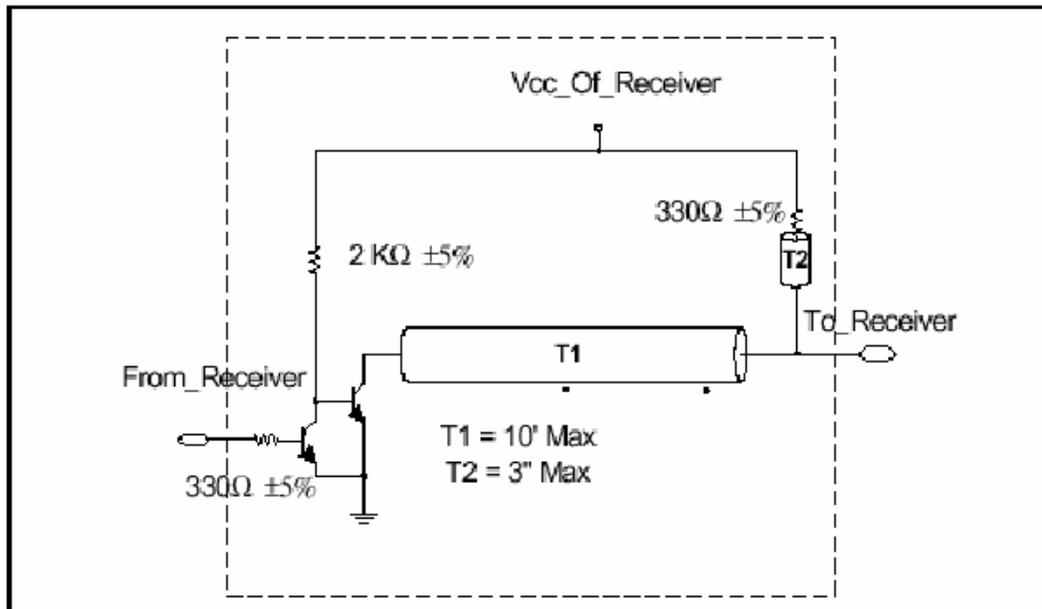
5 BIOS Support

5.1 Microcode Updates

The Intel® Celeron® D processor in the 478-pin package will use variable size microcode updates (as large as 16K bytes in size) that compliant with the new INT 15h Variable Size Microcode Update Specification. For the latest Microcode Update, please contact your local Intel Representative.

5.2 Processor Identification

The Intel® Celeron® D processor in the 478-pin package will not support the Brand ID feature of the CPUID instruction as method of processor identification. The BIOS should use Brand String feature of the CPUID instruction as the preferred processor identification mechanism.

6 System Bus Design Changes

6.1 Pinout Changes

There are several new signal assignments - some of which are required for platforms supporting the Intel® Celeron® D processor in the 478-pin package - from the pinout defined by the current Pentium 4 processor with 512-KB L2 cache on 0.13 micron process. The platform must be designed with the 478-pin socket in order to mechanically support the Intel® Celeron® D processor in the 478-pin package.

Table 4. 478-Pin Socket Pin-Map Changes

Pin	Old Name 1	New Name 2	Signal Group 2
AD3	RESERVED	VID5	Output
AF3	RESERVED	VCCVIDLB	Power/Other
AD2	RESERVED	VIDPWRGD	Power/Other
AE26	Vss	OPTIMIZED/COMPAT#	Input
AD1	Vss	BOOTSELECT	Input

NOTES:
1. Definition associated with the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process.
2. Definition associated with the Intel® Celeron® D processor in the 478-pin package. These new pin definitions do not interfere with the proper operation of the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process.

6.1.1 Pinout Definitions and Implementation Details

This section provides specific changes to the processor pinout to migrate a design from supporting only the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process to one supporting the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process and the Intel® Celeron® D processor in the 478-pin package. Only those pinout changes mark as "Required Platform Changes" must be implemented by the platform and impact the connectivity of the 478-pin socket pinout.

6.1.1.1 VID5 (VRD 10.0)

The compatible platforms should connect the VID5 pin to the VRD 10.0. A pull-up resistor of 1 kΩ to a 3.3 V, or less, supply is required.

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6.1.1.2 VCCVID and VCCVIDLB (Required Platform Change, VRD 10.0)

For platforms that were designed to support only the Intel® Pentium® 4 Processor, the VCCVID output is tied to a 1.2-V linear regulator on the platform. This regulator provides the power to the processor logic responsible for driving the VID[5:0] and the BSEL[1:0] outputs. The compatible platform must connect the VCCVID pin to the VCCVIDLB pin. A 5-mil trace is acceptable to connect these pins. The current specification for the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process VCCVID supply is 30 mA. In order to support the Intel® Celeron® D processor in the 478-pin package, a linear regulator that can supply at least 150 mA should be used.

Note: **VCCVID and VCCVIDLB pins need to be tied together, and the 1.2 V is required to be supplied to the VCCVID (AF4) and VCCVIDLB (AF3) pin.**

6.1.1.3 VIDPWRGD (VRD 10.0)

VIDPWRGD should be pulled up to 1.2V VCCVID through a 680 Ω resistor. The VIDPWRGD pin does not have an on die pull-up resistor, and should follow the timing and voltage requirements below:

Table 5. VIDPWRGD Specifications

VIDPWRGD	Min	Max
Input Low Voltage (V_{IL})	–	0.3 V
Input High Voltage (V_{IH})	0.9 V	–
Falling Edge Voltage (V_T)	–	0.95 V
Rise Time -	–	150 ns

NOTE: In these specifications differ from the Intel® Celeron® D Processor in the 478-pin Package datasheet, the datasheet supersedes.

6.1.1.4 Optimized/Compat# pin (VRD 10.0)

The OPTIMIZED/COMPAT# input informs the processor about the type of platform the processor is installed. This signal must be connected to Vss to signify that the platform offers compatibility with the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process. This signal must use a 60 Ω pull-down resistor to connect to Vss.

6.1.1.5 BOOTSELECT

Please refer to Section 4.2 of this document for BOOTSELECT information.

7 Thermal - Mechanical Changes

The *Intel® Celeron® D processor for Embedded Applications Thermal Design Guide* document will contain the latest information on the Intel reference solution and the enabled retention mechanism.

The Intel® Celeron® D processor in the 478-pin package is identical to the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process package except for a slight difference in total package height, defined as the distance from the bottom of the substrate to the top of the integrated heat spreader (IHS). The table below provides a comparison between the two processor package heights. Currently, the package height change has been determined to have no impact on the existing Intel reference thermal and mechanical solution. Customers planning on re-using their Pentium 4 processor with 512-KB L2 cache on 0.13 micron process thermal and mechanical solutions for the Intel® Celeron® D processor in the 478-pin package should consider the package height change and ensure that their designs have adequate performance over the package height range.

The dimensions for the bottom-side component keep-out zones have been slightly changed for the Intel® Celeron® D processor in the 478-pin package. The zone dimension for the Intel® Celeron® D processor in the 478-pin package is 1.5 mm [0.059 in] while the dimension for the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process is 1.25 mm [0.049 in]. Any components mounted on the motherboard in the socket center opening must not intrude into this keep-out zone underneath the processor package.

Refer to the Intel® Pentium® 4 Processor on 90 nm Process Thermal Design Guidelines or Intel® Celeron® D Processor for Embedded Applications Thermal Design Guidelines for additional information. Locations of these documents can be found in Section 1.2.

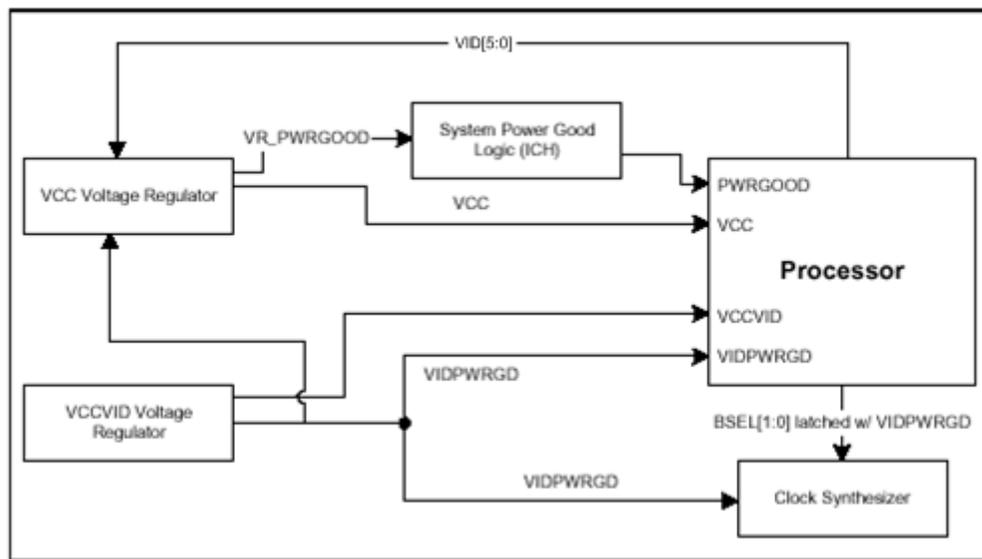**Table 6. Intel® Celeron® D Processor in the 478-pin package Height Comparison**

	Intel® Celeron® D Processor in the 478-Pin Package	Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process
Minimum Package Height	3.308 mm [0.130 in]	3.246 mm [0.128 in]
Maximum Package Height	3.848 mm [0.151 in]	3.670 mm [0.144 in]

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8   Other Platform Considerations

8.1   Power Sequencing

In order to support the Intel® Celeron® D processor in the 478-pin package there are some additional power sequencing requirements. This is mainly due to the addition of a VIDPWRGD input to the Intel® Celeron® D processor in the 478-pin package. This input is designed to indicate when the VCCVID voltage is stable and the processor is able to drive the VID[5:0] outputs. The block diagram seen in Figure 6 is an example implementation.

Figure 6. Voltage Sequence Block Diagram

8.2   System Bus Signal Levels

The estimated value for the VID code of the Intel® Celeron® D processor in the 478-pin package is 1.25 V to 1.40 V. The current VID value for VCC of the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process is 1.475 to 1.550 V. The specific values will be determined as the processors are fully characterized. For the latest processor specifications, refer to the *Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Datasheet* and *the Intel® Celeron® D Processo in the 478-pin Package Datasheet.*

Table 7 outlines AGTL+ signal level definition differences between the Intel® Celeron® D processor in the 478-pin package and the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process. I/O buffer models are available for the Intel® Celeron® D processor in the 478-pin package, simulation should be performed for the system bus interface to ensure that these

levels are met. Other bus electrical characteristics are expected to be compatible with the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process specifications.

Because the system bus is terminated to the processor's power supply, all chipset devices and other logic tied to the system bus must be capable of operating within the voltage ranges associated with the Intel® Celeron® D processor in the 478-pin package and Pentium 4 processor with 512-KB L2 cache on 0.13 micron process. Refer to Table 7 for estimated voltage ranges of these processors.

Table 7. System Bus Voltage Estimates

Processor	VID	VCC Max 2	VCC Min 2	GTLREF Max	GTLREF Min	Notes
Intel® Celeron® Processor on 90 nm Process and in the 478-pin Package	1.25 to 1.4	Note 2	Note 2	2/3 * V $_{CC}$ + 2%	2/3 * V $_{CC}$ - 2%	1
Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 Micron Process	1.475 to 1.550	Note 2	Note 2	2/3 * V $_{CC}$ + 2%	2/3 * V $_{CC}$ - 2%	1

NOTES:
1. These values are for reference only. The processor datasheet contains the actual specifications for the processor. If the specifications in this table conflict with the specifications found in the datasheet, the datasheet supersedes.
2. VCC minimum and maximum specifications are processor core frequency specific. VCC maximum is dependent on ICC for a given frequency. VCC minimum is rated at any ICC value for a given frequency. Please refer to the latest processor datasheet for the values.

Any platform logic that connects to system bus signals must be compatible with the lower voltages of the Intel® Celeron® D processor in the 478-pin package and must tolerate the lower reference point if the logic connects to AGTL+ system bus signals.

8.3   Voltage Tolerance for Special Signals

There are two groups of Intel® Celeron® D processor in the 478-pin package signals that will have a higher voltage tolerance to ease compatibility with components enabled for the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process. The VID[5:0] and BSEL[1:0] outputs are designed to tolerate a pull up voltage of up to 3.3 V. This allows Intel® Celeron® D processor in the 478-pin package to be used with existing clock synthesizers and voltage regulators that pull these signals up to a 3.3 V power supply.

8.4   Designing to Support Debug Tools

Intel strongly recommends that platforms be designed to support run time control tools, such as the Intel in-target probe (ITP), and logic analyzer interfaces. These tools can greatly reduce the time required to troubleshoot platform, BIOS, and application issues.

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8.4.1 Run Time Control Tools

Existing run time control tools, like the ITP, are able to support the Intel® Celeron® D processor in the 478-pin package with only a software update.

8.4.2 Logic Analyzer Interface

Initial debug of a compatible platform utilizing the Celeron® D processor in the 478-pin package is supported by current LAIs for the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process.