495-PIN AND 615-PIN MICRO-PGA ZIF SOCKET DESIGN SPECIFICATION

Application Note

October 5, 1999

Order Number: 245284-001

Contents

1. INTRODUCTION

This document defines the SMT ZIF (Zero Insertion Force) socket that will support the 615-pin Micro-PGA and 495-pin Micro-PGA mobile processor packages. The 615-pin Micro-PGA and 495-pin Micro-PGA sockets must be low cost, low risk, robust, reliable, manufacturable in high volumes, and multi-sourceable. The 615-pin Micro-PGA mobile socket has 615 contacts with a pitch of 1.27 mm that mates with a 615-pin Micro-PGA package. The 495-pin Micro-PGA mobile socket has 495 contacts with a 1.27 mm pitch that mates with the 495-pin Micro-PGA package.

1.1. Purpose

To define the mechanical, electrical, quality, and reliability requirements necessary to meet the product requirements of the 615-pin Micro-PGA and 495-pin Micro-PGA mobile processor package ZIF sockets.

1.2. Scope

This specification applies to all ZIF sockets designed for use with the Intel mobile processor 495-pin and 615-pin Micro-PGA packages.

2. PACKAGE DESCRIPTION

Information provided in this section is to ensure dimensional compatibility of the 615-pin Micro-PGA and 495-pin Micro-PGA sockets with the corresponding packages. The 615-pin Micro-PGA and 495-pin Micro-PGA packages must be insertable into the sockets with zero insertion force when the socket is not actuated.

2.1. Package Layout

The outline of the packages that can be used with the 615-pin Micro-PGA and 495-pin Micro-PGA sockets are illustrated in **Figures 1 and 2**.

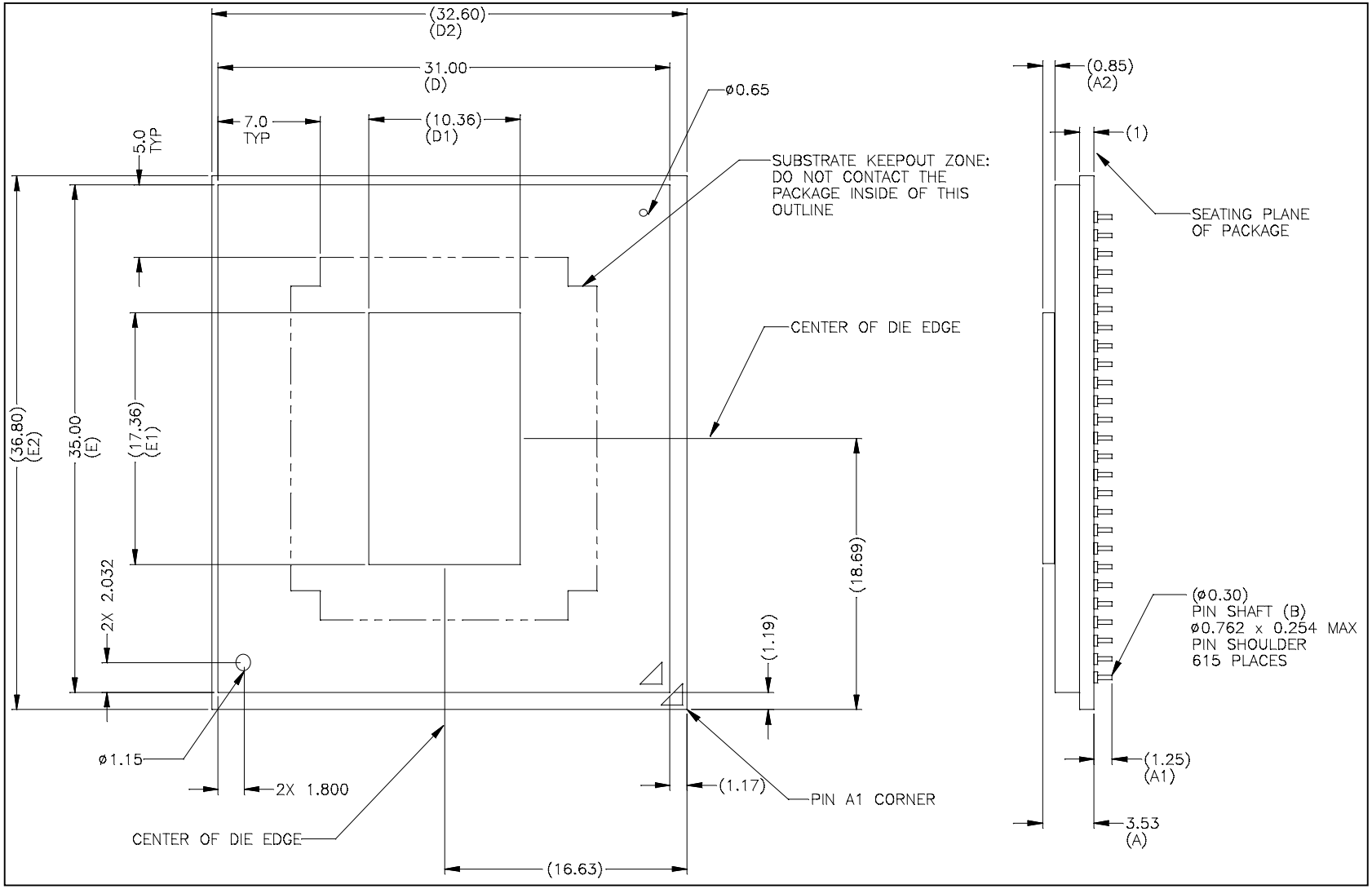
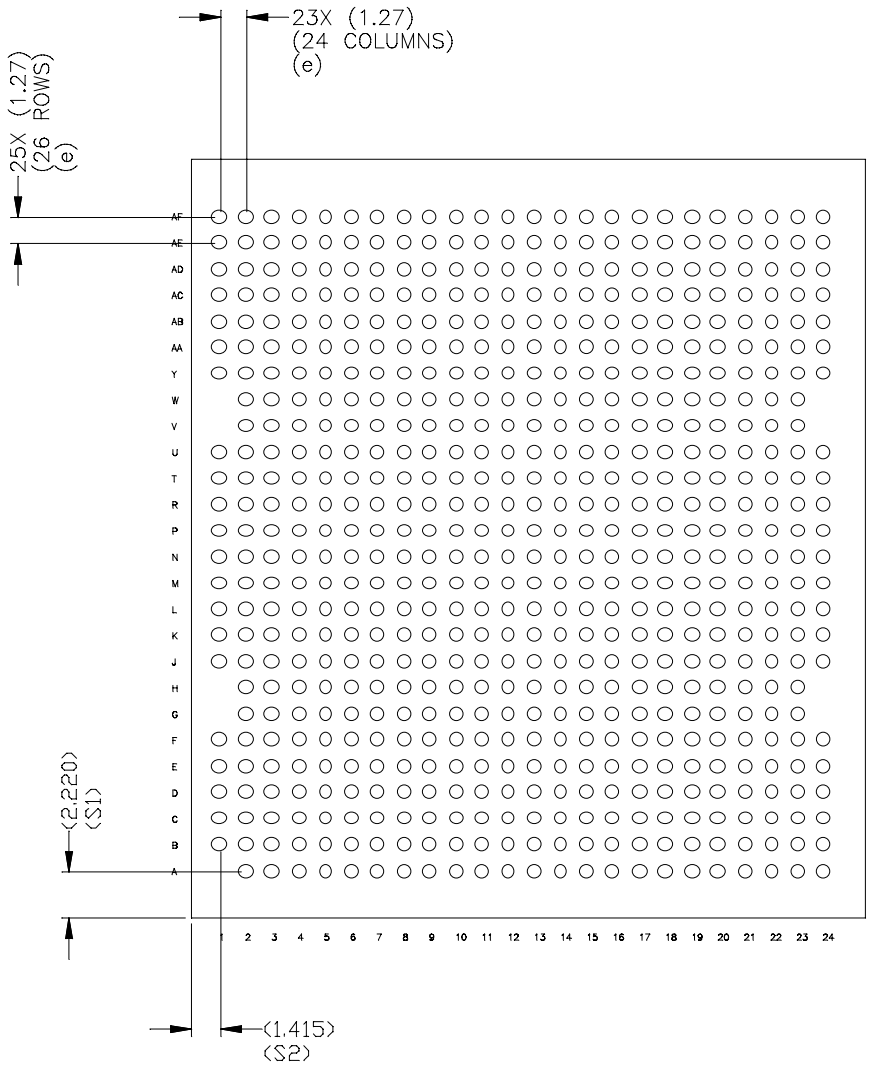


Figure 1a: 615-pin Micro-PGA package top and side view (see Figure 1b for package dimension).



Symbol	Parameter	Min	Max	Unit
A	Overall height, top of die to seating plane of interposer	3.23	3.83	mm
-	Overall height, top of die to PCB surface, including socket(1)	5.40	6.00	mm
A1	Pin length	1.25		mm
A2	Die height	0.854		mm
B	Pin diameter	0.3		mm
D	Die substrate width	30.85	31.15	mm
D1	Die width	10.36		mm
D2	Package interposer width	32.60		mm
E	Die substrate length	34.85	35.15	mm
E1	Die length	17.36		mm
E2	Package interposer length	36.80		mm
e	Pin pitch	1.27		mm
-	Pin tip radial true position	<=0.127		mm
N	Pin count	615		each
S1	Pin row A to short edge of interposer	2.220		mm
S2	Pin column 1 to long edge of interposer	1.415		mm
Pdie	Allowable pressure on the die for thermal solution	-	689	kPa
W	Package weight	7.5		g
Notes:	All dimensions are PRELIMINARY and subject to change at an time.			
	(1) Overall height with socket is based on measurements from the PCB surface to the top of the exposed die of uPGA packages in sockets with no thermal solution attached. Measurements were taken from pre-production units. This dimension may change based on socket design, OEM motherboard design, or OEM SMT process.			

Figure 1b: 615-pin Micro-PGA package pin layout and key package dimensions.

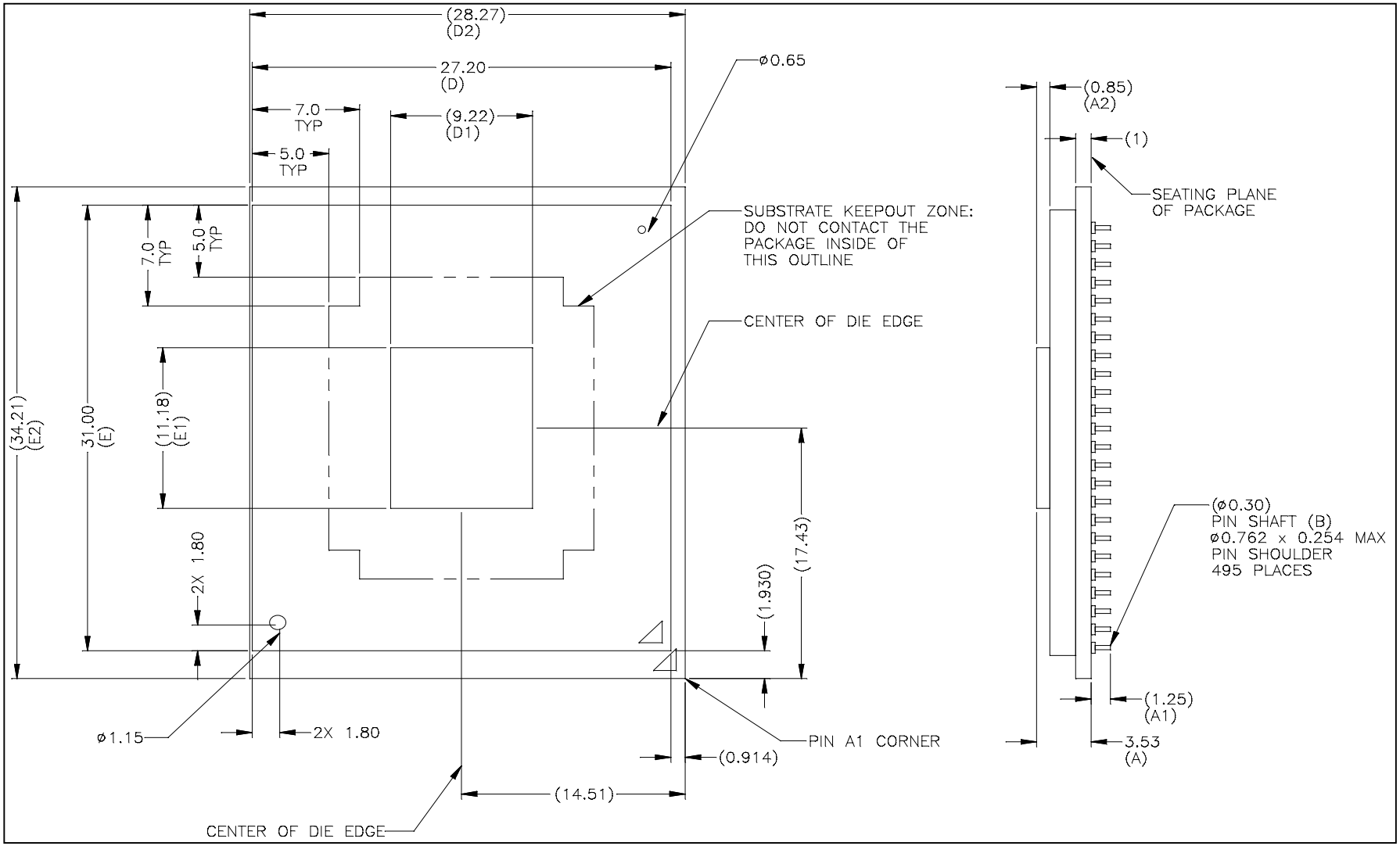
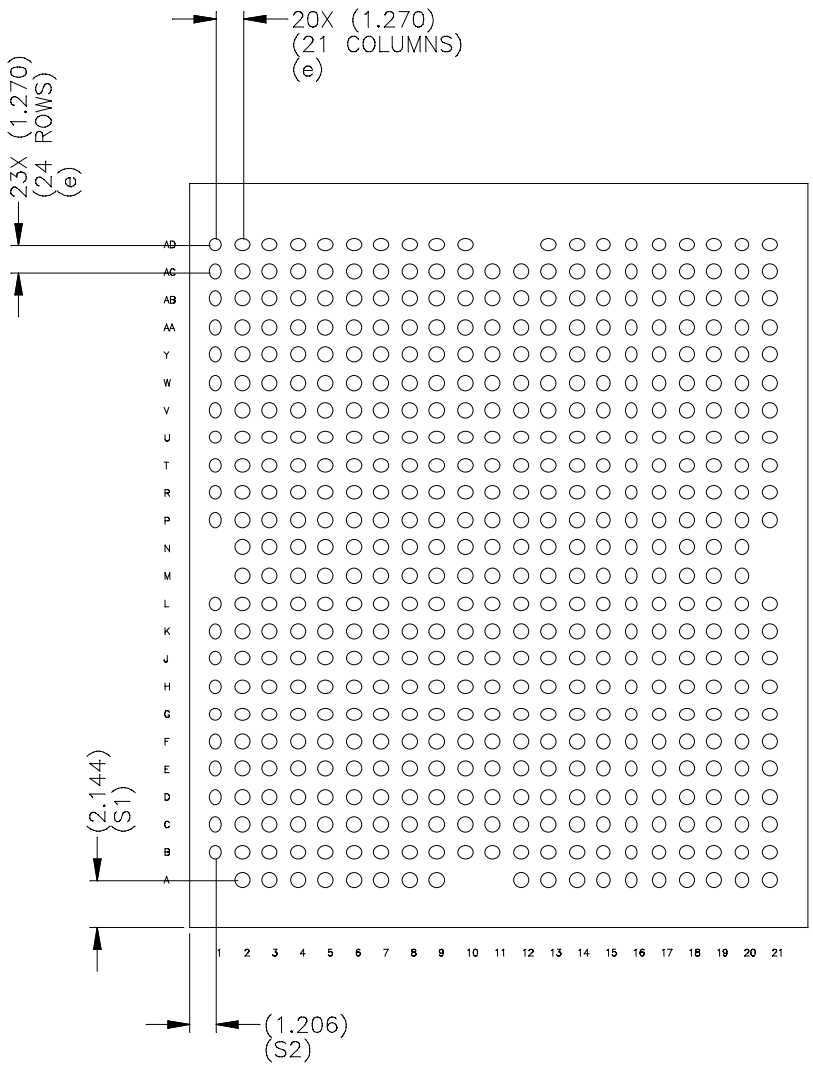


Figure 2a: 495-pin Micro-PGA package top and side view (see Figure 2b for package dimension).



Symbol	Parameter	Min	Max	Unit
A	Overall height, top of die to seating plane of interposer	3.23	3.83	mm
-	Overall height, top of die to PCB surface, including socket(1)	5.40	6.00	mm
A1	Pin length	1.25		mm
A2	Die height	0.854		mm
B	Pin diameter	0.3		mm
D	Die substrate width	27.05	27.35	mm
D1	Die width	9.22		mm
D2	Package interposer width	28.27		mm
E	Die substrate length	30.85	31.15	mm
E1	Die length	11.18		mm
E2	Package interposer length	34.21		mm
e	Pin pitch	1.27		mm
-	Pin tip radial true position	<=0.127		mm
N	Pin count	495		each
S1	Pin row A to short edge of interposer	2.144		mm
S2	Pin column 1 to long edge of interposer	1.206		mm
Pdie	Allowable pressure on the die for thermal solution	-	689	kPa
W	Package weight	6.2		g
Notes:	All dimensions are PRELIMINARY and subject to change at any time.			
	(1) Overall height with socket is based on measurements from the PCB surface to the top of the exposed die of uPGA packages in sockets with no thermal solution attached. Measurements were taken from pre-production units. This dimension may change based on socket design, OEM motherboard design, or OEM SMT process.			

Figure 2b: 495-pin Micro-PGA package pin layout and key package dimensions.

2.2. Package Dimensions

Table 1

Parameter	615-pin Micro-PGA (Max Values)	495-pin Micro-PGA (Max Values)	Comment
Pins			
Pin Pitch	1.27 mm	1.27 mm	Nominal value
Pin Tip True Position	0.254 mm	0.254 mm	Max diametrical value pin to pin
Pin Diameter	0.305 + 0.0508 mm / - 0.0254 mm	0.305 + 0.0508 mm / - 0.0254 mm	
Pin Length	1.25 +/- 0.0508 mm	1.25 +/- 0.0508 mm	
Pin Shoulder/Solder Fillet Diameter	0.762 mm	0.762 mm	Max value
Pin Shoulder/Solder Fillet Height	0.254 mm	0.254 mm	Max value
1st Row to Edge Distances	See Figure 1b.	See Figure 2b.	Package must be able to sit flush against socket cover
Substrate			
Thickness	1.0 +/- 0.15 mm	1.0 +/- 0.15 mm	
Width	36.75 +/- 0.15 mm	34.22 +/- 0.15 mm	Offset pin field
Length	32.56 +/- 0.15 mm	28.27 +/- 0.15 mm	Offset pin field
Flatness	0.7% mm/mm	0.7% mm/mm	

2.3. Package Seating

The package's pin shoulder and/or solder fillet should be able to completely fit inside the socket so that there is no gap between the package and the socket cover plate. See **Figure 3** for pin shoulder dimensions.

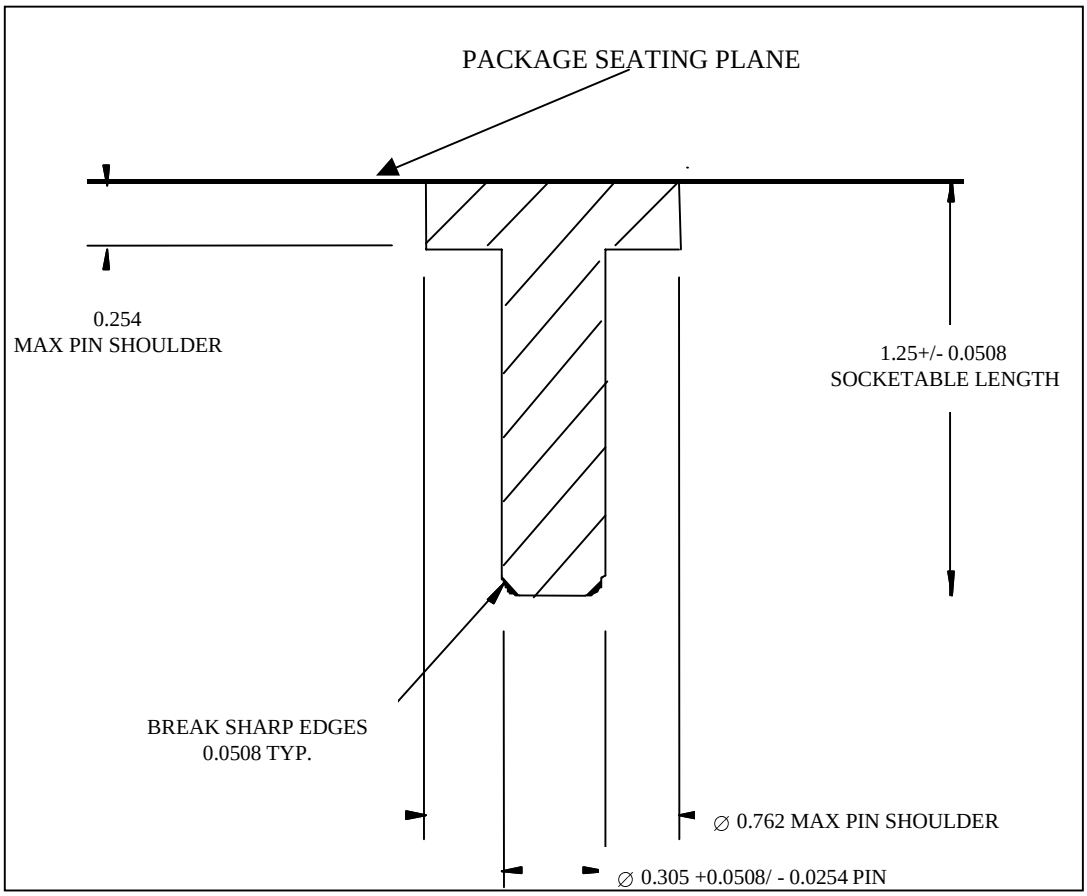


Figure 3: Pin shoulder drawing for 615-pin Micro-PGA and 495-pin Micro-PGA packages.

3. MECHANICAL REQUIREMENTS

3.1. Socket Size

3.1.1. Contact Array

3.1.1.1 615-Pin Micro-PGA Contact Array

The 615 contacts are to be located in a 24 by 26 contact array. The centerline to centerline distance of the contacts, or pitch, is to be 1.27 mm. The overall dimensions of the contact array is 29.21 mm by 31.75 mm. See **Figure 4** for exact shape of contact array as viewed looking down at the mother board attach pads.

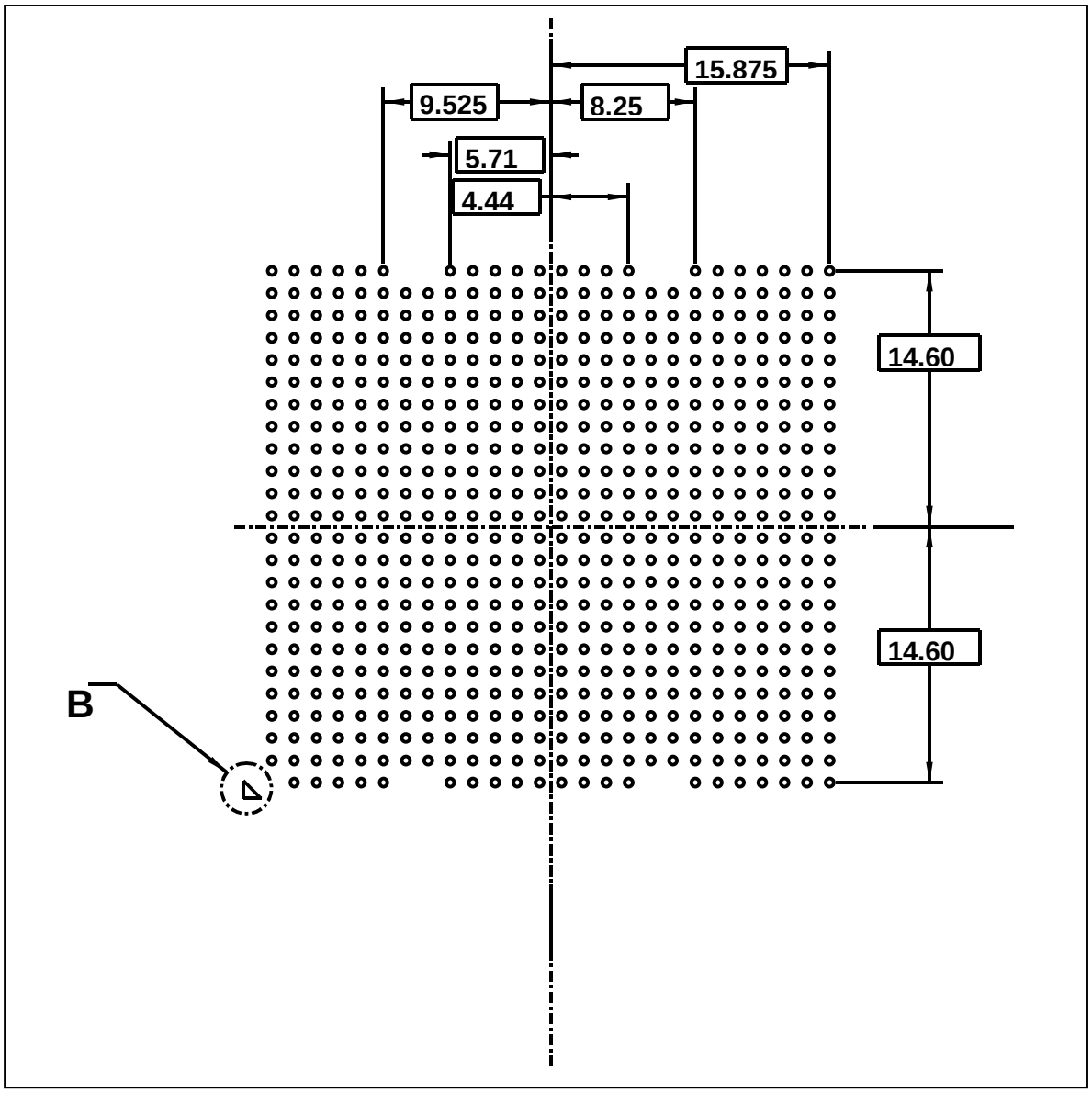
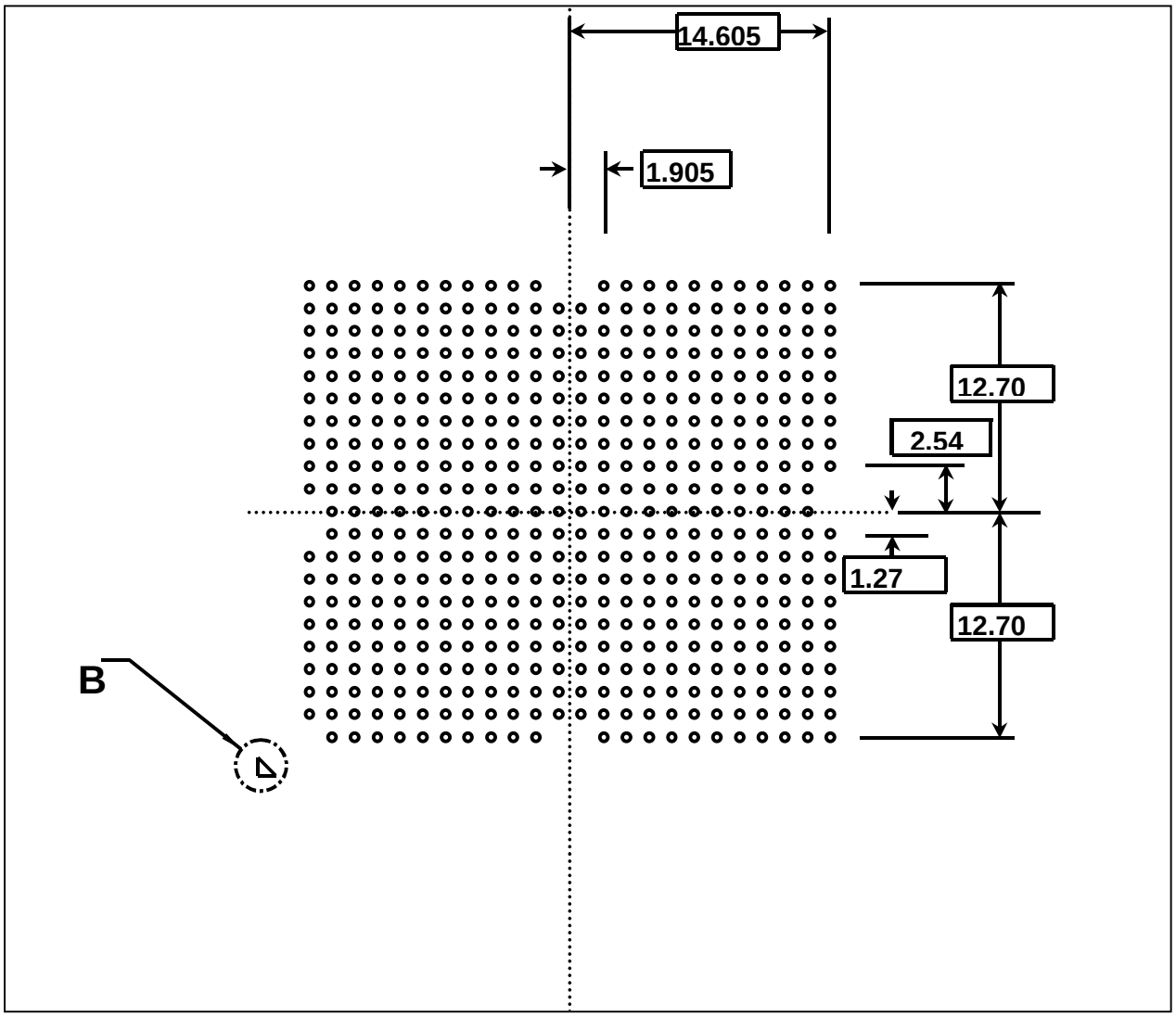
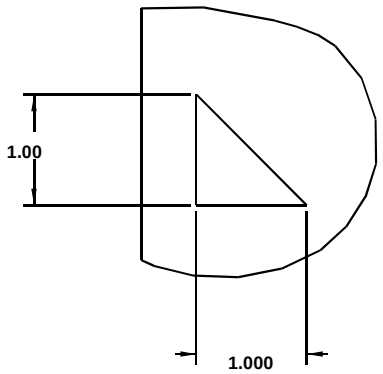


Figure 4: 615-pin Micro-PGA contact array

3.1.1.2 495-pin Micro-PGA Contact Array

The 495 contacts are to be located in a 21 by 24 contact array. The centerline to centerline distance of the contacts, or pitch, is to be 1.27 mm. The overall dimensions of the contact array is 25.40 mm by 29.21 mm. See **Figure 5** for exact shape of contact array as viewed looking down at the mother board attach pads.





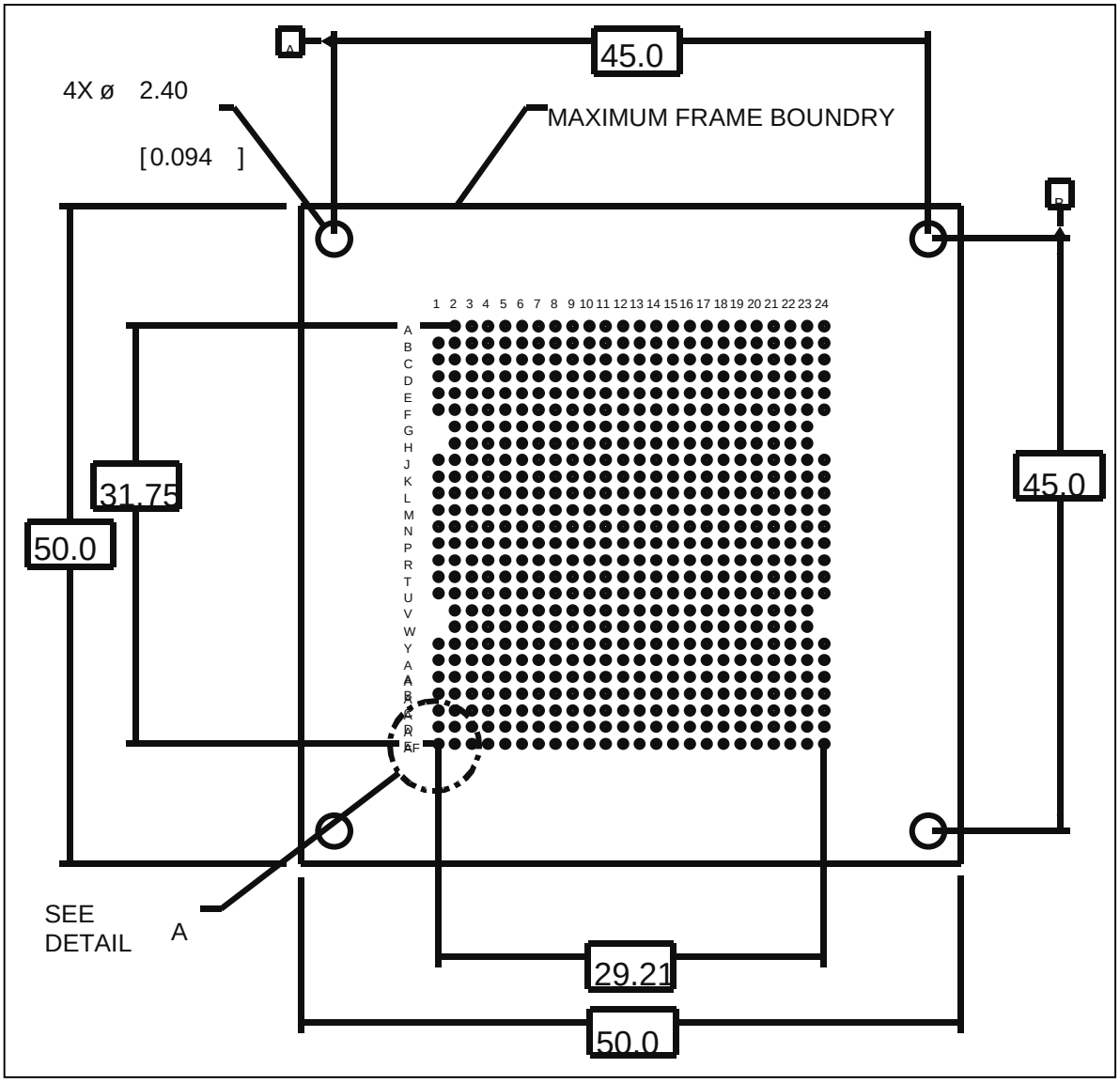
Detail B: Pin 1 Triangle

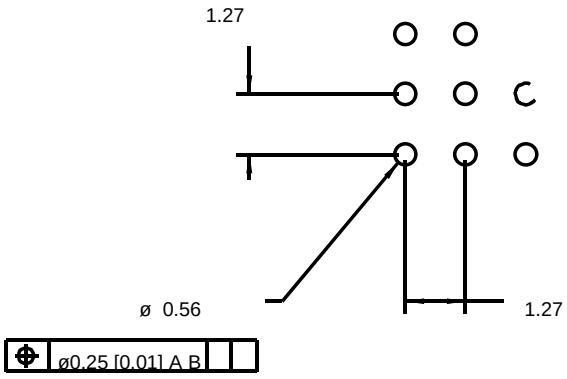
Figure 5: 495-pin Micro-PGA contact array

3.1.2. Motherboard Landing Zone

Use of the Intel thermal reference design requires the entire socket and frame to fit inside a specified landing zone that has four equally spaced threaded holes used to attach the thermal frame. The recommended landing zone for the 615-pin Micro-PGA package is 50 mm by 50 mm (hole spacing 45 mm by 45 mm) and 46 mm by 46 mm (hole spacing 41 mm by 41 mm) for the 495-pin Micro-PGA package. The solder ball array (bottom side of socket) is to be centered between the four frame holes for both the 615-pin Micro-PGA and 495-pin Micro-PGA. See **Figures 6 and 7** for location of the contact arrays with respect to the landing zone boundaries and thermal reference holes.

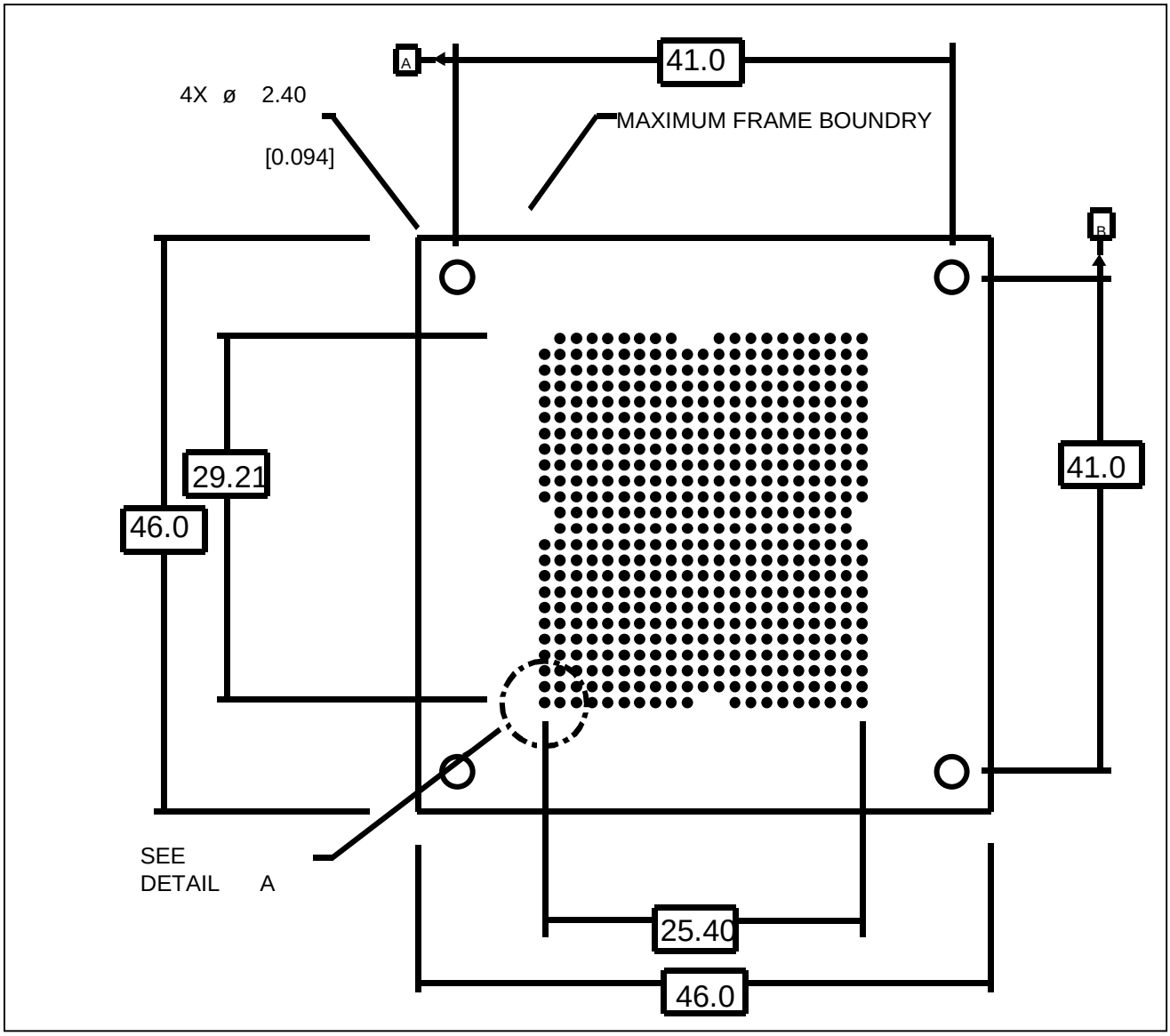
NOTE: The above landing zone sizes are minimum requirements that may vary depending on the thermal solutions used by OEMs.

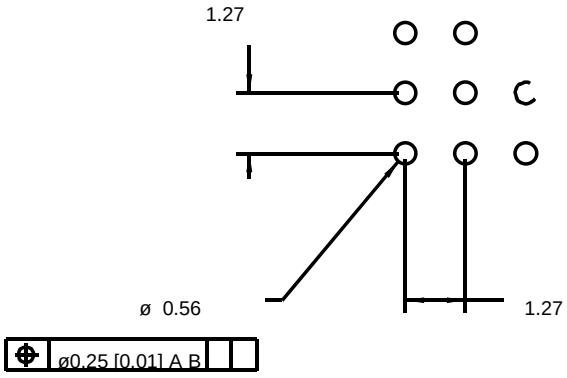




Detail A: Contact Pitch (NOTE: TP call out is for array position w.r.t. datums A and B)

Figure 6: 615-pin Micro-PGA landing zone





Detail A: Contact Pitch (NOTE: TP call out is for array position w.r.t. datums A and B)

Figure 7: 495-pin Micro-PGA landing zone

3.1.3. Weight

The socket is not to exceed 14 grams for either the 615-pin Micro-PGA or 495-pin Micro-PGA packages.

3.2. Materials

3.2.1. Socket Housing

Material with a UL 94V-0 flame rating that is capable of withstanding a SMT reflow process.

3.2.2. Color

The Micro-PGA sockets will be off-white or brown in color.

3.2.3. Visual Markings

The following marks can either be molded, laser marked, or ink marked on the cover of the socket. The mark must be able to withstand two reflows at temperatures of 240 °C for 30 seconds per cycles.

3.2.3.1 Orientation Mark

A triangular shape, on the pin 1 corner, must be located on the socket frame so that it is still visible when the interposer/OLGA is socketed to ensure proper orientation. In addition to the orientation mark, there will not be an eyehole or contact at pin 1. The purpose of this is to increase the insertion force needed to socket a misoriented interposer.

3.2.3.2 Open/Close Designation

Clear indicator marks must be located on the socket that identify the open and closed positions of the cover. These marks should still be visible after an interposer is inserted into the socket.

3.2.4. Contact Characteristics

3.2.4.1 Number of Contacts

Total number of contacts: 615 for the 615-pin Micro-PGA socket and 495 for the 495-pin Micro-PGA socket.

3.2.4.2 Base Material

High strength copper alloy.

3.2.4.3 Contact Area Plating

0.254 μm minimum gold plating over 1.27 μm minimum nickel underplate.

3.2.4.4 Solder Ball/Surface Mount Feature Characteristics

NOTE: Solder balls or other surface mount features may be used to attach the socket to the motherboard.

Solder Balls: Tin/Lead (63/37 ± 0.5% Sn) with a 0.762 mm (0.030 in) diameter.

Surface Mount Feature: Surface mount feature must extend at least 0.175 mm from the bottom of the base housing to prevent solder paste from contacting the housing

3.2.4.5 Lubricants

No lubricants are to be used on the socket contacts.

3.2.5. Environmental Concerns Requirements

Cadmium shall not be used in the painting or plating of the socket. CFCs and HFCs shall not be used in manufacturing the socket.

3.3. Visual Inspection

Visual inspection is to be performed at 1x except for lead inspection.

NOTE: The visual inspection requirements listed below contain defects that affect the functionality of the ZIF socket. Cosmetic defects will not be covered in this specification.

3.3.1. Damaged, Missing, or Misaligned Solder Balls/Leads

Requirement: No damaged, malformed, missing or misaligned solder balls or leads used in attaching the socket to the motherboard. Lead inspection is to be inspected at 5-10 x magnification.

Note that dimensional measurements of solder ball or lead true position (Section 3.5.5. Motherboard Attachment) is the primary means of determining solder ball or lead alignment.

3.3.2. Bent/Missing Contacts

Requirement: No contacts are to be missing or damaged in any way that will prevent proper functionality of the socket.

3.3.3. Missing Plating

Requirement: No missing Au plating on the mating surface of the contact.

3.3.4. Cover/Base Alignment

Requirement: No contacts are to be visible through the cover hole when the cover is located in the “open” position.

3.3.5. Damaged Housing

Requirement: No cracks are to be present on the socket housing that are visible at 1x.

3.3.6. Damaged/Missing Tabs

Requirement: The tabs/guides that connect the cover to the base are not to be missing or damaged. There should not be a visible gap between the cover and base.

3.4. Socket/Interposer Actuation

3.4.1. Actuation Tool

The socket should be designed so that it can be easily actuated in a high volume manufacturing environment. The preferred actuation tools are regular, Phillips, or hex screwdrivers. A design that requires the use of a custom tool is not recommended, however, a special actuation tool may be used if it is approved by OEMs.

3.4.2. Locking Mechanism

The socket must have a locking mechanism that holds the cover in the open position to assure a zero package insertion force at the OEMs.

3.4.3. Socket/Package Pin Field Movement

The socket will be designed so that the package pin field displacement will not exceed 1 mm during actuation and deactuation.

3.4.4. Package Pin/Motherboard Pad Position

The true position of the package pin in the engaged position must be within 1 mm of the of the true position of the motherboard pads.

3.5. Socket Manufacturability Requirements

3.5.1. Insertion/Extraction Force

The insertion and extraction forces should both be zero when the socket is not engaged (in the “open” position).

3.5.2. Socket Engagement/Disengagement Force

3.5.2.1 Lever

Less than 44.48 N (10 lbf.) to move the screwdriver (or lever) in order to engage the socket.

3.5.2.2 Torque

Less than 0.92 N-m (8.16 lbf-in) of torque must be applied to engage the socket.

NOTE: This limit is based on using a screwdriver with a handle diameter of less than 1 in and holding it with the palm of the hand.

3.5.3. Socket Retention Force

A minimum pin retention force of 10 gm/pin must be met in order to secure the package to the socket during the manufacturing process. Retention force is defined as the force required to pull the pins out of the contacts when the socket is engaged.

3.5.4. Durability

The socket must maintain mechanical and electrical characteristics after 20 insertion/extraction cycles.

3.5.5. Motherboard Attachment

The socket must be able to be surface mounted to motherboard pads ranging in diameter from 0.559 to 0.660 mm (0.022 to 0.026 in) with pad to pad true positions of 0.025 mm (0.001 in).

3.5.5.1 Coplanarity and True Position

The coplanarity and true position requirements will differ depending on the method used to mount the socket to the motherboard (solder balls vs. leads). For solder balls, the coplanarity requirement is 0.203 mm (0.008 in) and the ball true position is 0.102 mm (0.004 in). For leads, the coplanarity requirement is 0.152 mm (0.006 in) and the lead true position is 0.076 mm (0.003 in).

3.5.5.2 Flatness

The flatness of the assembled socket is not to exceed 0.7%.

3.5.5.3 Pick & Place

Tape or a plastic cover must be present on the top of the socket to allow it to be placed by a vacuum nozzle. The tape must not outgas during reflow or leave behind any residue.

3.5.5.4 Reflow

Max temperature: 240°C

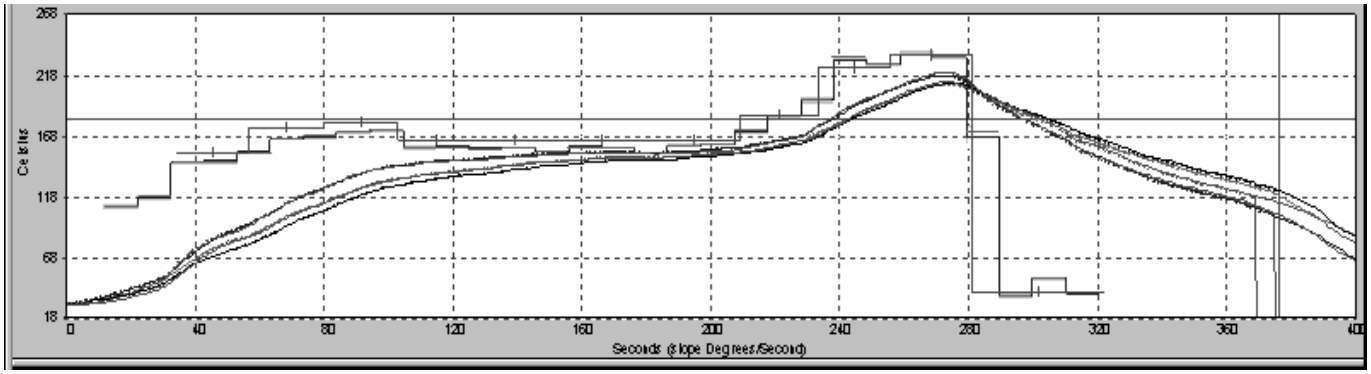


Figure 8: Typical Reflow Profile for 63Sn/37Pb solder

3.6. Critical to Function (CTF) Parameters

Critical to function dimensions are identified in **Table 2**. Also, the supplier will both provide and maintain Critical Process Parameters controlling these CTFs and provide direct measurements to meet ongoing quality requirements.

Table 2 Critical to Function Parameters

Parameter	615-Pin Micro-PGA Socket	495-Pin Micro-PGA Socket	Comment
Outer Length	40 mm Max	36 mm Max	May exceed as long as it fits inside landing zone and does not interfere with thermal reference holes
Outer Width	40 mm Max	36 mm Max	May exceed as long as it fits inside landing zone and does not interfere with thermal reference holes
Mounted Z-Height	2.2 mm Target (Height necessary to achieve 6.0 mm max total stack height)	2.2 mm Target (Height necessary to achieve 6.0 mm max total stack height)	Motherboard to package seating plane of socket (Total stack height defined as distance from motherboard to top of die)
Assembled Cover/Base Flatness	0.7%	0.7%	Value determined by length or width of socket seating area (whichever is larger)
Coplanarity – Lead – Solder Ball	 0.152 mm (0.006 in) 0.203 mm (0.008 in)	 0.152 mm (0.006 in) 0.203 mm (0.008 in)	
Cover Hole Diameter	0.40 mm Min 0.50 mm Max	0.40 mm Min 0.50 mm Max	Min size of hole for ZIF condition
Cover Hole True Position	0.10 mm	0.10 mm	Max TP for ZIF condition
Cover Thickness	0.75 mm	0.75 mm	Max allowable based on pin length
Contact Loop (Inserted Position)	Design specific	Design specific	Must not be visible through cover hole in open position
Contact Gap (Actuated Position)	Design specific	Design specific	Must achieve normal force requirements
Contact True Position	0.10 mm	0.10 mm	Max - contact must not be visible through cover hole, must not affect pin actuation
Solder Ball/Lead True Position	0.076 mm (0.003 in)	0.076 mm (0.003 in)	
Au Thickness	0.254 μm	0.254 μm	Min plating thickness
Ni Thickness	1.27 μm	1.27 μm	Min plating thickness
Actuation Distance	1.0 mm	1.0 mm	Minimum determined by contact design

4. ELECTRICAL REQUIREMENTS

4.1. Electrical Performance Specifications

The contact design of the 615-pin Micro-PGA and 495-pin Micro-PGA sockets must be capable of meeting the following performance characteristics when mated with a Kovar pin.

Specifications are from the top of the socket to the top of test board to which it is attached.

All specifications are MAX (unless otherwise stated) for a single socket pin, but includes effects of adjacent pins where indicated.

Signal-to-V_{SS} pin ratio is 2:1 and signal-to-combined V_{ss}/V_{cc} pin ratio 1:1.

Pin and socket inductance includes exposed pin from mated contact to bottom of the package.

Table 3 Electrical requirements for Micro-PGA SOCKET

	Definition	Specification	Measurement
Mated self inductance of a single pin	The inductance of a single pin of mated package and socket with no mutual inductance from any other conductor.	2nH	Can not be measured directly. Calculated by: (0.5*Loop inductance – mutual inductance) of two nearest pins.
Mated loop inductance of two nearest pins	The inductance of two nearest pins of mated socket and package considering one forward conductor and one return conductor.	Maximum: 3nH	Measured from the top pads of the package for two nearest pins (one as signal, one as ground) shorted at the bottom of the socket.
Mated mutual capacitance of two nearest pins	The capacitance between two nearest pins of mated socket and package.	Maximum: 1pF	Measured from the top pads of the package for two nearest pins (one as signal, one as ground) but not connected at the bottom of the socket.
Initial contact resistance (average of minimum 40 pins)	The DC resistance of a single pin of mated package and socket.	Maximum: 30mΩ	Measured for one pin from the top pad of the package to the bottom of the socket. This is the initial resistance before any reliability testing.
Final contact resistance (average of minimum 40 pins)	The DC resistance of a single pin of mated package and socket.	Maximum: 30mΩ	Measured for one pin from the top pad of the package to the bottom of the socket. This is the final resistance after any reliability testing.

Measurement frequency for capacitance.	Frequency at which the S-parameter measurement performed.	500MHz	
Measurement frequency for inductance.	Frequency at which the S-parameter measurement performed.	500MHz	
Socket minimum current rating and test voltages		1.0 A/pin @ $\leq$ 2 V and < 20°C temp rise due to Joule heating	Refer to 4.2.4.
Dielectric withstand voltage (min)		1000 Vac	Refer to 4.2.5.
Pin-to-Pin Insulation Resistance (min)		1000MΩ	Refer to 4.2.6.

4.2. Electrical Qualification Requirements

4.2.1. Inductance (self and mutual)

The mated self-inductance of a socket is the measured partial self-inductance of a socket pin. The components that are included in this computation are shown in **Figure 9**. These include the CPU pins after the CPU package, the socket and the socket pins before the MB connection. The definition of self-inductance does not include any mutual inductances, only the partial self-inductance of the pin with respect to infinity.

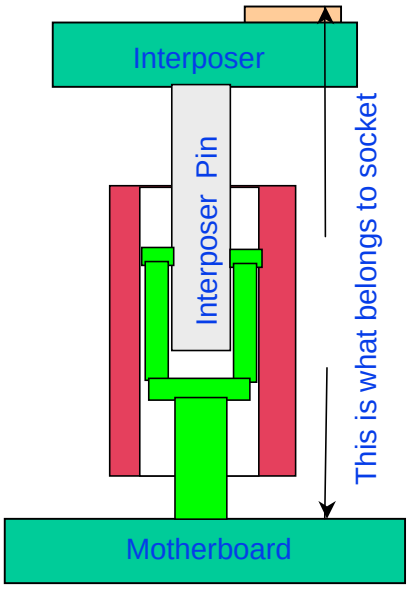


Figure 9: Socket mated self-inductance

The mated mutual inductance of the socket is defined as the inductive coupling between pins.

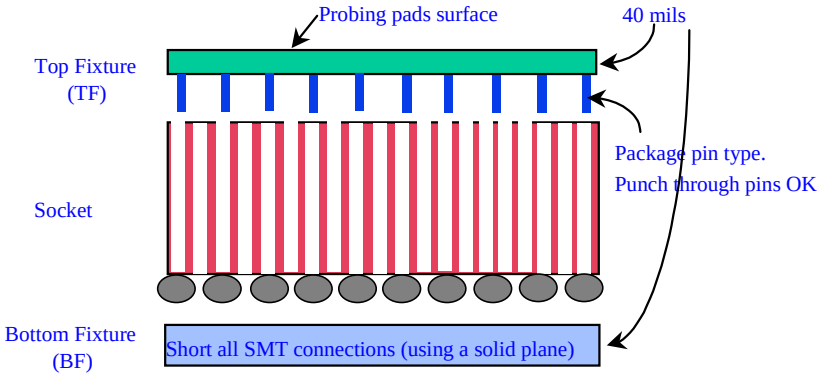


Figure 10: Cross-sectional view of the top and bottom L fixtures

A set of probe pad patterns is designed on the Top L fixture to measure the specified parameters. This is shown in **Figure 11**.

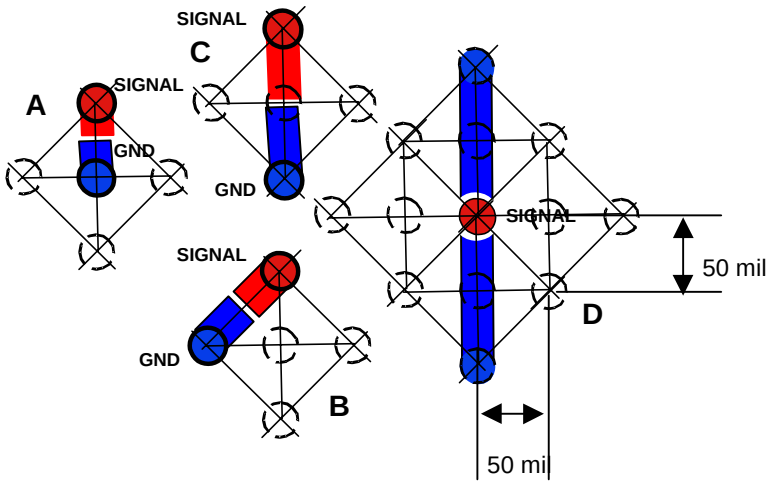


Figure 11: Top L Fixture probing pad design (50 mil grid pattern)

As can be observed in **Figure 11**, there are 4 distinct structures for characterization, corresponding to the 4 parasitics that need to be extracted:

<u>50 mil grid array socket</u>

- Pin Self Inductance - (L_s)
- Pin Mutual Inductance (50 mils) - (M_{50} – average of two directions)
- Pin Mutual Inductance (70.71 mils) - (M_{70} – average of two directions)
- Pin Mutual Inductance (100 mils) - (M_{100} – average of two directions)

The parasitics of the fixture are calibrated out by shorting the Top L fixture with the Bottom L fixture. The gap between the top and bottom fixtures should be as small as possible (ideal is no gap), and the maximum allowable gap on any sides is 10 mils. The pintail of the package pins should be trimmed off.

To calibrate out the fixture for surface mount sockets, the pins of the top fixture will need to be cut and shaved, and then mounted just as the socket would be mounted.

4.2.1.1 Solving for unknowns

To obtain the 4 unknowns, 4 sets of measurements are made after obtaining the fixture parasitic. Denoting the structure as A,

B, C and D while giving the suffix for the fixture of each measurement as L_{fA}, L_{fB}, L_{fC}, and L_{fD}, the values of each parameters are solved using the 4 equations below:

Table 4 Equations for inductance calculation

50 mil grid
$2(Ls - M_{50}) = L_A$, $M_{50} = L_s - L_A/2$
$2(L_s - M_{70}) = L_B$, $M_{70} = Ls - L_B/2$
$2(L_s - M_{100}) = L_C$, $M_{100} = L_S - L_C/2$
$1.5L_S - 2M_{100} + 0.5M_{200} = L_D$
$1.5L_S - 2(L_S - L_C/2) = L_D$ (M_{280} assumed = 0)
$L_S = 2(L_C - L_D)$
$L_{LOOP} = 2*(L_S - M_{50})$

4.2.2. Capacitance

Pin-to-pin capacitance shall be measured as per EIA 364, Test procedure 30. Pin-to-pin contact capacitance shall be measured between adjacent signal pins (signal to signal) The signal to signal measurements and the signal to ground measurements will be done with a signal to ground ratio of 1:1 where the ground pin has 50 mil pitch to signal pin. Five (5) measurements each shall be made between random lateral, diagonal and vertical adjacent pins for a total of fifteen (15) measurements. This measurement is in the unmounted condition and includes the contact and solder balls.

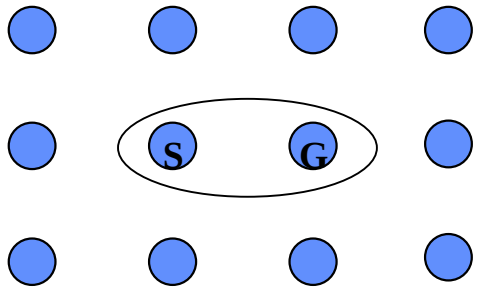


Figure 12: Pin layout for capacitance meaurements

NOTE: Pin-to-pin capacitance is for the socket only, and is for signal pins coupled to other adjacent signal or V_{CC}/V_{SS} pins.

4.2.3. Contact Resistance

This is to make sure that the contact resistance (bulk resistance of contact, solder ball, and package pin + interface resistance) has not degraded during environmental testing. The measured value includes the mounted socket plus engaged package pin, and can be measured on any low voltage, current controlled tester.

Measure total contact resistance R_i for each of the 20 contact pairs (40 total contacts). To determine average contact resistance, sum up R_i for all contact pairs and divide by the number of contacts. That is, for Micro-PGA,

$R_{ave} = \sum R_i$ / (2*# of contact pairs)

4.2.3.1 Initial Contact Resistance:

Measured immediately after the first mating and actuation of the package and socket. The three performance requirements for initial contact resistance are:

a) Initial total contact resistance average of 40 contacts is not to exceed 30mΩ.

b) No pin can exceed the initial contact resistance of 500mΩ.

c) 2 or more contacts per socket cannot exceed the initial contact resistance of 35mΩ.

4.2.3.2 Final Contact Resistance:

Measured after the environmental tests developed that are based on the expected field use environment for mobile products found in **Table 5**.

The requirement for the measured contact pairs is that the final average total contact resistance is not to exceed 30mΩ per contact.

4.2.4. Test Voltage and Current Rating

Test to be performed at 1.0 A/contact. Voltage can vary to a maximum of 2.0V during test to attain 1.0A. Less than 20°C rise in temperature due to Joule heating.

Once the current rating of 1.0 amp IDC is established, monitor the contact temperature for 5 minutes. Measure the temperature rise after stabilization has occurred. Contact current rating shall be measured for five contacts per socket. Testing shall be measured as per EIA 364, test procedure 70, method 13.

4.2.5. Dielectric Withstand Voltage

A minimum requirement of 1000 Vac as measured per EIA 364, Test Procedure 20.

Pin dielectric withstand voltage shall be measured between adjacent random lateral, diagonal and vertical adjacent pins.

Five (5) measurements shall be made for each of the above three options for a total of fifteen (15) measurements.

NOTE: This measurement is on socket only in unmated condition (no substrate mated).

4.2.6. Pin-to-Pin Insulation Resistance

A minimum requirement of 1000MΩ, as measured per EIA 364, Test Procedure 21.

Pin-to-pin insulation resistance shall be measured between adjacent random lateral, diagonal and vertical pins.

Five (5) measurements shall be made for each of the above three options to a total of fifteen (15) measurements.

NOTE: This measurement is on socket only in unmated condition (no substrate mated).

5. RELIABILITY TARGETS

The reliability targets in this section are based on the expected field use environment for a mobile product. The test sequence for new sockets will be developed using the knowledge-based reliability evaluation methodology, which is acceleration factor dependent. A simplified process flow of this methodology can be seen in **Figure 13**. A more detailed description of this methodology can be found at: http://developer.intel.com/design/packtech. The use environment expectations assumed for mobile processors, based on an expected life of 7 to 10 years, are listed in **Table 5**. The suggested target for the expected fail rates are 1% at 7 years and 3% at 10 years.

Figure 13: Flow chart of knowledge-based reliability evaluation methodology

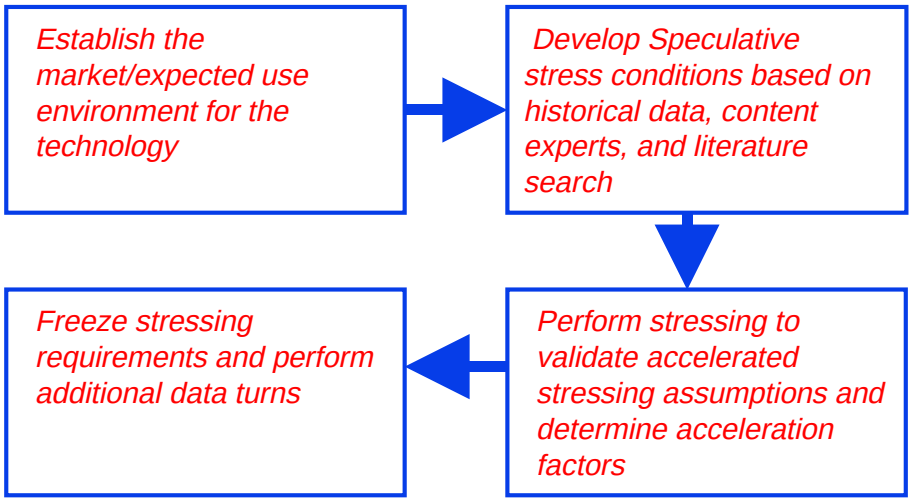


Table 5 Expected Field Use Environment

Use Environment Expectations	7 Year Life Expectation
Slow small internal gradient changes due to external ambient (temperature cycle or externally heated)-**Temperature Cycle**	3000 cycles with a mean $\Delta T = 40^{O}C$
High ambient moisture during low-power state (operating voltage)- **THB/HAST**	62K hours at $30^{O}C$/85%RH
High Operating temperature and short duration high temperature exposures - **Bake**	62K hours at Max operating temperature
Fast, large gradient On/off (to max operating temperature) (power cycle or internally heated including power save features)**- Power Cycle**	7500 cycles
Mechanical Shock	Trapezoidal 50g. Velocity change 170 in./sec 3 drops in each of 6 directions
Mechanical Vibration	5 Hz - 20 Hz .01 g2/Hz sloping up to .02 g2/Hz 20 Hz - 500 Hz .02 g2/Hz 3.13 gRMS, random10 minutes/axis
Operating Temperature	$0^{O}C$ to $105^{O}C$

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