# intel®

# Intel® Mobile Processor Micro-FCPGA Socket (mPGA479M)

**Design Guidelines**

*November 2001*

*Revision 1.0*

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# Revision History

| Rev. | Doc. ID | Description | Date |
|------|---------|-------------|------|
| 1.0 | 298520-001 | Initial Release | November 2001 |

# 1. Introduction

## 1.1. Objective

This document defines the Surface Mount Technology (SMT) Zero Insertion Force (ZIF) socket that will support the Micro-FCPGA mobile processor packages.  The mobile Micro-FCPGA socket (mPGA479M) must be low cost, low risk, robust, reliable, and manufacturable in high volumes.  The mPGA479M socket has 479 contacts with a pitch of 1.27 mm, mating with a Micro-FCPGA package that has a maximum of 479 pins.

## 1.2. Purpose

To define for the mPGA479M socket the mechanical, electrical, quality, and reliability requirements necessary to meet the product requirements of the Micro-FCPGA mobile processor package.

## 1.3. Scope

This specification applies to all ZIF sockets designed for use with all Intel mobile processor in the Micro-FCPGA package having a maximum of 479 pins per package.

# 2. Package Description and Assembled Component

Information provided in this section is to ensure dimensional compatibility of the mPGA479M socket with the corresponding package. Zero insertion force (ZIF) is required for placement of the Micro-FCPGA package into the socket prior to actuation.

## 2.1. Package Description

The outline of the package that can be used with the mPGA479M socket is illustrated in Appendix Z.1. The package will contain a 26 x 26 array of pins (with a center cavity gap of a 14 x14 array of pins) contained in a substrate that is 35.1mm x 35.1mm maximum. The pin length is 2.03mm nominal. The package dimensions and tolerances are specified in Appendix Z.1.

## 2.2. Assembled Component

The assembled component may consist of a processor inserted into the socket, a thermal solution, and attachment hardware.

### 2.2.1. Motherboard Landing Zone

Intel's mechanical system recommendations suggest that a keepout border of approximately 5mm surround the entire socket, resulting in a 54mm x 46mm landing zone as illustrated in Appendix Z.2. Included in the keepout zone are four holes, used for thermal solution attach, located in a 41mm nominal square pattern. The motherboard pad array is located in perfect symmetry with the centerline axis of the square pattern defined by the four holes. See Appendix Z.2 for location of the contact arrays with respect to the landing zone boundaries and thermal reference holes.

*Note:* The above landing zone sizes are Intel's recommended minimum requirements that may vary depending on the thermal solutions implemented by OEMs.

# 3. Mechanical Requirements

## 3.1. Socket Dimensions

The socket must meet the mechanical dimensions listed in Table 1 and illustrated in Appendix Z.3.

## 3.2. Mechanical Support

The socket must pass the mechanical shock and vibration conditions listed in Section 5 with the associated thermal solution and retention mechanism in place. The maximum compressive load, applied by the retention mechanism and thermal solution that the socket must be able to withstand is 50 lbf. The socket can only be attached to the motherboard by the socket solder ball/surface mount feature. No additional methods of attaching the socket (i.e. screws, extra solder, adhesive, etc) are acceptable.

## 3.3. Materials

### 3.3.1. Environmental Concerns Requirements

CFCs and HFCs shall not be used in manufacturing the socket. Cadmium shall not be used in the painting or plating of the socket.

### 3.3.2. Socket Housing

Material with a UL 94V-0 flame rating that is capable of withstanding a SMT reflow process. The material must have a coefficient of expansion in the x-y plane capable of passing reliability tests rated for an expected high operating temperature while mounted on a typical motherboard material.

### 3.3.3. Color

The color of the mPGA479M socket should be optimized to provide the contrast needed for OEM's pick and place vision systems. The base and cover of the socket may be different colors as long as they meet the above requirement.

## 3.4. Visual Markings

The following marks can either be molded, laser marked, or ink marked on the cover of the socket. The mark must be able to withstand two reflows at temperatures of 240 $^\circ$C for 30 seconds per cycles. If ink is used, the ink must be solvent resistant. No smearing or fading of ink mark is acceptable when subjected to testing per EIA 364 -11A.

### 3.4.1. Name

**mPGA479M** (Minimum letter size is 0.75 mm high by 0.5 mm wide, Font type is Helvetica).

**Manufacturer's insignia** (font size at supplier's discretion).

### 3.4.2. Locked (Closed) and Unlocked (Open) Markings

Mark the Locked and Unlocked positions on the socket with the universal symbol of the locked and unlocked pictures shown below in Figure 1. Clear indicator marks must be located on the actuation mechanism that identifies the lock (closed) and unlock (open) positions of the cover as well as the actuation direction. These marks should remain visible after a package is inserted into the socket.

**Figure 1. Illustration of Universal Locked/Unlocked Symbols**



Locked (closed)          Unlocked (open)

### 3.4.3. Lot Traceability

Each socket shall be marked with a lot identification code that will allow traceability of all components, date of manufacture (year and week), and assembly location. The mark must be placed on a surface that is visible when mounted on a printed circuit board. In addition, this identification code must be marked on the exterior of the box in which the units ship.

### 3.4.4. Keying Feature and Orientation Mark

There shall be no through hole at location A1 to prevent improper insertion/seating of a misoriented package. In addition, the socket must have a triangular shape feature located on the socket frame that indicates the corner of location A1 that remains visible when the package is inserted. Detail of the orientation mark is defined in Appendix Z.3.

## 3.5. Contact Characteristics

### 3.5.1. Number of Contacts

Total number of contacts: 479

### 3.5.2. Base Material

High strength copper alloy.

### 3.5.3. Contact Area Plating

0.762 µm (30 uin) minimum gold-plating over 1.27 µm (50 uin) minimum nickel under-plate in area on contact where package pins will mate. No contamination by solder in the contact area is allowed during solder reflow.

### 3.5.4. Plating Thickness

Plating thickness shall be measured at various locations on contact surface per EIA 364, Test Procedure 48, Method C or Method A. Test to be performed on a minimum of 5 sockets, 20 randomly selected contacts per socket. No plating thickness measured shall be less than the minimum plating thickness specified in Section 3.5.3.

### 3.5.5. Plating Porosity

Plating porosity shall be tested per EIA 364-53A on a minimum of 5 sockets, 20 randomly selected contacts per socket. The average porosity count as defined by EIA 364, test procedure 53A for the lot shall not exceed 2 counts.

### 3.5.6. Solder Ball/Surface Mount Feature Characteristics

*Note:* Solder balls or other surface mount features may be used to attach the socket to the motherboard.

Solder ball material type shall be of Tin/Lead (63/37 $\pm$ 0.5% Sn). Ball diameter may be either 0.508mm (0.020 in) or 0.762mm (0.030 in) as long as the socket passes the reliability targets described herein.

Surface mount features must extend at least 0.175mm from the bottom of the base housing to prevent solder paste from contacting the housing

### 3.5.7. Lubricants

No lubricants are to be used on the socket contacts. No lubricants are allowed on the socket contacts. If lubricants are used elsewhere within the socket assembly, these lubricants must not migrate to the contacts.

## 3.6.        Weight

The socket shall not exceed 14 grams.

## 3.7.        Visual Inspection

Visual inspection is to be performed at 1x except for lead inspection.

*Note:* The visual inspection requirements listed below contain defects that affect the functionality of the ZIF socket.  In addition, the socket must be inspected to ensure the critical-to-function dimensions listed in Table 3.1 and illustrated in Appendix Z.3 are met.  Cosmetic defects are not covered in this specification.

### 3.7.1.        Damaged, Missing, or Misaligned Solder Ball

**Requirement:**  Solder Ball inspection shall be inspected at 5-10 x magnification.  No damaged, malformed, misaligned or missing solder ball is permissible.

*Note:* Visual Inspection cannot detect solder ball true position and misalignment in all cases.  Dimensional measurement using more precise equipment shall be the primary means of determining solder ball true position and alignment.

### 3.7.2.        Bent/Missing Contacts

**Requirement:**  No contacts are to be missing or damaged in any way that will prevent proper functionality of the socket.

### 3.7.3.        Missing Plating

**Requirement:**  No missing Au plating on the mating surface of the contact.

### 3.7.4.        Cover/Base Alignment

**Requirement:**  No contacts are to be visible through the cover hole when the cover is located in the "open" position.  There should not be a visible gap between the cover and base.

### 3.7.5.        Damaged Housing

**Requirement:**  No cracks are to be present on the socket housing that are visible at 1x.

### 3.7.6.        Damaged/Missing Tabs

**Requirement:**  The tabs/guides that connect the cover to the base are not to be missing or damaged. There should not be a visible gap between the cover and base.

## 3.8. Package Insertion/Removal

A Zero-Insertion-Force (ZIF) condition must be achieved in the design of the socket. In addition, the following guidelines describe socket features required for proper interaction with the processor package.

### 3.8.1. Insertion/Extraction Force

The insertion and extraction forces shall be zero when the socket is not engaged (in the "open" position).

### 3.8.2. Socket Cover Standoff Height

The package should be designed to have cover standoffs along the socket's external and internal perimeter that allow the package seating plane (substrate of the package) to sit flush with the standoffs. They should be large enough to prevent warpage of the package under compressive loading. The external standoffs should be designed to allow easy removal of the package from the socket without the use of a tool. The cover standoffs should be high enough (0.25 mm to 0.35 mm) to prevent the solder fillet at the base of the package pins from making contact with the cover of the socket. The assembled cover flatness requirement of 0.25 mm is to be measured on the top of the standoffs.

### 3.8.3. Package Seating

To ensure that the socket design allows for proper seating, the socket stand off height, cover lead in, and cover lead in depth must be sized to prevent possible interference with package pin shoulder at all worst case conditions (see Figure 2 below). The package solder fillet dimension is defined in Appendix Z.1. In addition, no z-axis travel (lift out) of the package is allowed during actuation.

**Figure 2. Illustration of Proper Seating**
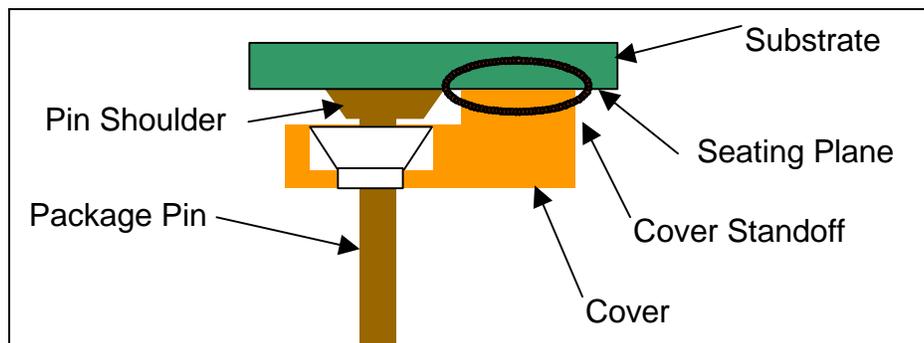


### 3.8.4. Finger Relief Cutouts For Package Removal

Recessed cutouts on either side of the socket are required to facilitate the manual removal of inserted package. Recommended size and location of the finger relief cutouts are defined in Appendix Z.3.

# 3.9.        Socket Actuation and Package Retention

This section describes requirements for socket actuation and package retention once the package is inserted into the socket.

## 3.9.1.        Actuation Tool

The socket should be designed so that it can be easily actuated in a high-volume manufacturing environment using a 4.0-4.5mm regular (flat head) screwdriver.

## 3.9.2.        Socket Engagement/Disengagement Force

No more than 0.92 N-m (8.16 lbf-in) of torque shall be required to engage and disengage the socket.

*Note:*     This limit is based on using a screwdriver with a handle diameter of less than 1 inch and holding it with the palm of one hand**.**

## 3.9.3.        Actuation Mechanism

The actuation mechanism of the socket must hold the cover in the open position to assure a zero package insertion force.  Hard stops are needed at the actuation mechanism's open and closed positions to prevent overtravel that may cause damage to the package pins and the socket itself.  The actuation mechanism should be designed so that the actuation direction is clockwise and the deactuation direction is counterclockwise.

## 3.9.4.        Socket/Package Translation During Actuation

Cover movement during actuation should be in the Y direction (refer to axes as indicated in Appendix Z.3) away from the actuation mechanism. The maximum cover travel distance should not exceed 1mm. The outer edges of the socket need to fit within the maximum socket size outline in both the open and closed positions.

## 3.9.5.        Pin-To-Contact Mating

Extreme stack-up conditions such as maximum package warpage, maximum socket cover warpage, maximum socket thickness, etc., may position the package pin away from the socket contacts.  Under those extreme conditions, the socket shall be designed to:

1.   Ensure proper pin-contact engagement to maintain an acceptable electrical performance.
2.   Prevent any subsequent damage to the package and socket itself in the event the package is moving toward the socket under the compressive load applied by the thermal solution.

## 3.9.6.        Socket Retention Force

A minimum package retention force of 10 lbf is required in order to secure the package within the socket when actuated.  The retention force is defined as the force in Z direction required to pull the pins out of the contacts when the socket is fully engaged.

## 3.10.    Socket Manufacturability Requirements

This section describes requirements to ensure the socket meets the rigors of a high-volume manufacturing environment.

### 3.10.1.    Durability

Per EIA specification 364, test procedure 9, (referenced in EIA 540), the total durability requirement is 20 cycles.  The durability testing is performed with 4 separate devices, each undergoing 5 sequential durability cycles.   Measure contact resistance when mated in the 1st and 20th cycles.  The package should be removed at the end of each de-actuation cycle and reinserted into the socket.

*Note:*  It is important to use an unused test device for the first and last cycles in order to make the appropriate resistance measurements

### 3.10.2.    Motherboard Attachment

The socket must be able to be surface mounted to motherboard pads ranging in diameter from 0.559 to 0.660 mm (0.022 to 0.026 in) with pad-to-pad true positions of 0.025mm (0.001 in).

### 3.10.3.    Coplanarity and True Position

The coplanarity requirements will differ depending on the method used to mount the socket to the motherboard (solder balls vs. leads).  The coplanarity requirement is 0.203 mm (0.008 in) for solder balls and 0.152 mm (0.006 in) for leads.  The true position requirements are the same for solder balls and leads.  The pattern locating true position is 0.406 mm (0.016 in) and the feature relating true position is 0.25 mm (0.010 in).

### 3.10.4.    Pick & Place

A smooth, flat surface must be present on the socket's top surface to allow the socket to be picked and placed using a vacuum nozzle.  The pick and place feature should be easily removable without leaving behind any residue and must not outgas during reflow.

#### 3.10.4.1.    Reflow

The socket must be able to withstand double sided reflow at a max temperature of 240°C.  For reference, a typical reflow temperature profile is shown in Figure 3.

**Figure 3. Typical Reflow Profile for 63Sn/37Pb Solder Based on Intel's Test Board**
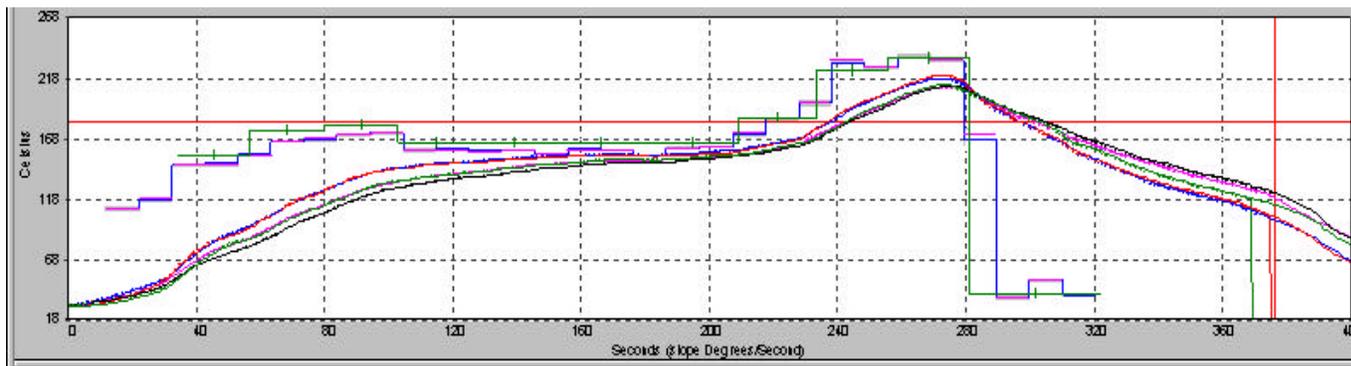


# 3.11.    Critical to Function (CTF) Parameters

Critical to function dimensions are identified in the generic mPGA479M socket drawing in Appendix Z.3 and Table 1 for convenient reference.  These dimensions shall be verified as part of the design validation process.  The manufacturer is required to monitor these critical-to-function (CTF) parameters as part of on-going quality control.

**Table 1. Critical to Function Parameters**

| Dimension | Minimum | Nominal | Maximum | Comment |
|---|---|---|---|---|
| Socket Height Beneath Package | 2.8 mm | 3.0 mm (target) | 3.2 mm | Post-reflow from package seating plane (top of cover standoffs) to motherboard |
| Socket Height Above Package Seating Plane | | | 1.5 mm | From package seating plane to top surface of cam box. |
| Socket Overall Width (X) | 35.8 mm | 36 mm | 36.2 mm | |
| Socket Overall Length (Y) | 43 mm | | 44 mm | Includes actuation mechanism. In both open and closed position. |
| Assembled Cover Standoff Flatness | | | 0.25 mm | Measured on cover standoffs |
| Cover Standoff height | 0.25 mm | 0.30 mm | 0.35 mm | See section 3.8.2 |
| Co-planarity Lead / Surface Mount Feature Solder Ball | | | 0.15 mm 0.20 mm | |
| Solder Ball/Lead True Position Pattern Locating Feature Relating | | | 0.41 mm 0.25 mm | |
| Gold Plating Thickness | 0.762 μm (30 μin) | | | Measured at mating area |
| Nickel Plating Thickness | 1.27 μm | | | Measured at mating area |

| | | | | |
|---|---|---|---|---|
| | (50 μin) | | | |
| Cover Hole diameter | 0.40 mm | | | Note 1. |
| Cover Hole True Position | Note 1. | | | Note 1. |
| Cover Hole Lead in Diameter | Design specific | | | See section 3.8.6 |
| Cover Hole Lead in Depth | Design specific | | | See section 3.8.6 |
| Contact Gap | Design specific | | | Note 2 |
| Contact True Position | Design specific | | | Note 2 |
| Contact Inner Loop Diameter | Design specific | | | Note 1 |
| Contact Inner Loop TP | Design specific | | | Note 1 |
| Contact Angle | Design specific | | | Note 2 |
| Through Cavity Y | 15.05 mm | | | In both open and closed position |
| Through Cavity X | 15.05 mm | | | In both open and closed position |

**NOTES:**
1. Design dimension and tolerance are to be selected by supplier to meet ZIF and to ensure no contact is visible through cover hole at OPEN position.
2. Design dimension and tolerance are to be selected by supplier to meet electrical, reliability, and durability requirement as described herein.

# *4.        Electrical Requirements*

In order to meet the performance requirements, the socket must meet the following electrical requirements as listed in Table 2.  These electrical characteristics are a unique function of the socket geometry and material properties.  Because the electrical characteristics of each socket design are different, they must be calculated and measured.  The definition for each electrical characteristic is listed in Table 3.

The measurement procedures to acquire the electrical characteristics are also provided in this section. The test procedures are based on the test vehicles listed in Table 4.

## 4.1.        Electrical Requirements

### Table 2. Electrical Requirements

| Item | Parameter | Limit | Note |
|------|-----------|-------|------|
| 1 | Final mating resistance (average of minimum 40 pin/contact mated connections) | ≤ 17 mΩ<br><br>≤ 25 mΩ | If Cu-194 alloy pin<br><br>If Kovar pin<br><br>(Requirement after environmental and reliability testing) |
| 2 | Mated loop inductance, Lloop | <3.0 nH | |
| 3 | Maximum mutual capacitance, C | ≤ 1.0 pF | |
| 4 | Socket minimum current rating @ 1.0A | Read & Record | Measured per EIA 364, Test Procedure 70, Method 1. |
| 5 | Pin-to-Pin/Connector-to-Connector insulation resistance (min) | > 800 MΩ | Minimum requirement.  Measured per EIA 364, Test Procedure 21 |
| 6 | Measurement frequency for Pin-to-Pin/Connector-to-Connector capacitance. | 400 MHz | |
| 7 | Measurement frequency(s) for Pin-to-Pin/Connector-to-Connector inductance. | 1 GHz | |

## 4.2. Definitions

**Table 3. Electrical Definitions**

| Item | Parameter | Definition |
|------|-----------|------------|
| 1 | Final Mating resistance | Average resistance per pin/contact location within a chain excluding the resistance of all the shorting bars in the package and the motherboard (or test board). This is measured for a minimum of 40 pin/contact connections after any environmental and reliability testing. |
| 2 | Mated loop inductance, Lloop | The inductance calculated for a pair of two adjacent pins/contacts, considering one forward conductor and one return conductor.<br><br>The inductance must include the entire length of the pins from the pin tip to the socket seating plane. |
| 3 | Maximum mutual capacitance, C | The capacitance between two pins/connectors. |
| 4 | Measurement frequency(s) for capacitance. | Capacitively dominant region. This is usually the lowest measurable frequency. This should be determined from the measurements done for the feasibility. |
| 5 | Measurement frequency(s) for inductance. | Linear region. This is usually found at higher frequency ranges. This should be determined from the measurements done for the feasibility. |

## 4.3. Electrical Test Vehicles

**Table 4. Electrical Test Vehicles**

| Item | Description | Part no. | Supplier | Purpose |
|------|-------------|----------|----------|---------|
| 1 | Cu-194 Alloy Pin Daisy Chained Package Test Vehicle | A52527-001 | Intel | Resistance measurement |
| 1A | Kovar Pin Daisy Chained Package Test Vehicle | RF860MCVA | Intel | Resistance measurement |
| 2 | Daisy Chained Test Board | A26796-001 | Intel | Resistance measurement |
| 3 | Daisy Chain Inductance Test Fixture | A00590-002 | Nanya | Inductance measurement |
| 4 | Daisy Chain Capacitance Test Fixture | 739901-002 | Intel | Capacitance measurement |

# 4.4. Electrical Resistance

The recommended methodology for measuring the final mating resistance is shown in Figure 4 and Figure 5. This method requires first measuring a Package Test Vehicle (PTV) flush-mounted directly to the motherboard fixtures so that the pin shoulder is flush with the motherboard, as shown in Figure 4. This gives the total resistance of all shorting bars, $R_{jumper}$. The mean or average $R_{jumper}$ should come from a good statistical average of 30 PTV fixtures flush mounted to a motherboard fixture. The same measurements are then made with a normal pinned PTV fixture mounted on a socket that has been surface mounted on a motherboard fixture, as shown in Figure 5. This provides $R_{Total}$. The resistance requirement, $R_{Req}$, can be calculated for each chain as will be explained in the following sections.

**Figure 4. Methodology for Measuring Rjumper**
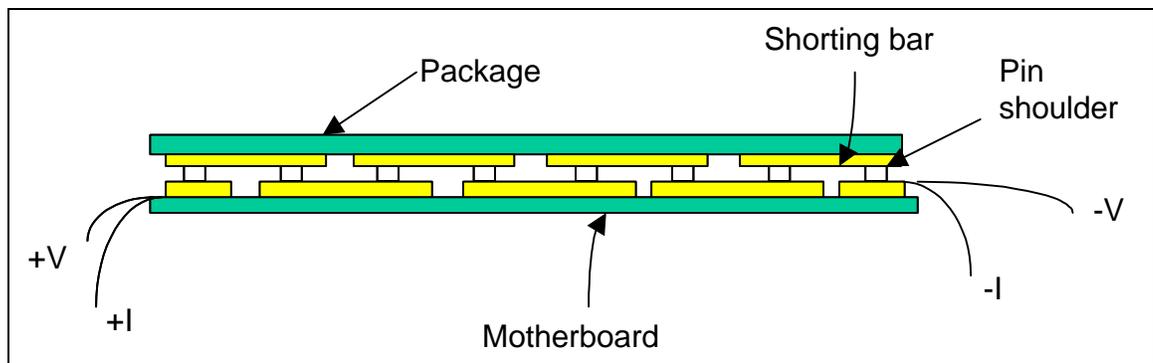


**Figure 5. Methodology for Measuring Rtotal**
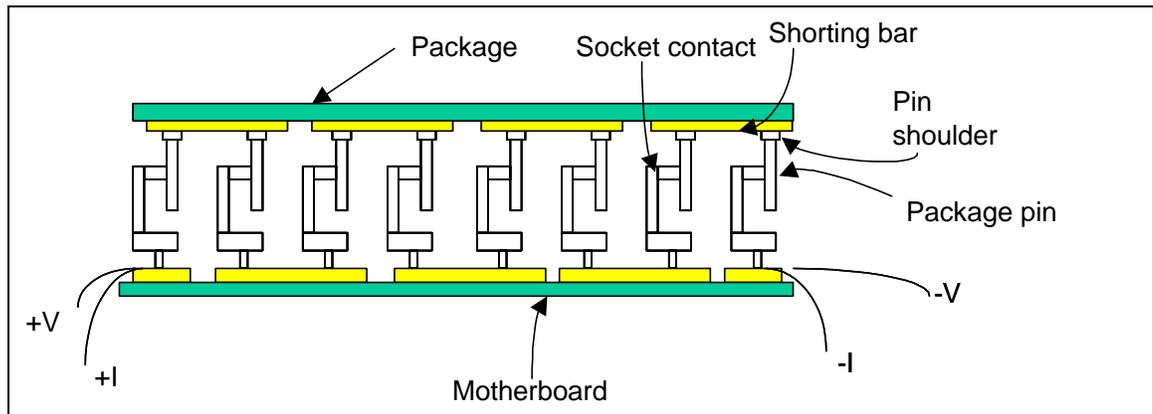
## 4.4.1. Jumper Types

Four types of jumpers (Type A, B1, B2 and PJRC) are used in the Package Test Vehicle (PTV) and are shown in Figure 6.  The mean of Rjumper is therefore different for each type in the calculation of the single pin resistance (see section for calculating single pin resistance).

**Figure 6. Four different jumpers types used in the Package Test Vehicle**
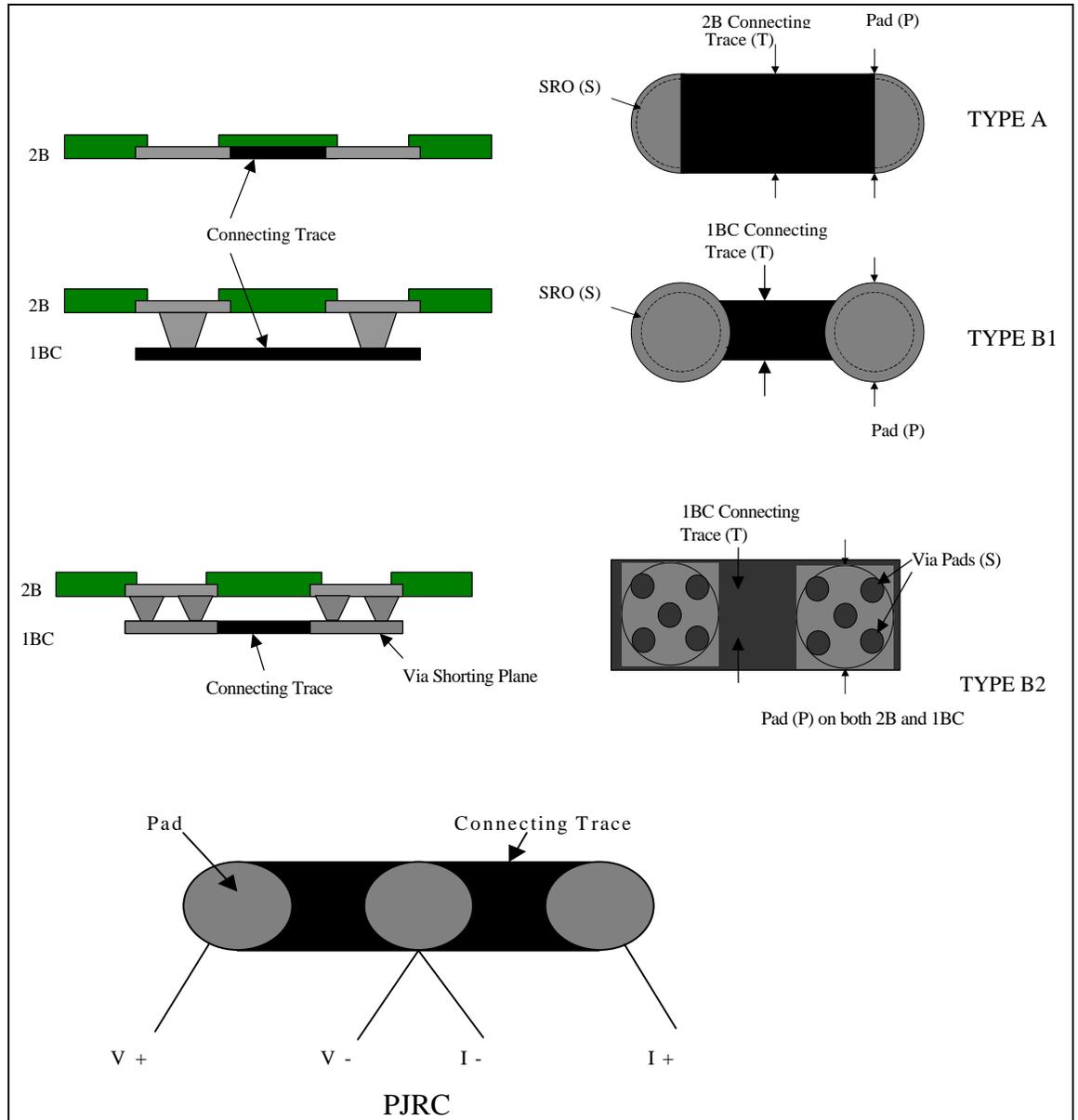
## 4.4.2. Jumper Locations

Physical locations (Pin side view) of the four types of jumpers in the Package test vehicle is shown in Figure 7. Care must be taken to make sure that the correct value of Rjumper(mean) is subtracted from the daisy chains type (A, B1 or B2).

**Figure 7. Location of type A, B1, B2 and PJRC daisy chains from pin side of PTV.**
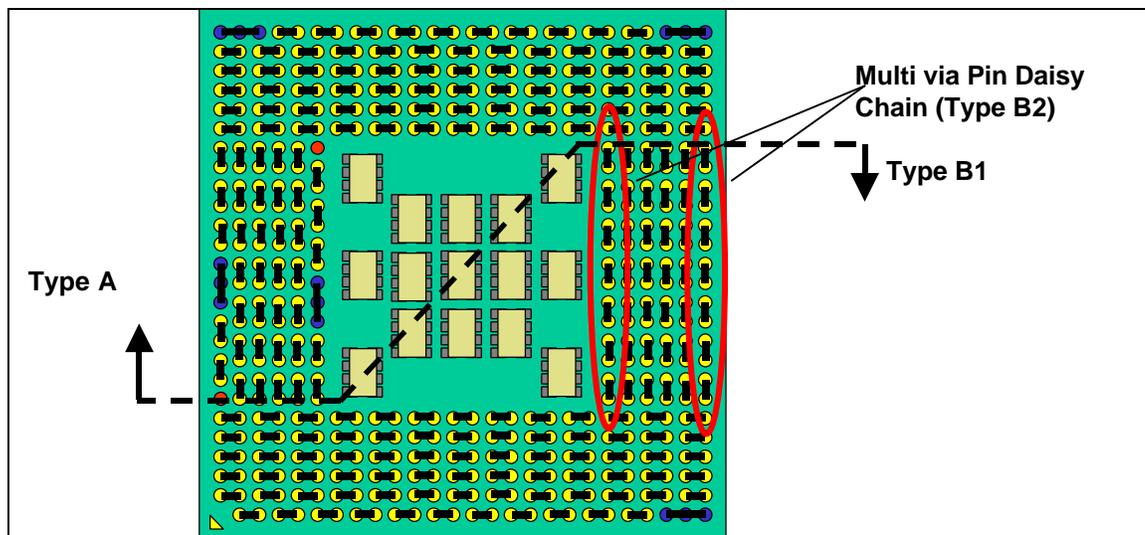


## 4.4.3. Package Test Vehicle and Test Board Netlist

A top view of the test vehicle, Intel part number RF860MCVA, used for resistance measurement is shown in . The different types of daisy chains are also highlighted. There are 36 daisy chain configurations defined on a resistance test board. lists these configurations with the number of pins per each chain and location of each chain. The reference edge finger locations are based on a previously defined Electrical Test Board (ETB), Intel part number A26796-001, used for resistance measurement.

**Figure 8. Electrical Resistance Test Vehicle Top View**
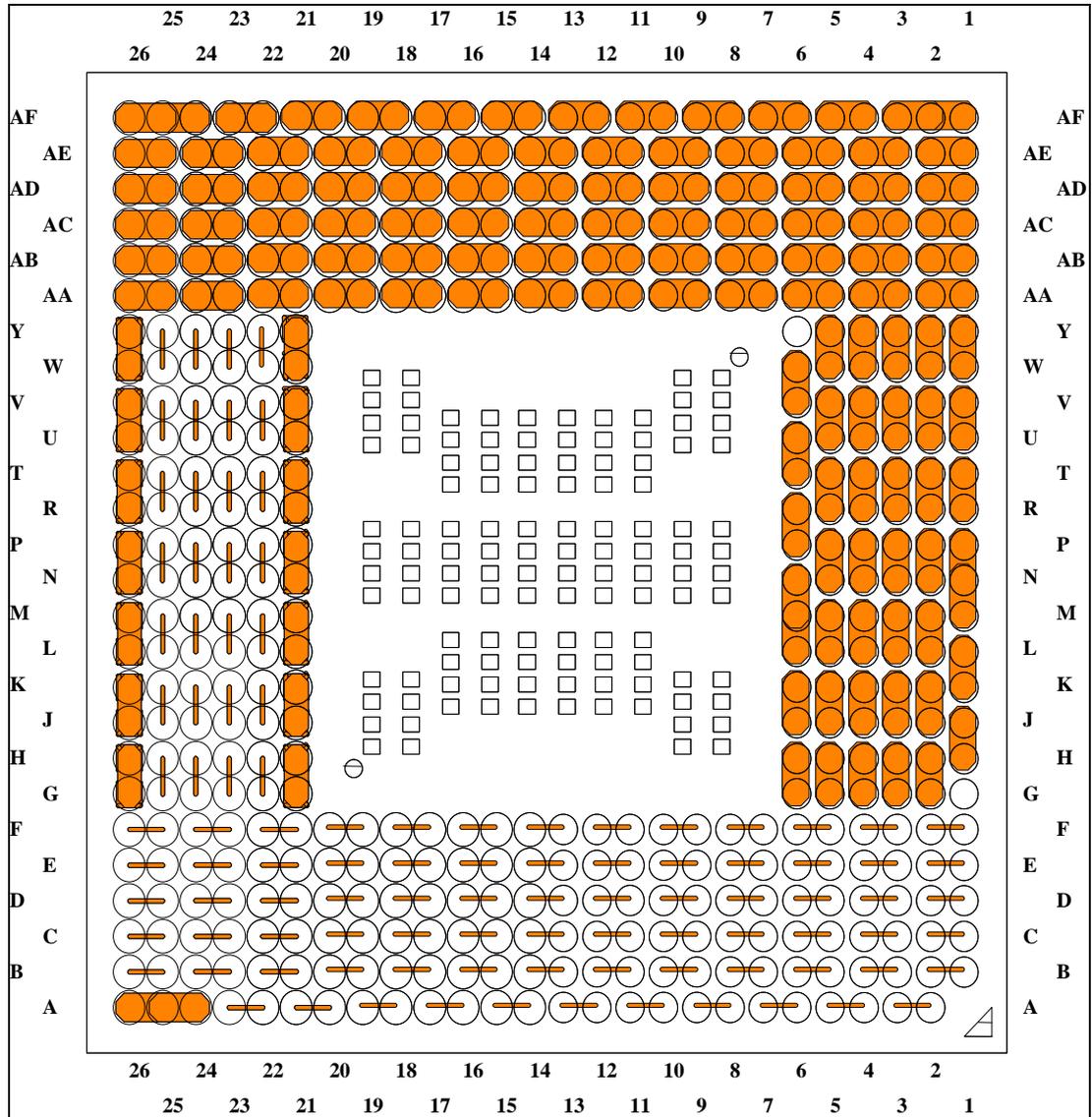
**Table 5. Socket Positions Daisy Chained in Test Board**

| Chain No. | Socket Positions Daisy Chained | # of pins/ chain | DC Endpoints at Socket | | Edge Finger: Hi (reference) | | Edge Finger: Low (reference) | |
|---|---|---|---|---|---|---|---|---|
| | | | Hi | Low | +I | +V | -I | -V |
| 1 | A13-A14, A15-A16, A17-A18, A19-A20, A21-A22, A23-A24 | 12 | A13 | A26 | A125 | A126 | A101 | A102 |
| 2 | B14-B15, B16-B17, B18-B19, B20-B21, B22-B23, B24-B25 | 14 | B13 | B26 | A123 | A124 | A99 | A100 |
| 3 | C14-C15, C16-C17, C18-C19, C20-C21, C22-C23, C24-C25 | 14 | C13 | C26 | A121 | A122 | A97 | A98 |
| 4 | D14-D15, D16-D17, D18-D19, D20-D21, D22-D23, D24-D25 | 14 | D13 | D26 | A119 | A120 | A95 | A96 |
| 5 | E14-E15, E16-E17, E18-E19, E20-E21, E22-E23, E24-E25 | 14 | E13 | E26 | A117 | A118 | A93 | A94 |
| 6 | F14-F15, F16-F17, F18-F19, F20-F21, F22-F23, F24-F25 | 14 | F13 | F26 | A115 | A116 | A91 | A92 |
| 7 | H21-J21, K21-L21, M21-N21, P21-R21, T21-U21, V21-W21 | 14 | G21 | Y21 | A113 | A114 | A89 | A90 |
| 8 | H22-J22, K22-L22, M22-N22, P22-R22, T22-U22, V22-W22 | 14 | G22 | Y22 | A111 | A112 | A87 | A88 |
| 9 | H23-J23, K23-L23, M23-N23, P23-R23, T23-U23, V23-W23 | 14 | G23 | Y23 | A109 | A110 | A85 | A86 |
| 10 | H24-J24, K24-L24, M24-N24, P24-R24, T24-U24, V24-W24 | 14 | G24 | Y24 | A107 | A108 | A83 | A84 |
| 11 | H25-J25, K25-L25, M25-N25, P25-R25, T25-U25, V25-W25 | 14 | G25 | Y25 | A105 | A106 | A81 | A82 |
| 12 | H26-J26, K26-L26, M26-N26, P26-R26, T26-U26, V26-W26 | 14 | G26 | Y26 | A103 | A104 | A79 | A80 |
| 13 | NOT USED | | | | A51 | A52 | A77 | A78 |
| *14 | PJRC - Pin Joint Resistance Circuit | Not defined | M1 | P1 | A49 | A50 | A75 | A76 |
| *15 | PJRC - Pin Joint Resistance Circuit | Not defined | L6 | N6 | A47 | A48 | A73 | A74 |
| *16 | PJRC - Pin Joint Resistance Circuit | Not defined | A26 | A24 | A45 | A46 | A71 | A72 |
| 17 | NOT USED | | | | A43 | A44 | A69 | A70 |

| Chain No. | Socket Positions Daisy Chained | # of pins/chain | DC Endpoints at Socket | | Edge Finger: Hi (reference) | | Edge Finger: Low (reference) | |
|---|---|---|---|---|---|---|---|---|
| | | | Hi | Low | +I | +V | -I | -V |
| *18 | PJRC - Pin Joint Resistance Circuit | Not defined | AF24 | AF26 | | A42 | | A68 |
| *19 | PJRC - Pin Joint Resistance Circuit | Not defined | AF1 | AF3 | | A40 | | A66 |
| 20 | AA14-AA15, AA16-AA17, AA18-AA19, AA20-AA21, AA22-AA23, AA24-AA25 | 14 | AA13 | AA26 | A37 | A38 | A63 | A64 |
| 21 | AB14-AB15, AB16-AB17, AB18-AB19, AB20-AB21, AB22-AB23, AB24-AB25 | 14 | AB13 | AB26 | A35 | A36 | A61 | A62 |
| 22 | AC14-AC15, AC16-AC17, AC18-AC19, AC20-AC21, AC22-AC23, AC24-AC25 | 14 | AC13 | AC26 | A33 | A34 | A59 | A60 |
| 23 | AD14-AD15, AD16-AD17, AD18-AD19, AD20-AD21, AD22-AD23, AD24-AD25 | 14 | AD13 | AD26 | A31 | A32 | A57 | A58 |
| 24 | AE14-AE15, AE16-AE17, AE18-AE19, AE20-AE21, AE22-AE23, AE24-AE25 | 14 | AE13 | AE26 | A29 | A30 | A55 | A56 |
| 25 | AF13-AF14, AF15-AF16, AF17-AF18, AF19-AF20, AF21-AF22, AF23-AF24 | 12 | AF13 | AF26 | A27 | A28 | A53 | A54 |
| 26 | A3-A4, A5-A6, A7-A8, A9-A10, A11-A12 | 12 | A13 | A2 | A125 | A126 | A149 | A150 |
| 27 | B2-B3, B4-B5, B6-B7, B8-B9, B10-B11, B12-B13 | 12 | B13 | B1 | A123 | A124 | A147 | A148 |
| 28 | C2-C3, C4-C5, C6-C7, C8-C9, C10-C11, C12-C13 | 12 | C13 | C1 | A121 | A122 | A145 | A146 |
| 29 | D2-D3, D4-D5, D6-D7, D8-D9, D10-D11, D12-D13 | 12 | D13 | D1 | A119 | A120 | A143 | A144 |
| 30 | E2-E3, E4-E5, E6-E7, E8-E9, E10-E11, E12-E13 | 12 | E13 | E1 | A117 | A118 | A141 | A142 |
| 31 | F2-F3, F4-F5, F6-F7, F8-F9, F10-F11, F12-F13 | 12 | F13 | F1 | A115 | A116 | A139 | A140 |
| 32 | NOT USED | | | | | A114 | | A138 |
| | | | | | | A113 | | A137 |

| Chain No. | Socket Positions Daisy Chained | # of pins/ chain | DC Endpoints at Socket | | Edge Finger: Hi (reference) | | Edge Finger: Low (reference) | |
|---|---|---|---|---|---|---|---|---|
| | | | Hi | Low | +I | +V | -I | -V |
| 33 | NOT USED | | | | | A112 | | A136 |
| | | | | | | A111 | | A135 |
| 34 | NOT USED | | | | | A110 | | A134 |
| | | | | | | A109 | | A133 |
| 35 | NOT USED | | | | | A108 | | A132 |
| | | | | | | A107 | | A131 |
| 36 | NOT USED | | | | | A106 | | A130 |
| | | | | | | A105 | | A129 |
| 37 | NOT USED | | | | | A104 | | A128 |
| | | | | | | A103 | | A127 |
| 38 | NOT USED | | | | | A52 | | A2 |
| | | | | | | A51 | | A1 |
| **39 | H6-J6, K6-L6, N6-P6, R6-T6, U6-V6 | 12 | G6 | W6 | | A50 | | A26 |
| **40 | H5-J5, K5-L5, M5-N5, P5-R5, T5-U5, V5-W5 | 14 | G5 | Y5 | | A48 | | A24 |
| **41 | H4-J4, K4-L4, M4-N4, P4-R4, T4-U4, V4-W4 | 14 | G4 | Y4 | | A46 | | A22 |
| 42 | H3-J3, K3-L3, M3-N3, P3-R3, T3-U3, V3-W3 | 14 | G3 | Y3 | | A44 | | A20 |
| **43 | H2-J2, K2-L2, M2-N2, P2-R2, T2-U2, V2-W2 | 14 | G2 | Y2 | | A42 | | A18 |
| **44 | J1-K1, L1-M1, P1-R1, T1-U1, V1-W1 | 12 | H1 | Y1 | | A40 | | A16 |
| 45 | AA2-AA3, AA4-AA5, AA6-AA7, AA8-AA9, AA10-AA11, AA12-AA13 | 12 | AA13 | AA1 | A37 | A38 | A13 | A14 |
| 46 | AB2-AB3, AB4-AB5, AB6-AB7, AB8-AB9, AB10-AB11, AB12-AB13 | 12 | AB13 | AB1 | A35 | A36 | A11 | A12 |
| 47 | AC2-AC3, AC4-AC5, AC6-AC7, AC8-AC9, AC10-AC11, AC12-AC13 | 12 | AC13 | AC1 | A33 | A34 | A9 | A10 |
| 48 | AD2-AD3, AD4-AD5, AD6-AD7, AD8-AD9, AD10-AD11, AD12-AD13 | 12 | AD13 | AD1 | A31 | A32 | A7 | A8 |
| 49 | AE2-AE3, AE4-AE5, AE6-AE7, AE8-AE9, | 12 | AE13 | AE1 | A29 | A30 | A5 | A6 |

| Chain No. | Socket Positions Daisy Chained | # of pins/ chain | DC Endpoints at Socket | | Edge Finger: Hi (reference) | | Edge Finger: Low (reference) | |
|---|---|---|---|---|---|---|---|---|
| | | | Hi | Low | +I | +V | -I | -V |
| | AE10-AE11, AE12-AE13 | | | | | | | |
| 50 | AF3-AF4, AF5-AF6, AF7-AF8, AF9-AF10, AF11-AF12 | 12 | AF13 | AF1 | A27 | A28 | A3 | A4 |

**NOTES:**

1. Daisy chains are categorized as:

   TYPE A :        18 total    Chain No.:  20,21,22,23,24,25,39,40,41,42,43,4445,46,47,48,49,50.

   TYPE B1: 16 total    Chain No.:  1,2,3,4,5,6,8,9,10,11,26,27,28,29,30,31.

   TYPE B2:        2 total     Chain No.:  7,12.

   TYPE PJRC:     5 total     Chain No.:  14,15,16,18,19.

   Not used        9 total     Chain No.:  13,17,32,33,34,35,36,37,38.

2. * = Pin Joint Resistance Circuit – Not properly set up for 4-wire measurement to define the number of pin. Those chains are not be used for electrical validation.

3. ** = Chain 39,40,41,43,44 (type A) shall not be used for electrical validation since the resistance of shorting bars may vary in Reliability testing.

## 4.4.4.    Determination of Final Mating Resistance

This section provides a procedure for measurement and calculating final mating resistance.

*Note:*    All instrument used shall meet  EIA 364-23A guideline

1.  All resistance measurements must use a 4-wire technique, where the instruments provide two separate circuits.  One is a precision current source to deliver the test current.  The other is a precision voltmeter circuit to measure the voltage drop between the desired points.

2.  These separate circuits can be contained within one instrument, such as a high quality micro-ohmmeter, a stand-alone current source and voltmeter, or the circuits of a data acquisition system.

3.  Measurement accuracy in $\Omega$ is specified as $\pm$ 0.1% of reading, or $\pm$ 0.1 m$\Omega$, whichever is greater.  The vendor is responsible for demonstrating that their instrument(s) can meet this accuracy.

4.  Automation of the measurements can be implemented by scanning the chains through the edge or cable test connector using a switch matrix.  The matrix can be operated by hand, or through software.

5.  Measure $R_{Total}$ for each daisy chain of "package + socket + motherboard" unit.

6.  Measure $R_{jumper}$ for each daisy chain of 30 "package + motherboard" units.  Calculate the mean of Rjumper ( $\overline{R}_{jumper}$ ) from 30 measured sandwich units for each daisy chain.

7.  For each chain, calculate average final mating resistance for each pin within the chain, $R_{Req}$

$$R_{Req} = \frac{R_{Total} - \overline{R}_{jumper}}{N}$$

Where N is the number of pin within the chain

# 4.5. Inductance

Loop inductance of the socket pin is measured from the solder ball side of the socket using a resistance daisy chain test fixture to short the two socket pins, as shown in Figure 9.  Any two balls that are shorted by the test fixture can be used for the inductance measurement.  The figure illustrates the cross-section of the socket and test fixture package with the location of the shorting bar.  Figure 10 shows the test fixture mounted on top of a socket.  After the inductance measurement is made, all the pins will be cut away from the test fixture package as shown in Figure 11. Inductance value measured on the test fixture package without the pins will be used to determine the fixture contribution.  The test fixture must be made from materials that closely match the materials used in the processor.  The part number for the daisy chain test fixture is A00590-002, made by Nanya*.

**Figure 9. Inductance Measurement Technique Cross-Section Illustration**
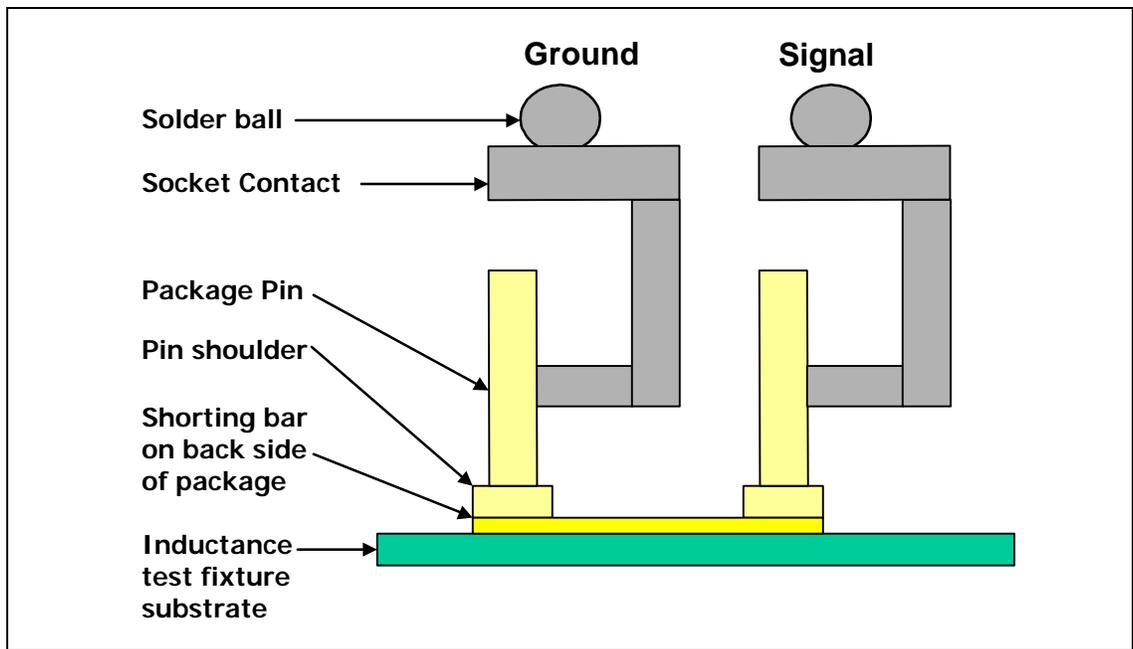


**Figure 10. Picture of Test Fixture Mounted on a Socket**
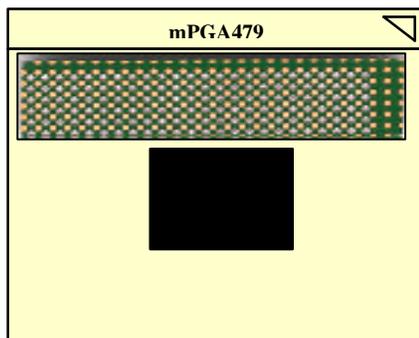
**Figure 11. Inductance Test Fixture Before and After Pins are Cut**
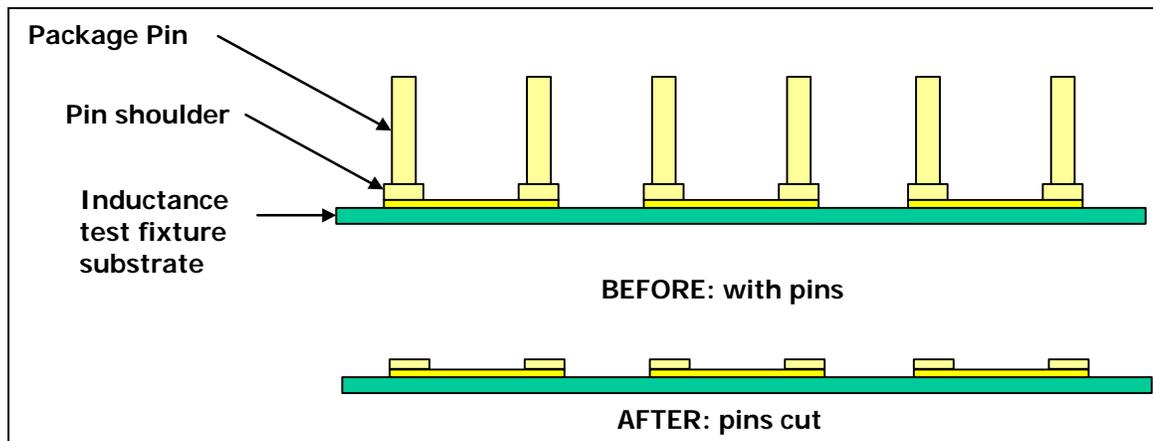


## 4.5.1.   Procedure for Inductance Measurements

### 4.5.1.1.   Measurement Equipment Required

- Equipment - HP8753D Vector Network Analyzer or equivalent
- Robust Probe Station (GTL4040) or equivalent
- Probes - GS1250 & GSG1250 Air-Co-Planar or equivalent
- Calibration – Cascade Calibration Substrates or equivalent
- Measurement objects – Package test vehicles, Sockets, Motherboards

### 4.5.1.2.   Measurement Steps

**1. Equipment setup**

Cables should be connected to the network analyzer and to the probes using the appropriate torque wrench to ensure consistent data collection every time the measurement is performed.

**2. Set VNA**

(a) Bandwidth = 300KHz – 3GHz with 801 points

(b) Averaging Factor = 16

**intel**

**3. Perform Open/Short/Load calibration**

(a) Calibration should be performed at the start of any measurement session.

(b) Please refer to Intel Calibration Document

(c) Create Calibration Kit if necessary for 1st time

(d) Do not perform port extension after calibration

**4. Check to ensure calibration was successfully performed**

**5. With the test fixture package installed on the socket, measure the inductance by probing on each pair of the solder balls.**

(a) Call this inductance reading $L_{socket-assembly}$

(b) Export data into MDS/ADS, or capture data at frequency specified by Table 2.

**6. Measure the inductance by probing on the shoulder of the test fixture with the pins cut as shown in Figure 11. .**

(a) Call this $L_{sandwich}$.

(b) Measure 30 units.  Note: the package for 30 units must be chosen from different lots.  Use 5 different lots, 6 units from each lot.

(c) Export data into MDS/ADS, or capture data at frequency specified in Table 2.

(d) Calculate the mean of the 30 readings and call this $\overline{L}_{sandwich}$ .

For each pin pair, calculate:

$$L_{socket} = L_{socket\ assembly} - \overline{L}_{sandwich}$$

It means $\overline{L}_{sandwich}$ will be subtracted from each $L_{socket\ assembly}$ and the result will be compared with the spec value for each individual pin pair.

# 4.6.        Pin-to-Pin Capacitance:

Pin-to-pin capacitance shall be measured using the top fixture (test vehicle) shown in Figure 12, which contains pins that will connect to the socket. The figure also shows the area to be cut out from the test fixture, and the R1 pin pair. Figure 13 shows the fixture as it appears after being cut out.

**Figure 12. Top View of the Capacitance Test Fixture With Dashed Line Showing Cut Out Area**
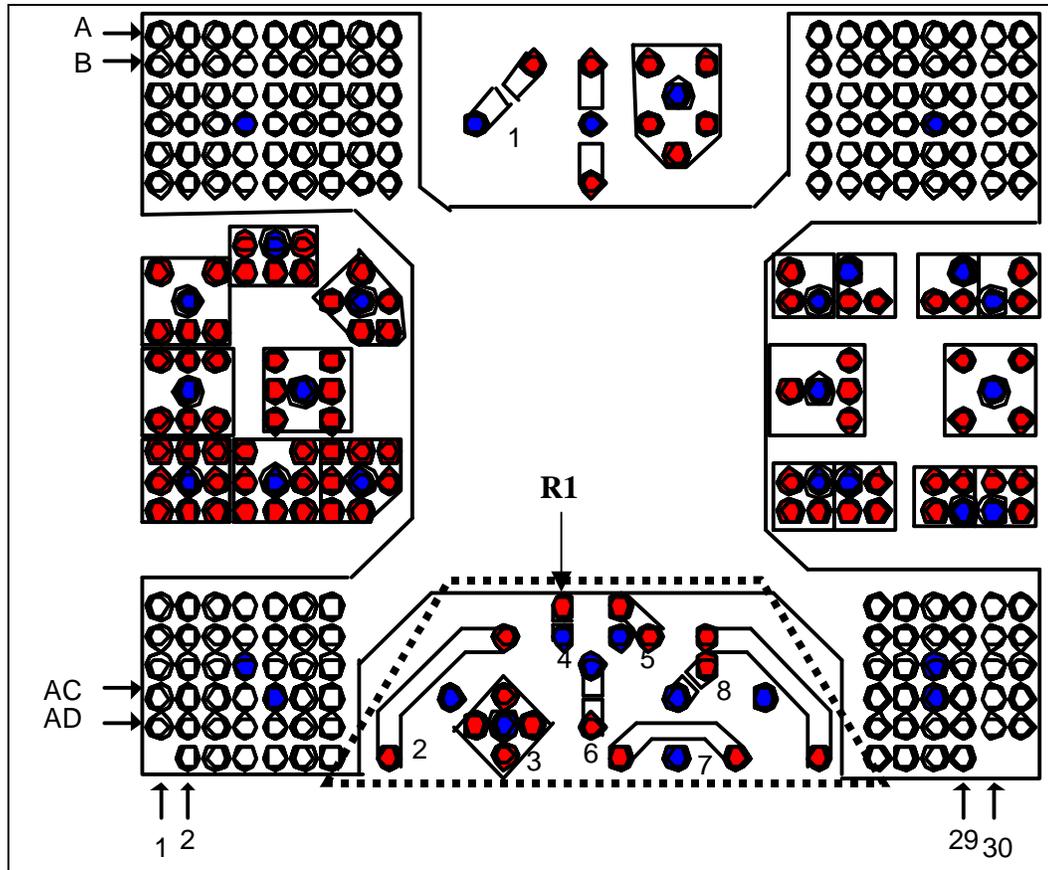


**Figure 13. Picture of Capacitance Test Fixture Cut Out (Arrow Indicates Configuration R1 Test Structure)**
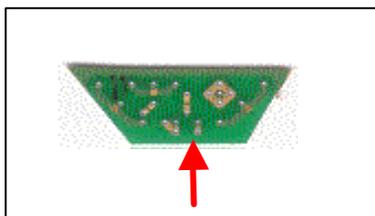
Figure 14 shows the capacitance measurement fixture cross-section and the capacitance measurement methodology.  After the measurement is made, the pins are cut away as shown in Figure 15.  The fixture with the cut pins is used to calibrate out the fixture contribution.  Capture data at the frequency specified in Table 2. The part number of the test fixture shown in Figure 12 is 739901-002

**Figure 14. Capacitance Measurement Technique Cross-Section Illustration**
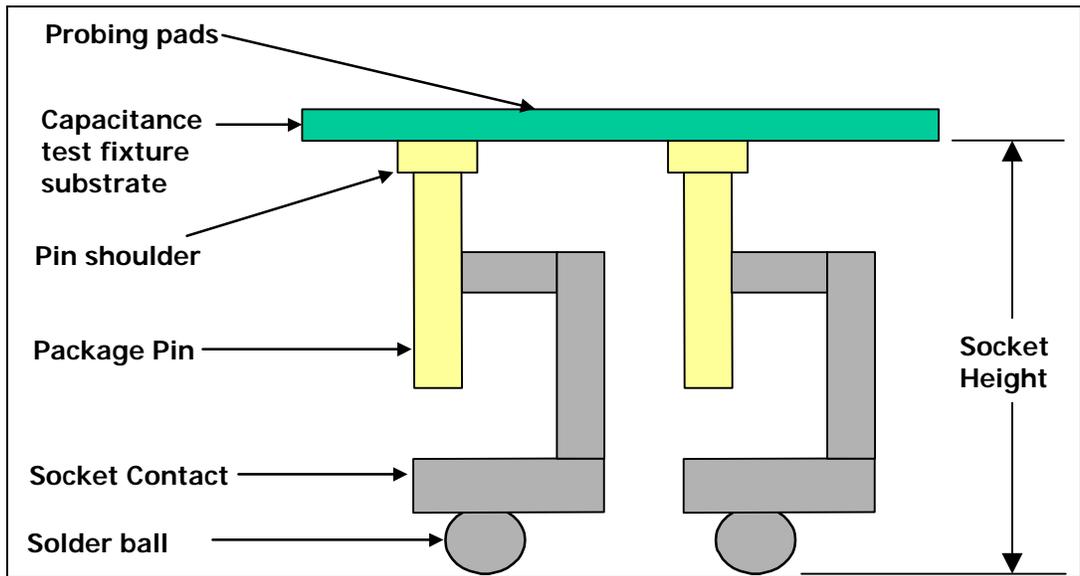


**Figure 15. Capacitance Test Fixture Before and After Pins are Cut**
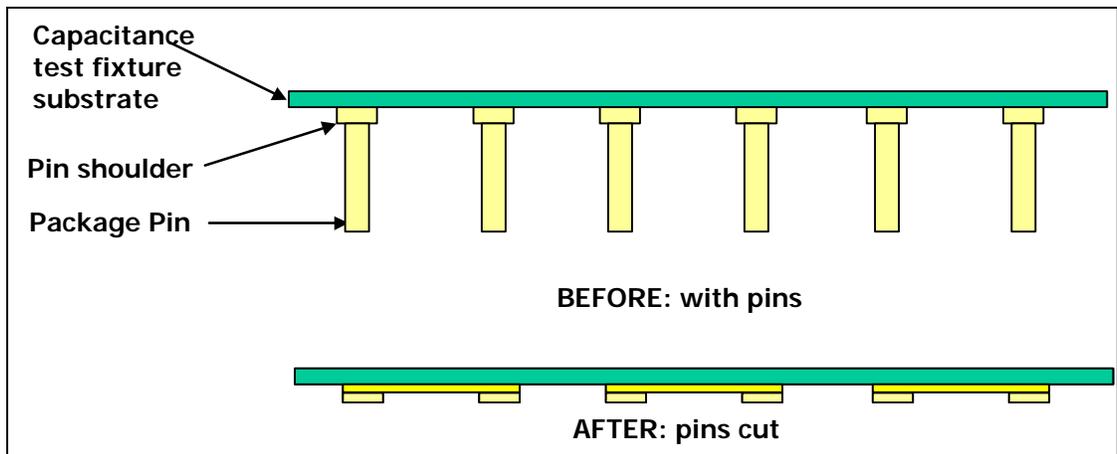


## 4.6.1.    Procedure for Capacitance Measurements

### 4.6.1.1.    Measurement Equipment Required

- HP8753D Vector Network Analyzer or equivalent
- Robust Probe Station (GTL4040) or equivalent
- Probes - GS1250 & GSG1250 Air-Co-Planar or equivalent

- Calibration – Cascade Calibration Substrates or equivalent
- Measurement objects – Package test vehicles, Sockets, Motherboards

## 4.6.1.2.    Measurement Steps

**1. Equipment setup**

Cables should be connected to the network analyzer and to the probes using the appropriate torque wrench to ensure consistent data collection every time the measurement is performed.

**2. Set VNA**
- Bandwidth = 300KHz – 3GHz with 801 points
- Averaging Factor = 16

**3. Perform Open/Short/Load calibration**

(a) Calibration should be performed at the start of any measurement session.

(b) Please refer to Intel Calibration Document

(c) Create Calibration Kit if necessary for 1st time

(d) Do not perform port extension after calibration

**4. Check to ensure calibration successfully performed**

**5. Measure the capacitance of the test vehicle mounted on the socket for the Configuration R1.**

(a) Call this Csocket_assembly.

(b) Export data into the MDS/ADS, or capture data at frequency specified in Table 2.

# 5.       Reliability Targets

Socket supplier shall design and validate their socket to the reliability and life target based on the expected use condition and environmental data supplied by the PC OEM.  For Intel's socket validation activities, the use environment expectations are listed in Table 6, with an expected fail rate of 1% at 7 years and 3% at 10 years.

**Table 6. Expected Field Use Environment**

| Use Environment Expectations | 7 Year Life Expectation |
|---|---|
| Slow small internal gradient changes due to external ambient (temperature cycle or externally heated)-**Temperature Cycle** | 3000 cycles with a mean $\Delta T = 40^O C$ |
| High ambient moisture during low-power state (operating voltage)- **THB/HAST** | 62K  hours at $30^O C$/85%RH |
| High Operating temperature and short duration high temperature exposures - **Bake** | 62K  hours at Max operating temperature |
| Fast, large gradient On/off (to max operating temperature) (power cycle or internally heated including power save features)**- Power Cycle** | 7500 cycles |
| **Mechanical Shock** | Trapezoidal 50g.  Velocity change 170 in./sec 3 drops in each of 6 directions |
| **Mechanical Vibration** | 5 Hz - 20 Hz  .01 g2/Hz sloping up to .02 g2/Hz  20 Hz - 500 Hz  .02 g2/Hz 3.13 gRMS, random10 minutes/axis |
| **Operating Temperature** | $0^O C$ to $105^O C$ |

## 5.1. Reliability Validation Testing

The Reliability Test Criteria used by Intel to validate the mPGA479M socket was developed using the knowledge-based reliability evaluation methodology.  Test conditions and duration are dependent on the acceleration factor of each possible failure mode, which is derived from the mechanical model, industry information, test data, or past experience.  A simplified process flow of this methodology can be seen in Figure 16.

A more detailed description of this methodology can be found at:
http://developer.intel.com/design/packtech

or by ordering a hardcopy from Intel, document number 245162-001, dated March 1999, under title "Knowledge Based Reliability Evaluation of New Package Technologies Utilizing Use Conditions".

**Figure 16. Flow Chart of Knowledge-Based Reliability Evaluation Methodology**
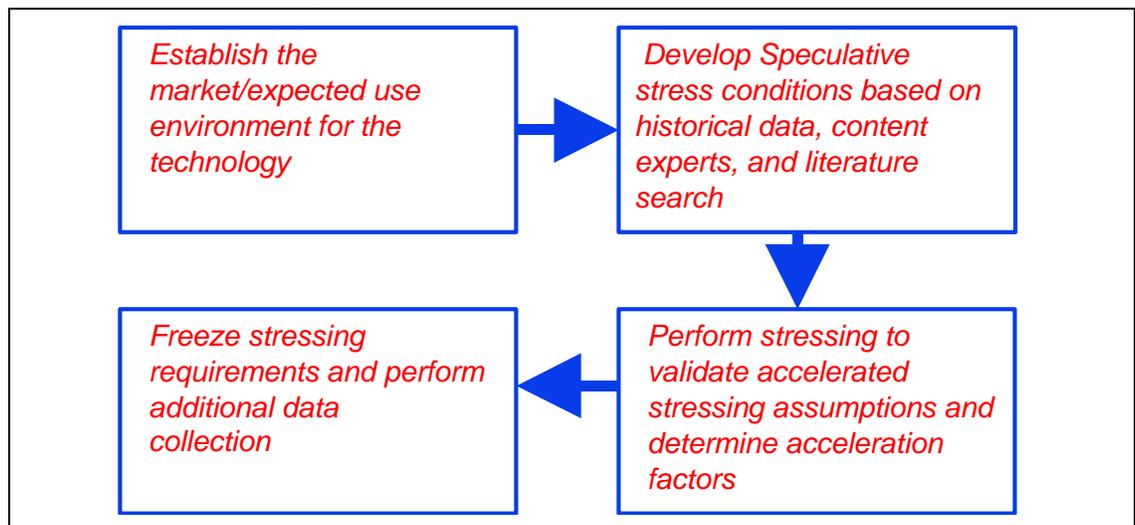
# 6. Safety Guidelines

Design, including materials, shall be consistent with the manufacture of units that meet the following safety design guidelines:

1. UL 1950 most current editions
2. CSA 950 most current edition
3. EN60 950 most current edition and amendments
4. IEC60 950 most current edition and amendments
5. SEMI S2-93 Product Safety Guidelines most current edition and amendments

# *Appendix Z.1: Package Generic Mechanical Drawing*

**Figure 17. Micro-FCPGA Package Assembly (no IHS) Page 1 of 3**

**Figure 18. Micro-FCPGA Package Assembly (no IHS) Page 2 of 3**
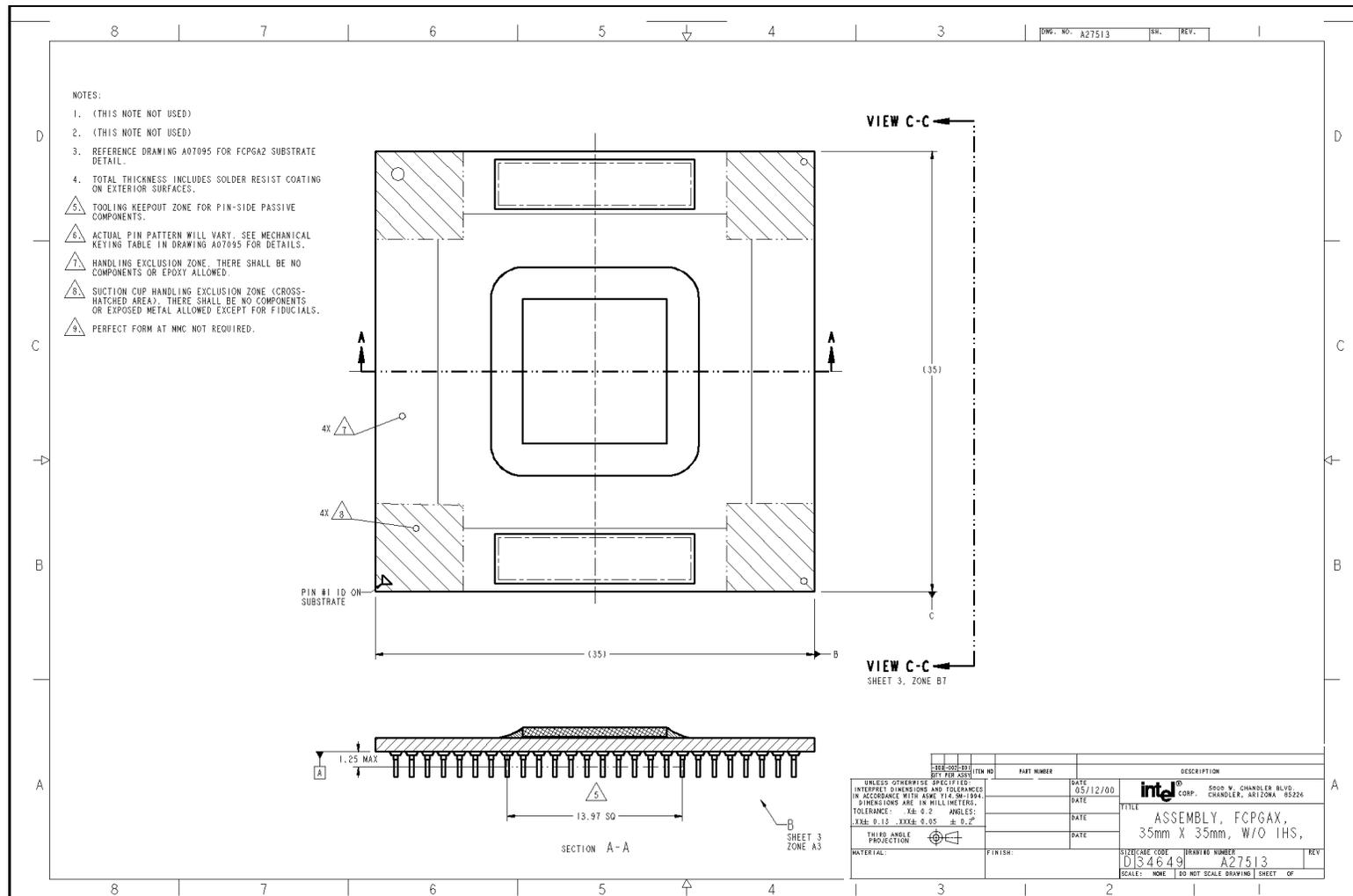
**Figure 19. Micro-FCPGA Package Pin Shoulder Details (Page 3 of 3)**
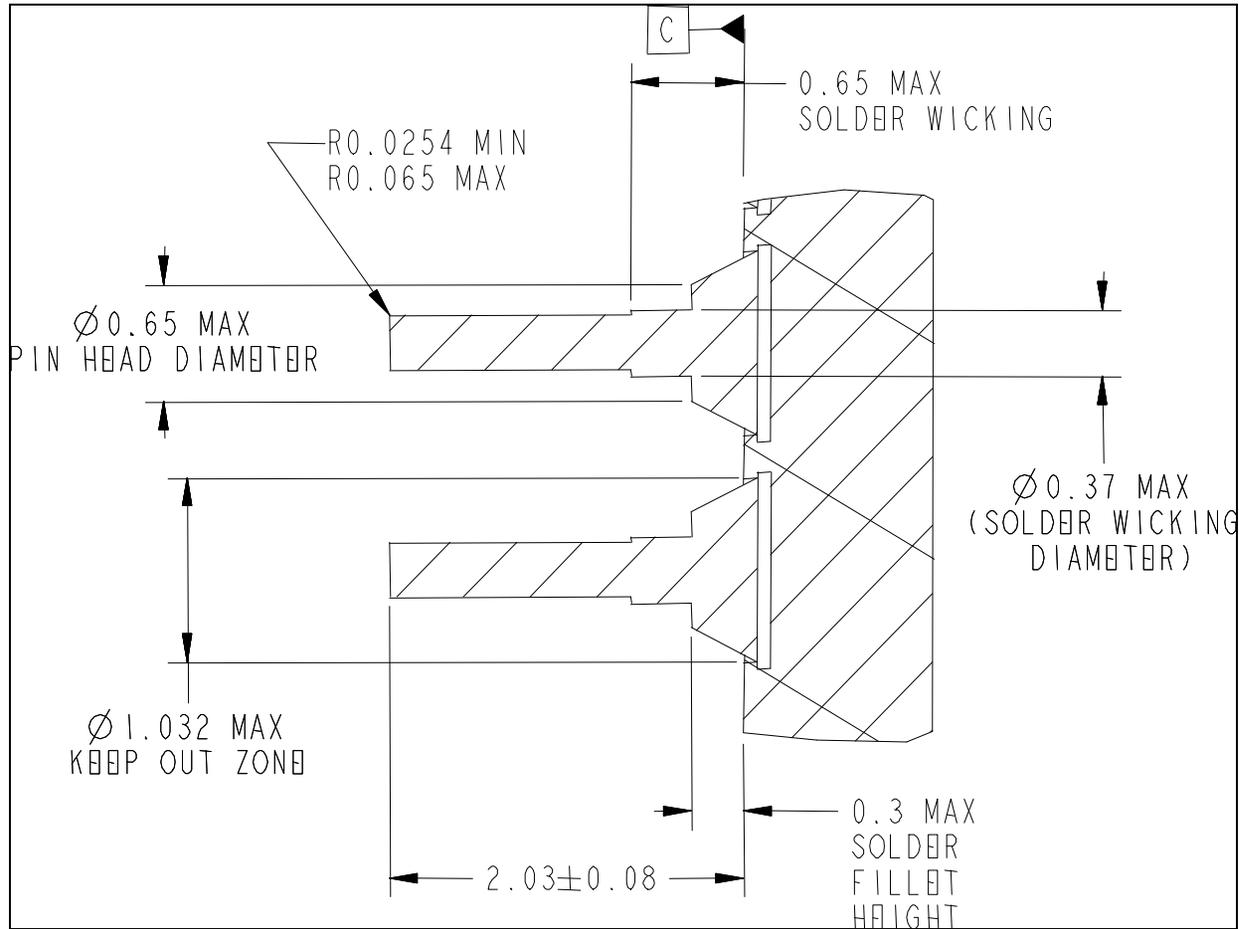
# *Appendix Z.2: Motherboard Generic Mechanical Drawing (REFERENCE ONLY)*

*Note:* Socket dimensions shown are nominal and do not account for solderball pattern true position tolerance to socket body. also, the socket footprint as shown does not account for motherboard pad pattern true position tolerance to the four hole pattern nor does it account for the surface mount manufacturer's capabilities for placing the socket. surface mount are not included.

### Figure 20. Motherboard Landing Zone
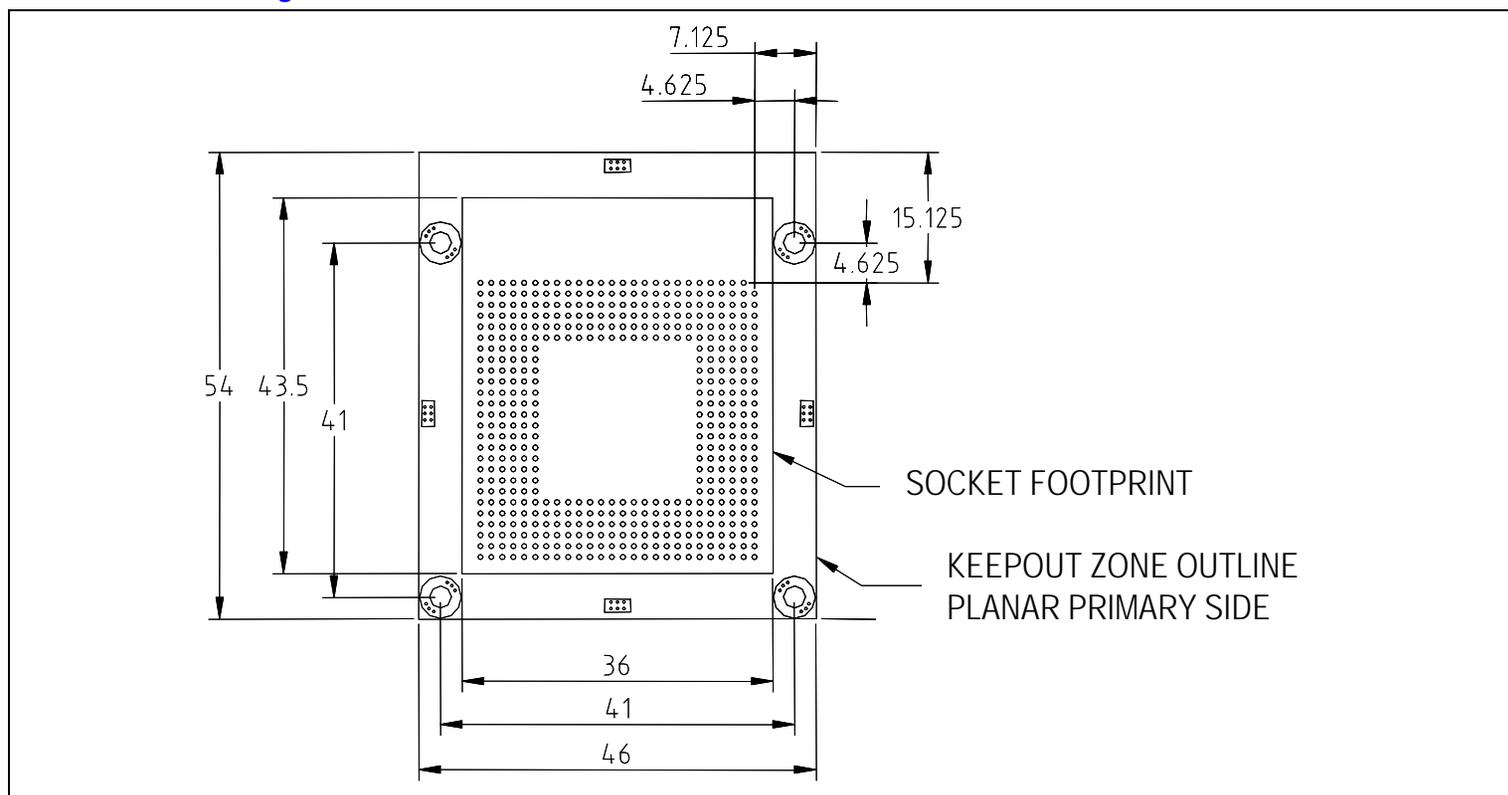
# *Appendix Z.3: Socket Generic Mechanical Drawing*

**Figure 21. Generic Socket Illustration (Page 1 of 2)**



NOTES:

1. THE PURPOSE OF THIS DRAWING IS TO ESTABLISH THE MECHANICAL FORM FACTOR OF THE SOCKET. DRAWING IS NOT INTENDED TO SHOW INTERNAL DETAIL OF SOCKET WHICH MAY VARY FROM SUPPLIER TO SUPPLIER.
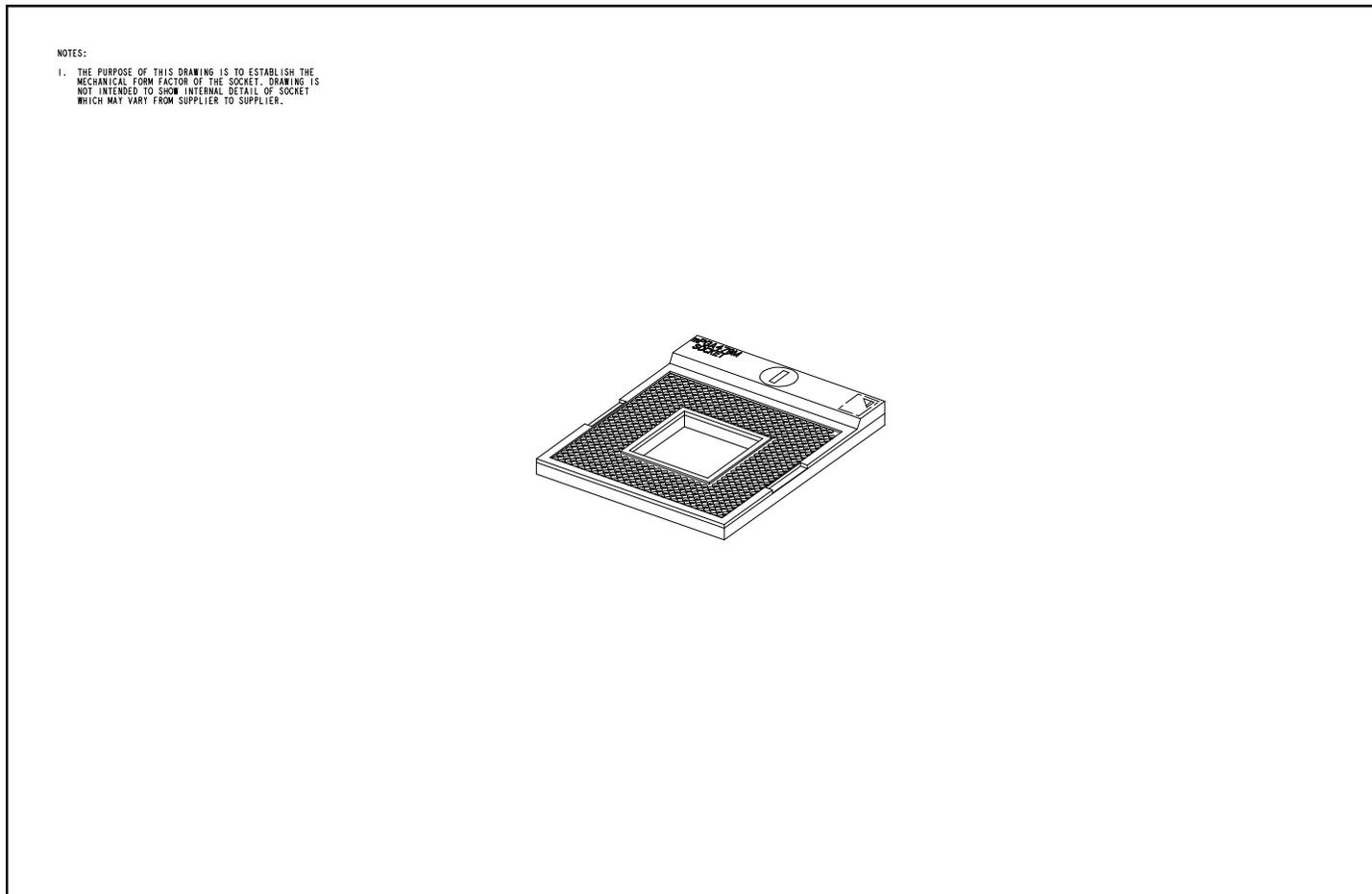
**Figure 22. Generic Socket Illustration (Page 2 of 2)**



mPGA479M SOCKET ASSEMBLY