Intel Ethernet Controllers Timing Device Selection Guide

Application Note (AP-419)

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Revision History

Revision	Revision Date	Description
0.3	May 2000	Initial release (Intel Confidential - Controlled Access).
0.4	Jun 2000	Removed Intel Confidential status.
1.0	Sep 2003	Updated for the 8254x controllers.
1.1	Oct 2003	Added Appendix A, “Measuring LAN Reference Frequency Using a Frequency Counter”.
1.2	Sep 2004	Updated Table 1 to reflect new crystal parameters. Added Appendix B, “GigConf.exe Register Settings for 82541GI(EI) and 82547GI(EI)”.

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1.0 Introduction and Scope

This application note provides information regarding frequency control devices, including crystals and oscillators, for use with all Intel® Ethernet controllers. Several suitable frequency control devices are available; none of which present any unusual challenges in selection. The concepts documented herein are applicable to other data communication circuits, including Physical Layer devices (PHYs).

The Intel® Ethernet controllers contain amplifiers which, when used with the specific external components, form the basis for feedback oscillators. These oscillator circuits, which are both economical and reliable, are described in more detail throughout this document.

The Intel® Ethernet controllers also have bus clock input functionality, however a discussion of this feature is beyond the scope of this document, and will not be addressed.

The chosen frequency control device vendor should be consulted early in the design cycle. Crystal and oscillator manufacturers familiar with networking equipment clock requirements may provide assistance in selecting an optimum, low-cost solution.

The following list of references provide supplemental background material:

- *Oscillation Circuit Design Guide* Application Note, Epson Electronics America, Inc. (www.eea.epson.com).
- *Quartz Crystal Theory of Operation and Design Notes*. Fox Electronics (www.foxonline.com).
- *Crystal Technical Glossary.* Fox Electronics.
- *Crystal Frequently Asked Questions*. Fox Electronics.
- *Resonator Terminology and Formulas.* Piezo Technology, Inc. (www.piezotech.com).
- *New Crystal Specification for 82541EI/GI and 82547EI/GI*, Technical Advisory 162. Intel Corporation.
- *Indirect Measurement of Transmitter Reference Frequency,* Application Note (AP-457). Intel Corporation.

2.0 Frequency Control Component Types

Several types of third-party frequency reference components are currently marketed. A discussion of each follows, listed in preferred order.

2.1 Quartz Crystal

Quartz crystals are generally considered to be the mainstay of frequency control components due to their low cost and ease of implementation. They are available from numerous vendors in many package types and with various specification options.

2.2 Fixed Crystal Oscillator

A packaged fixed crystal oscillator is comprised of an inverter, a quartz crystal, and passive components conveniently packaged together. The device renders a strong, consistent square wave output. Oscillators used with microprocessors are supplied in many configurations and tolerances.

Crystal oscillators should be restricted to use in special situations, such as shared clocking among devices or multiple controllers. As clock routing can be difficult to accomplish, it is preferable to provide a separate crystal for each device.

For Intel® Ethernet controllers, it is acceptable to overdrive the internal inverter by connecting a 25 MHz external oscillator to the X1 lead, leaving the X2 lead unconnected. The oscillator should be specified to drive CMOS logic levels, and the clock trace to the controller should be as short as possible. Controller specifications typically call for a 40% (minimum) to 60% (maximum) duty cycle and a ±50 ppm frequency tolerance.

Note: Please contact your Intel Customer Representative to obtain the most current device documentation prior to implementing this solution.

2.3 Programmable Crystal Oscillators

A programmable oscillator can be configured to operate at many frequencies. The device contains a crystal frequency reference and a phase lock loop (PLL) clock generator. The frequency multipliers and divisors are controlled by programmable fuses.

A programmable oscillator's accuracy depends heavily on the Ethernet controller's differential transmit lines. The Physical Layer (PHY) uses the clock input from the device to drive a differential Manchester (for 10 Mbps operation), an MLT-3 (for 100 Mbps operation) or a PAM-5 (for 1000 Mbps operation) encoded analog signal across the twisted pair cable. These signals are referred to as self-clocking, which means the clock must be recovered at the receiving link partner. Clock recovery is performed with another PLL that locks onto the signal at the other end.

PLLs are prone to exhibit frequency jitter. The transmitted signal can also have considerable jitter even with the programmable oscillator working within its specified frequency tolerance. PLLs must be designed carefully to lock onto signals over a reasonable frequency range. If the transmitted signal has high jitter and the receiver's PLL loses its lock, then bit errors or link loss can occur.

PHY devices are deployed for many different communication applications. Some PHYs contain PLLs with marginal lock range and cannot tolerate the jitter inherent in data transmission clocked with a programmable oscillator. The American National Standards Institute (ANSI) X3.263-1995 standard test method for transmit jitter is not stringent enough to predict PLL-to-PLL lock failures, therefore, the use of programmable oscillators is generally not recommended.

2.4 Ceramic Resonator

Similar to a quartz crystal, a ceramic resonator is a piezoelectric device. A ceramic resonator typically carries a frequency tolerance of ±0.5%, – inadequate for use with Intel® Ethernet controllers, and therefore, should not be utilized.

3.0 Crystal Selection Parameters

All crystals used with Intel® Ethernet controllers are described as “AT-cut,” which refers to the angle at which the unit is sliced with respect to the long axis of the quartz stone.

Table 1 lists the crystal electrical parameters and provides suggested values for typical designs. These parameters are described in the following subsections.

Table 1. Crystal Parameters

Parameter	Suggested Value
Vibrational Mode	Fundamental
Nominal Frequency	25.000 MHz at 25° C (required)
Frequency Tolerance	• ±30 ppm recommended • ±50 ppm across the entire operating temperature range (required by IEEE specifications)
Temperature Stability	±100 ppm at 0° C to 70° C
Calibration Mode	Parallel
Load Capacitance	• 16 pF to 20 pF • 18 pF for the 82541GI(EI) and 82547GI(EI)
Shunt Capacitance	6 pF maximum
Equivalent Series Resistance	• 50 Ω maximum • 20 Ω maximum for the 82541GI(EI) and 82547GI(EI)
Drive Level	0.5 mW maximum
Aging	±5 ppm per year maximum

3.1 Vibrational Mode

Crystals in the above-referenced frequency range are available in both fundamental and third overtone. Unless there is a special need for third overtone, use fundamental mode crystals.

At any given operating frequency, third overtone crystals are thicker and more rugged than fundamental mode crystals. Third overtone crystals are more suitable for use in military or harsh industrial environments. Third overtone crystals require a trap circuit (extra capacitor and inductor) in the load circuitry to suppress fundamental mode oscillation as the circuit powers up. Selecting values for these components is beyond the scope of this document.

3.2 Nominal Frequency

Intel® Ethernet controllers use a crystal frequency of 25.000 MHz. The 25 MHz input is used to generate a 125 MHz transmit clock for 100BASE-TX and 1000BASE-TX operation – 10 MHz and 20 MHz transmit clocks, for 10BASE-T operation.

3.3 Frequency Tolerance

The frequency tolerance for an Ethernet physical layer device is dictated by the IEEE 802.3 specification as ±50 parts per million (ppm). This measurement is referenced to a standard temperature of 25° C. Intel recommends a frequency tolerance of ±30 ppm.

3.4 Temperature Stability and Environmental Requirements

Temperature stability is a standard measure of how the oscillation frequency varies over the full operational temperature range (and beyond). Several optional temperature ranges are currently available, including -40° C to +85° C for industrial environments. Some vendors separate operating temperatures from temperature stability. Manufacturers may also list temperature stability as 50 ppm in their data sheets.

Note: Crystals also carry other specifications for storage temperature, shock resistance, and reflow solder conditions. Crystal vendors should be consulted early in the design cycle to discuss the application and its environmental requirements.

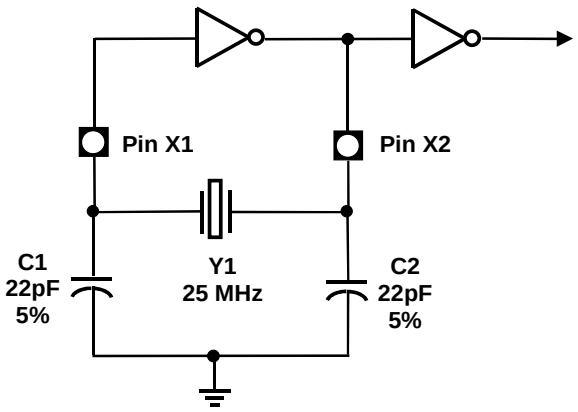
3.5 Calibration Mode

The terms “series-resonant” and “parallel-resonant” are often used to describe crystal oscillator circuits. Specifying parallel mode is critical to determining how the crystal frequency is calibrated at the factory.

A crystal specified and tested as series resonant oscillates without problem in a parallel-resonant circuit, but the frequency is higher than nominal by several hundred parts per million. The purpose of adding load capacitors to a crystal oscillator circuit is to establish resonance at a frequency higher than the crystal’s inherent series resonant frequency.

Figure 1 illustrates a simplified schematic of the 82551QM's oscillator circuit. Note that 8254x controllers are similar. The crystal and the capacitors form a feedback element for the internal inverting amplifier. This combination is called parallel-resonant, because it has positive reactance at the selected frequency. In other words, the crystal behaves like an inductor in a parallel LC circuit. Oscillators with piezoelectric feedback elements are also known as "Pierce" oscillators.

Figure 1. 82551QM Oscillator Circuit



3.6 Load Capacitance

The formula for crystal load capacitance is as follows:

$$C_L = \frac{(C1 \cdot C2)}{(C1 + C2)} + C_{stray}$$

where C1 = C2 = 22 pF (as suggested in most Intel reference designs)

and C_{stray} = allowance for additional capacitance in pads, traces and the chip carrier within the Ethernet controller package

An allowance of 3 pF to 7 pF accounts for lumped stray capacitance. The calculated load capacitance is 16 pF with an estimated stray capacitance of about 5 pF.

Individual stray capacitance components can be estimated and added. For example, surface mount pads for the load capacitors add approximately 2.5 pF in parallel to each capacitor. This technique is especially useful if Y1, C1 and C2 must be placed farther than approximately one-half (0.5) inch from the controller. It is worth noting that thin circuit boards generally have higher stray capacitance than thick circuit boards.

Standard capacitor loads used by crystal manufacturers include 16 pF, 18 pF and 20 pF. Any of these values will generally operate with the controller. However, a difference of several picofarads between the calibrated load and the actual load will pull the oscillator slightly off frequency.

The oscillator frequency should be measured with a precision frequency counter where possible. The 8255x Fast Ethernet controller has a FLA [16]/CLK25 signal output for this purpose. The load specification or values of C1 and C2 should be fine tuned for the design. As the actual capacitance load increases, the oscillator frequency decreases.

Note: C1 and C2 may vary by as much as 5% (approximately 1 pF) from their nominal values.

3.7 Shunt Capacitance

The shunt capacitance parameter is relatively unimportant compared to load capacitance. Shunt capacitance represents the effect of the crystal's mechanical holder and contacts. The shunt capacitance should equal a maximum of 6 pF (7 pF is also acceptable).

3.8 Equivalent Series Resistance

Equivalent Series Resistance (ESR) is the real component of the crystal's impedance at the calibration frequency, which the inverting amplifier's loop gain must overcome. ESR varies inversely with frequency for a given crystal family. The lower the ESR, the faster the crystal starts up. Use crystals with an ESR value of 50 Ω or better.

Note: Check the specific controller documentation carefully; some devices may have tighter ESR requirements. For example, Intel recommends that 82541GI/EI and 82547GI/EI devices use crystals with an ESR value of 20 Ω or less.

3.9 Drive Level

Drive level refers to power dissipation in use. The allowable drive level for a Surface Mounted Technology (SMT) crystal is less than its through-hole counterpart, because surface mount crystals are typically made from narrow, rectangular AT strips, rather than circular AT quartz blanks.

Some crystal data sheets list crystals with a maximum drive level of 1 mW. However, Intel® Ethernet controllers drive crystals to a level less than the suggested 0.5 mW value. This parameter does not have much value for on-chip oscillator use.

3.10 Aging

Aging is a permanent change in frequency (and resistance) occurring over time. This parameter is most important in its first year because new crystals age faster than old crystals. Use crystals with a maximum of ±5 ppm per year aging.

Appendix A: Measuring LAN Reference Frequency Using a Frequency Counter

A.1 Background

To comply with IEEE specifications for 10/100 Mbps and 10/100/1000Base-T Ethernet LAN, the transmitter reference frequency must be correct and accurate within ±50 parts per million (ppm).

Note: Intel recommends a frequency tolerance of ±30 (ppm).

Most Intel LAN devices will operate properly with a 25.000 MHz reference crystal, provided it meets the recommended requirements for frequency stability, equivalent series resistance at resonance (ESR), and load capacitance.

Most circuits for series resonant crystals include two discrete capacitors (typically C1 and C2), with values between 5 pF and 36 pF.

The most accurate way to determine the appropriate value for the discrete capacitors is to install the approximately correct values for C1 and C2. Next, a frequency counter should be used to measure the transmitter reference frequency (or transmitter reference clock).

- If the transmitter reference frequency is more than 20 ppm below the target frequency, then the values for C1 and C2 are too big and should be decreased.
- If the transmitter reference frequency is more than 20 ppm above the target frequency, then the values for C1 and C2 are too small and should be increased.

This Appendix provides instructions and illustrations that explain how to use a frequency counter and probe to determine the Ethernet LAN device transmit center frequency. An example describing how to calculate the frequency accuracy of the measured and averaged center frequency with respect to the target center frequency is also included.

A.2 Required Test Equipment

- Tektronix CMC-251, or similar high resolution, digital counter
- Tektronix P6246, or similar high bandwidth, low capacitance (less than 1 pF) probe
- Tektronix 1103, or similar probe power supply or probe amplifier
- BNC, 50-ohm coaxial cable (less than 6 feet long)
- System with power supply and test software for the LAN circuit to be tested

A.3 Reference Crystal

The normal tolerances of the discrete crystal components can contribute to small frequency offsets with respect to the target center frequency. To minimize the risk of tolerance-caused frequency offsets causing a small percentage of production line units to be outside of the acceptable frequency range, it is important to account for those shifts while empirically determining the proper values for the discrete loading capacitors, C1 and C2.

Even with a perfect support circuit, most crystals will oscillate slightly higher or slightly lower than the exact center of the target frequency. Therefore, frequency measurements (which determine the correct value for C1 and C2) should be performed with an ideal reference crystal. When the capacitive load is exactly equal to the crystal's load rating, an ideal reference crystal will be perfectly centered at the desired target frequency.

A.3.1 Reference Crystal Selection

There are several methods available for choosing the appropriate reference crystal:

- If a Saunders and Associates (S&A) crystal network analyzer is available, then discrete crystal components can be tested until one is found with zero or nearly zero ppm deviation (with the appropriate capacitive load). A crystal with zero or near zero ppm deviation will be a good reference crystal to use in subsequent frequency tests to determine the best values for C1 and C2.
- If a crystal analyzer is not available, then the selection of a reference crystal can be done by measuring a statistically valid sample population of crystals, which has units from multiple lots and approved vendors. The crystal, which has an oscillation frequency closest to the center of the distribution, should be the reference crystal used during testing to determine the best values for C1 and C2.
- It may also be possible to ask the approved crystal vendors or manufacturers to provide a reference crystal with zero or nearly zero deviation from the specified frequency when it has the specified CLoad capacitance.

When choosing a crystal, customers must keep in mind that to comply with IEEE specifications for 10/100 and 10/100/1000Base-T Ethernet LAN, the transmitter reference frequency must be precise within ±50 ppm. Intel® recommends customers to use a transmitter reference frequency that is accurate to within ±30 ppm to account for variations in crystal accuracy due to crystal manufacturing tolerance.

Note: For the 82541GI(EI) and 82547GI(EI) devices, Intel® recommends choosing a crystal with a ESR value of 20 Ω or less, an equivalent Cload of 18 pF, and a maximum of 30 ppm frequency shift. Cload is defined to be the load capacitance of the crystal, specified by the crystal vendor.

A.4 Circuit Board

Since the dielectric layers of the circuit board are allowed some reasonable variation in thickness, the stray capacitance from the printed board (to the crystal circuit) will also vary. If the thickness tolerance for the outer layers of dielectric are controlled within ±17 percent of nominal, then the circuit board should not cause more than ±2 pF variation to the stray capacitance at the crystal. When tuning crystal frequency, it is recommended that at least three circuit boards are tested for frequency. These boards should be from different production lots of bare circuit boards.

Alternatively, a larger sample population of circuit boards can be used. A larger population will increase the probability of obtaining the full range of possible variations in dielectric thickness and the full range of variation in stray capacitance.

Next, the exact same crystal and discrete load capacitors (C1 and C2) must be soldered onto each board, and the LAN reference frequency should be measured on each circuit board.

The circuit board, which has a LAN reference frequency closest to the center of the frequency distribution, should be used while performing the frequency measurements to select the appropriate value for C1 and C2.

A.5 Temperature Changes

Temperature changes can cause the crystal frequency to shift. Therefore, frequency measurements should be done in the final system chassis across the system's rated operating temperature range.

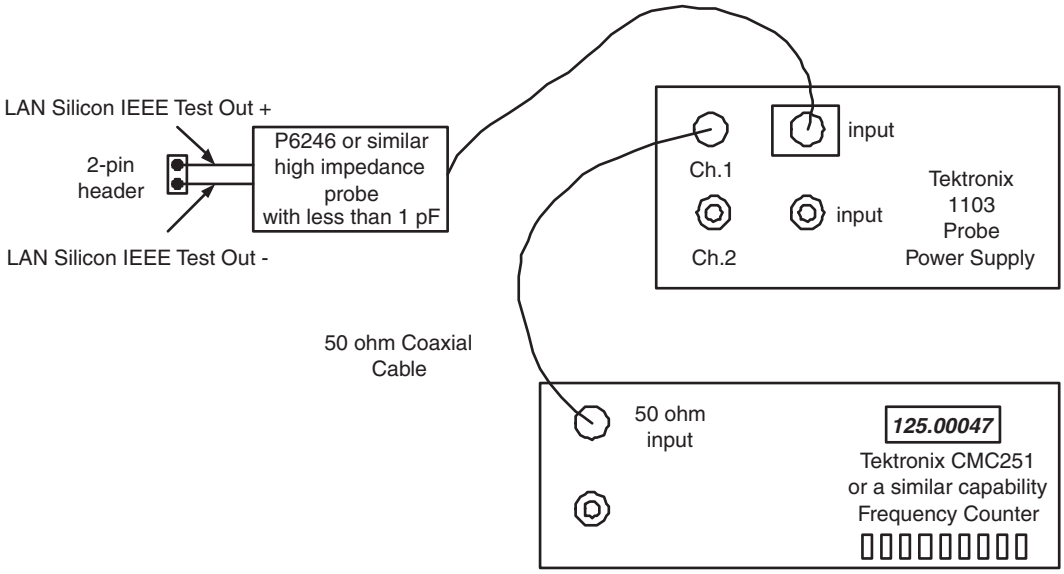
A.6 Indirect Probing Test Method

The indirect probing test method is applicable for most devices that support 100BASE-T. Since probe capacitance can load the reference crystal and affect the measured frequency, the preferred method is to use the indirect probing test method when possible.

Almost all Intel LAN silicon that support 1000BASE-T Ethernet can provide a buffered 125 MHz clock, which can be used for indirect probing of the transmitter reference clock. The buffered 125 MHz clock will be a 5X multiple of the crystal circuit's reference frequency (Figure 2).

Different LAN devices may require different register settings, to enable the buffered 125 MHz reference frequency. Please obtain the settings or instructions that are appropriate for the LAN controller you are using.

Figure 2. Indirect Probing Method



A.7 Indirect Frequency Measurement and Frequency Accuracy Calculation Steps

1. Make sure the system BIOS has the LAN controller enabled.
2. Connect the test equipment as shown in Figure 2.
3. Using the appropriate controls for your model of high resolution digital counter, make sure it can display ~125.0000 MHz with at least four decimal places frequency resolution.
4. Enable the 125 MHz buffered reference clock. An example can be found in Appendix B, “GigConf.exe Register Settings for 82541GI(EI) and 82547GI(EI) Devices”.
5. Determine the center reference frequency as accurately as possible. This can be done by taking 30 to 50 different readings using the frequency counter and then calculating the average results of the readings.
6. Calculate the accuracy of the measured and averaged center frequency with respect to an ideal 125.0000 MHz reference frequency.

$$FrequencyAccuracy(ppm) = \frac{(x - y)}{(y / 1000000)}$$

where x = Average measured frequency in Hertz and
y = Ideal reference frequency in Hertz

Example 1.

Given: The measured averaged center frequency is 124.99942 MHz (or 124,999,420 Hertz).

$$FrequencyAccuracy(ppm) = \frac{(124999420 - 125000000)}{(125000000 / 1000000)} = -4.64ppm$$

Example 2.

Given: The measured averaged center frequency is 125.00087 MHz (or 125,000,870 Hertz).

$$FrequencyAccuracy(ppm) = \frac{(125000870 - 125000000)}{(125000000 / 1000000)} = 6.96ppm$$

Note: The following items should be noted for an ideal reference crystal on a typical printed circuit board.

- If the transmitter reference frequency is more than 8 ppm below the target frequency, then the values for C1 and C2 are too big and they should be decreased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.
- If the transmitter reference frequency is more than 8 ppm above the target frequency, then the values for C1 and C2 are too small and they should be increased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.

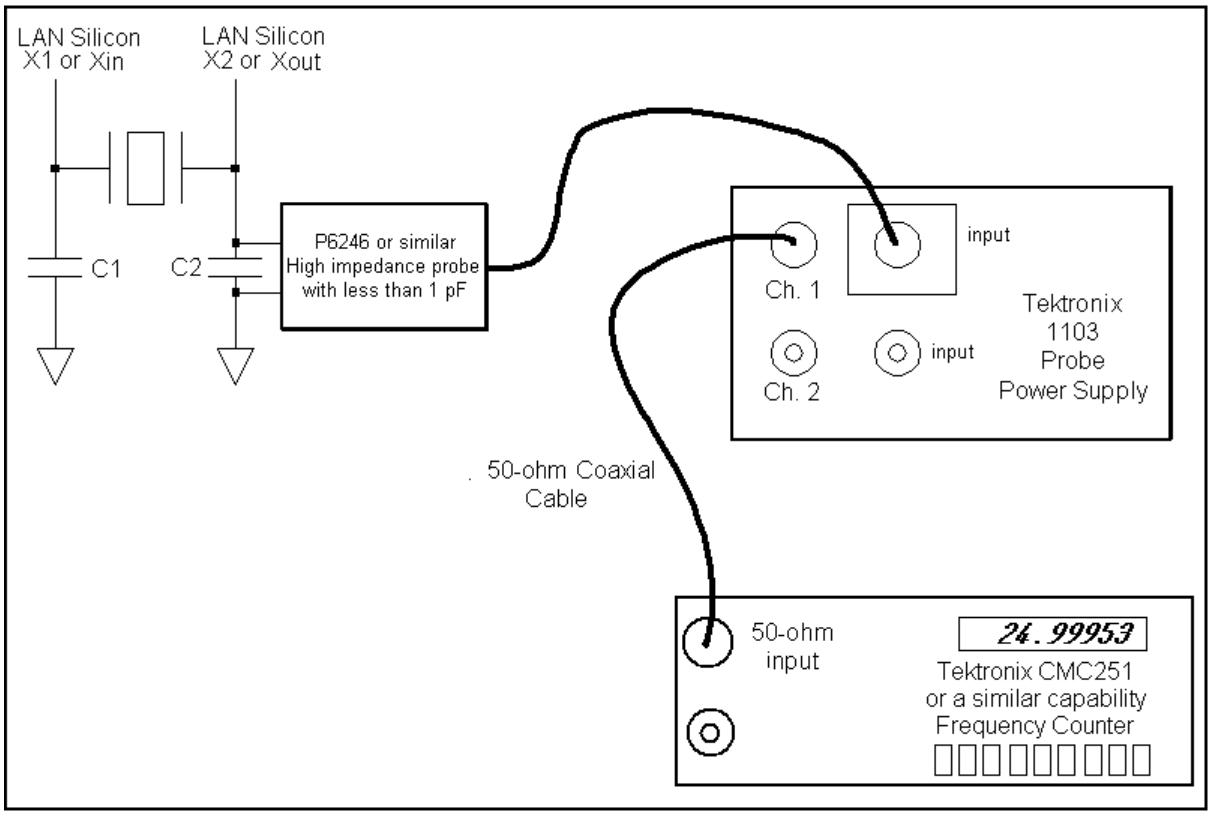
A.8 Direct Probing Test Method, Applicable for Most 10/100 Devices (Devices that do NOT support 1000Base-T)

Because probe capacitance can load the reference crystal affecting the measured frequency, it is preferable to use a probe with less than 1 pF capacitance.

Note: Direct probing is not recommended for the 82541GI(EI) and 82547GI(EI) LAN silicon.

The probe should be connected between the X2 (or Xout) pin of the LAN device and a nearby ground. Typically, it is possible to connect the probe pins across one of the discrete load capacitors (C2 in Figure 3).

Figure 3. Direct Probing Method



A.9 Direct Frequency Measurement and Frequency Accuracy Calculation Steps

1. Make sure the system BIOS has the LAN controller enabled.
2. Connect the test equipment as shown in Figure 3.
3. Using the appropriate controls for your model of high resolution digital counter, make sure it can display ~25.0000 MHz with at least four decimal places frequency resolution.
4. Ensure the LAN circuits are powered.
5. Determine the center reference frequency as accurately as possible. This can be done by taking 30 to 50 different readings using the frequency counter and then calculating the average results of the readings.
6. Calculate the accuracy of the measured and averaged center frequency with respect to an ideal 25.0000 MHz reference frequency.

$$FrequencyAccuracy(ppm) = \frac{(x-y)}{(y/1000000)}$$

where x = Average measured frequency in Hertz and
y = Ideal reference frequency in Hertz

Example 3.

Given: The measured averaged center frequency is 24.99963 MHz (or 24,999,630 Hertz).

$$FrequencyAccuracy(ppm) = \frac{(24999630-25000000)}{(25000000/1000000)} = -14.8ppm$$

Example 4.

Given: The measured averaged center frequency is 25.00027 MHz (or 25,000,270 Hertz).

$$FrequencyAccuracy(ppm) = \frac{(25000270-25000000)}{(25000000/1000000)} = 10.8ppm$$

Note: The following items should be noted for an ideal reference crystal on a typical printed circuit board.

- If the transmitter reference frequency is more than 8 ppm below the target frequency, then the values for C1 and C2 are too big and they should be decreased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.
- If the transmitter reference frequency is more than 8 ppm above the target frequency, then the values for C1 and C2 are too small and they should be increased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.

Appendix B: GigConf.exe Register Settings for 82541GI(EI) and 82547GI(EI) Devices

The following steps describe the indirect probing test method using GigConf.exe for 82541GI(EI) and 82547GI(EI) devices.

1. Boot to DOS using a DOS Boot Diskette.
2. Launch Gigconf from the diskette (gigconf.exe).
3. Select the Intel network connection to be measured.
    a. If multiple adapters are installed, use the arrow keys to navigate to highlight the selected adapter and press Enter.
4. Select Registers by pressing “R”.
5. Select PHY Registers by pressing “P”.
6. Use the arrow keys to navigate to the value listed next to address 0000.
7. Press Enter when the value is highlighted and then use Backspace to clear out the current value.
8. Type “0100” for the value and then press Enter.
9. Navigate to the value listed next to address 0012.
10. Press Enter to select the highlighted value and use Backspace to clear the current value.
11. Type “8000” for the value and then press Enter.
12. Navigate to the Set Address field on the right side of the screen (use the right arrow key)
13. Press Enter to select the highlighted value and then use Backspace to clear out the current value.
14. Type “4011” for the value and then press Enter.
    This changes the PHY register screen and updates it with new addresses and values.
15. Use the arrow keys to navigate to the value for address 4011.
16. Press Enter when the value is highlighted and then use Backspace to clear the current value.
17. Type “8000” for the value and then press Enter.
18. Use the right arrow key to navigate to the Set Address field on the right side of the screen.
19. Press Enter when the value is highlighted and use Backspace to clear the current value.
20. Enter “2F5B” (capital letters are not required) for the address and then press Enter.
21. Use the arrow keys to navigate to the value for address “2F5B”.
22. Press Enter when the value is highlighted and then use Backspace to clear the current value.
23. Type “0003” for the value and then press Enter.
24. Use the right arrow key to navigate to the Set Address field on the right side of the screen.
25. Press Enter when the value is highlighted and then use Backspace to clear the current value.
26. Enter “1F33” (capital letters are not required) for the value and then press Enter.
27. Use the arrow keys to navigate to the value for address “1F33”.

28. Press Enter once the value is highlighted and then use Backspace to clear the current value.
29. Type “0002” for the value and then press Enter.

The device should now be outputting the 125 MHz clock signal on IEEE output signals.

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