Ultra Low Voltage Intel® Celeron® M Processor at 600 MHz

Addendum to the Intel® Celeron® M Processor Datasheet

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Revision History

Rev. No.	Description	Rev. Date
1.0	Initial Release.	June 2004

1 Introduction

The ultra low voltage (ULV) Intel® Celeron® M Processors at 600 MHz has the following key features:

- Supports Intel Architecture with Dynamic Execution
- High performance, low power core
- On-die, primary 32-kbyte instruction cache and 32-kbyte write-back data cache
- On-die, 512-kbyte second level cache with Advanced Transfer Cache Architecture
- Advanced Branch Prediction and Data Prefetch Logic
- Streaming SIMD Extensions 2 (SSE2)
- 400-MHz, Source-Synchronous processor system bus
- Advanced Power Management features
- Micro-FCBGA packaging technology

The ULV Intel Celeron M processor at 600 MHz will be manufactured on Intel's advanced 0.13 micron process technology with copper interconnect. The processor maintains support for MMX™ technology and Internet Streaming SIMD instructions and full compatibility with IA-32 software. The high performance core features architectural innovations like Micro-op Fusion and Advanced Stack Management that reduce the number of micro-ops handled by the processor. This results in more efficient scheduling and better performance at lower power. The on-die 32-kbyte Level 1 instruction and data caches and the 512 kbyte Level 2 cache with Advanced Transfer Cache Architecture enable excellent performance.

The processor also features an advanced branch prediction architecture that significantly reduces the number of mispredicted branches. The processor's Data Prefetch Logic speculatively fetches data to the L2 cache before an L1 cache requests occurs, resulting in reduced bus cycle penalties and improved performance.

The Streaming SIMD Extensions 2 (SSE2) enable break-through levels of performance in multimedia applications including 3-D graphics, video decoding/encoding, and speech recognition. The new packed double-precision floating-point instructions enhance performance for applications that require greater range and precision, including scientific and engineering applications and advanced 3-D geometry techniques, such as ray tracing.

The processor's 400-MHz processor system bus utilizes a split-transaction, deferred reply protocol. The 400-MHz processor system bus uses Source-Synchronous Transfer (SST) address and data to improve performance by transferring data four times per bus clock (4X data transfer rate, as in AGP 4X). Along with the 4X data bus, the address bus can deliver addresses two times per bus clock and is referred to as a "double-clocked" or 2X address bus.

Working together, the 4X data bus and 2X address bus provide a data bus bandwidth of up to 3.2 Gbytes/second. The processor system bus uses Advanced Gunning Transceiver Logic (AGTL+) signal technology, a variant of GTL+ signalling technology with low power enhancements.

The processor features the Auto Halt, Stop Grant, Sleep and Deep Sleep low power states.

Note: The term AGTL+ has been used for Assisted Gunning Transceiver Logic signalling technology on other Intel products.

1.1 References

The primary reference document for this specification addendum is the *Intel® Celeron® M Processor Datasheet* found at http://developer.intel.com/design/mobile/datashts/300302.htm

Other references:

- Intel Celeron M Processor Specification Update
  http://developer.intel.com/design/mobile/specupdt/300303.htm

2 Specifications for the Ultra Low Voltage Intel® Celeron® M Processor at 600MHz

The *Intel® Celeron® M Processor Datasheet* is the basic reference for the electrical, mechanical and thermal specifications for the ULV Intel Celeron M processor at 600MHz.

There are some differences that are documented in this section. Table 1 documents the voltage and current specifications for this processor. Table 2 and Table 3 document the load line tolerances. Table 4 documents the power specifications. All specifications are at Tj (junction) = 100°C unless specified otherwise.

Table 1. Voltage and Current Specifications for the ULV Intel Celeron M Processor at 600MHz

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{CC}	V_{CC} for core logic		1.004		V	1, 2
$V_{CC,BOOT}$	Default boot voltage	1.14	1.2	1.26	V	2
V_{CCA}	PLL supply voltage	1.71	1.8	1.89	V	2
V_{CCP}	AGTL+ Termination Voltage	0.997	1.05	1.102	V	2
I_{CC}	Current for V_{CC} at core frequency 600 MHz & 1.004 V			7.2	A	3
I_{AH}, I_{SGNT}, I_{SLP}	Icc Auto Halt, stop Grant, Sleep at 1.004 V			3.4	A	4
I_{DSLP}	Icc Deep Sleep at 1.004 V			3.2	A	4
dI_{CC}/dt	V_{CC} power supply current slew rate			0.5	A/ns	5, 6
I_{CCA}	Icc for V_{CCA} supply			120	mA	
I_{CCP}	Icc for V_{CCP} supply			2.5	A	

NOTES:

1. The typical values shown are the VID encoded voltages. Static and Ripple tolerances (for minimum and maximum voltages) are defined in the load line tables i.e., Table 2 and Table 3.
2. The voltage specifications are assumed to be measured at a via on the motherboard's opposite side of the processor's socket (or BGA) ball with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-Mohm minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
3. Specified at VCC,STATIC (nominal) under maximum signal loading conditions.
4. Specified at the VID voltage.
5. Based on simulations and averaged over the duration of any change in current. Specified by design/ characterization at nominal VCC. Not 100% tested.
6. Measured at the bulk capacitors on the motherboard.

Table 2. Voltage Tolerances for VID = 1.004 V (Active State)

MODE	VID=1.004V, Offset=0%					
	I_{CC}, A	V_{CC}, V	STATIC		Ripple	
			Min	Max	Min	Max
ACTIVE	0	1.004	0.989	1.019	0.979	1.029
	0.3	1.003	0.988	1.018	0.978	1.028
	0.5	1.002	0.987	1.017	0.977	1.027
	0.8	1.002	0.986	1.017	0.976	1.027
	1.1	1.001	0.986	1.016	0.976	1.026
	1.4	1.000	0.985	1.015	0.975	1.025
	1.6	0.999	0.984	1.014	0.974	1.024
	1.9	0.998	0.983	1.013	0.973	1.023
	2.2	0.997	0.982	1.012	0.972	1.022
	2.5	0.997	0.982	1.012	0.972	1.022
	2.7	0.996	0.981	1.011	0.971	1.021
	3.0	0.995	0.980	1.010	0.970	1.020
	3.3	0.994	0.979	1.009	0.969	1.019
	3.6	0.993	0.978	1.008	0.968	1.018
	3.8	0.992	0.977	1.008	0.967	1.018
	4.1	0.992	0.977	1.007	0.967	1.017
	4.4	0.991	0.976	1.006	0.966	1.016
	4.7	0.990	0.975	1.005	0.965	1.015
	4.9	0.989	0.974	1.004	0.964	1.014
	5.2	0.988	0.973	1.003	0.963	1.013
	5.5	0.988	0.972	1.003	0.962	1.013
	5.8	0.987	0.972	1.002	0.962	1.012
	6.0	0.986	0.971	1.001	0.961	1.011
	6.3	0.985	0.970	1.000	0.960	1.010
	6.6	0.984	0.969	0.999	0.959	1.009
	6.9	0.983	0.968	0.999	0.958	1.009
	7.1	0.983	0.968	0.998	0.958	1.008
	7.4	0.982	0.967	0.997	0.957	1.007

Table 3. Voltage Tolerances for VID = 1.004 V (Deep Sleep State)

MODE	VID=1.004V, Offset=-1.2%					
	I_{CC}, A	V_{CC}, V	STATIC		Ripple	
			Min	Max	Min	Max
Deep Sleep	0.0	0.992	0.977	1.007	0.967	1.017
	0.2	0.991	0.976	1.006	0.966	1.016
	0.4	0.991	0.976	1.006	0.966	1.016
	0.6	0.990	0.975	1.005	0.965	1.015
	0.9	0.989	0.974	1.004	0.964	1.014
	1.1	0.989	0.974	1.004	0.964	1.014
	1.3	0.988	0.973	1.003	0.963	1.013
	1.5	0.987	0.972	1.003	0.962	1.013
	1.7	0.987	0.972	1.002	0.962	1.012
	1.9	0.986	0.971	1.001	0.961	1.011
	2.1	0.986	0.970	1.001	0.960	1.011
	2.3	0.985	0.970	1.000	0.960	1.010
	2.6	0.984	0.969	0.999	0.959	1.009
	2.8	0.984	0.969	0.999	0.959	1.009
	3.0	0.983	0.968	0.998	0.958	1.008
	3.2	0.982	0.967	0.997	0.957	1.007

Table 4. Power Specifications for the ULV Intel Celeron M Processor at 600MHz

Symbol	Core Frequency and Voltage	Thermal Design Power			Unit	Notes
TDP	600 MHz and 1.004 V		7		W	at 100°C, Note 1, 4
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Notes**
P_{AH} P_{SGNT}	Auto Halt Power, Stop Grant power at 1.004 V			2.0	W	at 50°C, Note 2
P_{SLP}	Sleep Power at 1.004 V			1.9	W	at 50°C, Note 2
P_{DSLP}	Deep Sleep Power at 1.004 V			1.5	W	at 35°C, Note 2
T_J	Junction Temperature	0		100	°C	Note 3

NOTES:

1. The Thermal Design Power (TDP) specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can dissipate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum T_J has been reached. Refer to Section 5.1.2 of the *Intel® Celeron® M Processor Datasheet* for more details.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.