Intel® IXDPG425 Gateway Reference Platform

User's Guide

November 2004

Document Number: 303146-002

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Revision History

Date	Revision	Description
November 2004	002	Added caution statement to Section 2.0, replaced Table 3, slightly modified Section 2.3, changed TRST_N “Connect to:” entry in Table 10, and added notes regarding RedHat* version to Section 3.0. Change bars indicate areas of change.
October 2004	001	Initial release.

1.0 Introduction

1.1 Purpose

This document provides an overview of the Intel® IXDPG425 Network Gateway Reference Platform, which is based on the Intel® IXP425 Network Processor. This document outlines procedures for demonstrating the typical functionality of a residential gateway.

The IXDPG425 network gateway reference platform comprises a set of building blocks and provides the functionality needed for a typical residential gateway. The platform features an IXP425 network processor, SDRAM memory, flash, a four-port Ethernet switch for LAN, an additional Ethernet port for WAN, four telephone line interfaces, a miniPCI interface to connect to a 802.11 WLAN, an ADSL mezzanine card interface, two USB 2.0 host ports, plus power-regulator devices.

The IXDPG425 is designed to be a turn-key solution so that original-equipment manufacturers can adopt the platform's design, select/deselect features, and quickly develop a desired solution. The platform also demonstrates the IXP425 network processor's scalability and processing power — delivered by an Intel XScale® Core and network processing engines (NPEs) — in supporting residential-gateway applications.

1.2 Intended Audience

This document is intended for residential-gateway architects and developers evaluating the performance, functions, or basic applications of the IXP425 network processor and IXDPG425.

This user's guide does not explore the entire architecture of the IXDPG425 nor the details on the various components that are used. Instead, it briefly discusses the platform's interfaces used to achieve desired functionality.

1.3 Related Information

Table 1. Related Documents

Document Title	Document Number/ URL[a]
Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Developer's Manual	252480
Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Hardware Design Guidelines	252817
Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Datasheet	252479

Table 1. Related Documents (Continued)

Intel® IXP400 Digital Signal Processing (DSP) Software Documentation	http://www.intel.com/design/network/products/npfamily/docs/ixp4xx.htm#
3-Volt Intel StrataFlash® Memory Datasheet	290667
Intel® PRO/100+ Adapter Technical Specifications	http://www.intel.com/network/connectivity/resources/doc_library/tech_specs/pro100_dsktop.htm

a. For Intel® IXP42X product line documentation, see http://www.intel.com/design/network/products/npfamily/docs/ixp4xx.htm#.

1.4 Acronyms and Terminology

ADSL	Asymmetric Digital Subscriber Line
AP	Access Point
ATM	Asynchronous Transfer Mode
CFI	Common Flash Interface
CPE	Customer-Premises Equipment
CS	Chip Select
DHCP	Dynamic Host Configuration Protocol
DNP	Do Not Populate
DSP	Digital Signal Processor
DTMF	Dual Tone Multi-Frequency
GPIO	General-Purpose Input/Output
HPI	Host-Port Interface
HSS	High-Speed Serial
IXP425 network processor	Intel® IXP425 Network Processor
JTAG	Joint Test Access Group
LAN	Local Area Network
LED	Light-Emitting Diode
MII	Media-Independent Interface
NPE	Network Processor Engine
PCA	Printed Circuit Assembly
PCI	Peripheral Component Interconnect
PCM	Pulse Code Modulation

PHY	Physical layer
ROM	Read-Only Memory
SDRAM	Synchronous Dynamic Random Access Memory
SLIC	Subscriber Line Interface Circuit
SPI	Serial Peripheral Interface
TCK	Test Clock
TDI	Test Data In
TDO	Test Data Out
TFTP	Trivial File Transfer Protocol
TMS	Test-Mode Strobe
TP	Test Point
UART	Universal Asynchronous Receiver Transceiver
USB	Universal Serial Bus
UTOPIA	Universal Test and Operations Physical Interface for ATM
WAN	Wide-Area Network
WLAN	Wireless LAN
WiFi	Wireless Fidelity
WEP	Wired Equivalent Privacy

1.5 Signal Naming Conventions

Table 2 shows the conventions used to identify and classify signal names:

Table 2. Signal Naming Conventions

Convention	Description
_N	(Placed after a signal name) The signal is active-low
I	Pin is input-only
O	Pin is output-only
I/O	Pin is bidirectional
Z	Tri-state
TTL	Transistor-Transistor Logic
OD	Open drain pin
U	Resistor is a pull-up resistor
D	Resistor is a pull-down resistor
h	(after numerals) Hexadecimal value (example: 2F8000h)

Table 2. Signal Naming Conventions

Convention	Description
b	(Behind numerals) Binary value (example: 010110b)
_DNP	(In a schematic) A component that should not be populated.
GND_DIGITAL	Ground plane for the base-card I/O card
TP	Test points.
#	The signal name preceding the "#" character is negated

2.0 Intel® IXDPG425 Network Gateway Reference Platform Overview

The IXDPG425 has all the components of a residential gateway, including the interface for LAN, WAN, and telephone. The 802.11 WLAN connectivity is implemented by an OEM-supplied miniPCI card.

The IXDPG425 consists of:

- Intel® IXP425 Network Processor
- SDRAM (32 Mbyte) — 48LC8M16A2 (x2)
- One flash memory (16 Mbyte) — E28F128J3x-150 (provision for second flash device)
- Five-port Ethernet switch with four-port LAN and a one-port WAN — the Realtek* RTL8305SB-VD
- UTOPIA ADSL mezzanine board interface
- Four-voice-port interface — Silicon Labs* 3201KS (x4); 3210KT (x4)

  Caution: The IXDPG425 cannot be directly or indirectly connected to any telecommunication network. Telephones to be connected must be within the same building.
- One miniPCI connector for 802.11 WLAN (plus available option of a second connector on the rear of the PCA)
- One serial port
- Two high-speed USB 2.0 host ports
- One USB 1.1 device port

Figure 1 provides a basic block diagram of the platform and its connections for external devices. Figure 2 presents a photograph showing the external-device connections.

Figure 1. Intel® IXDPG425 Network Gateway Reference Platform Block Diagram

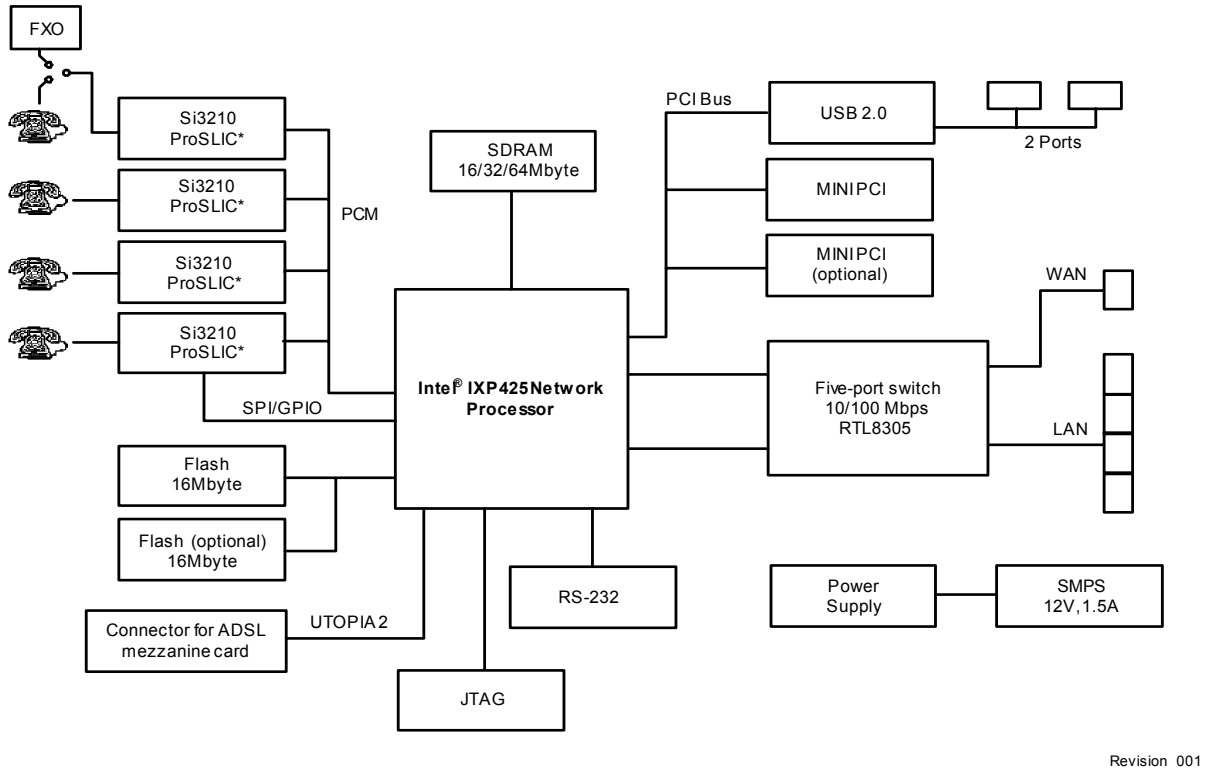
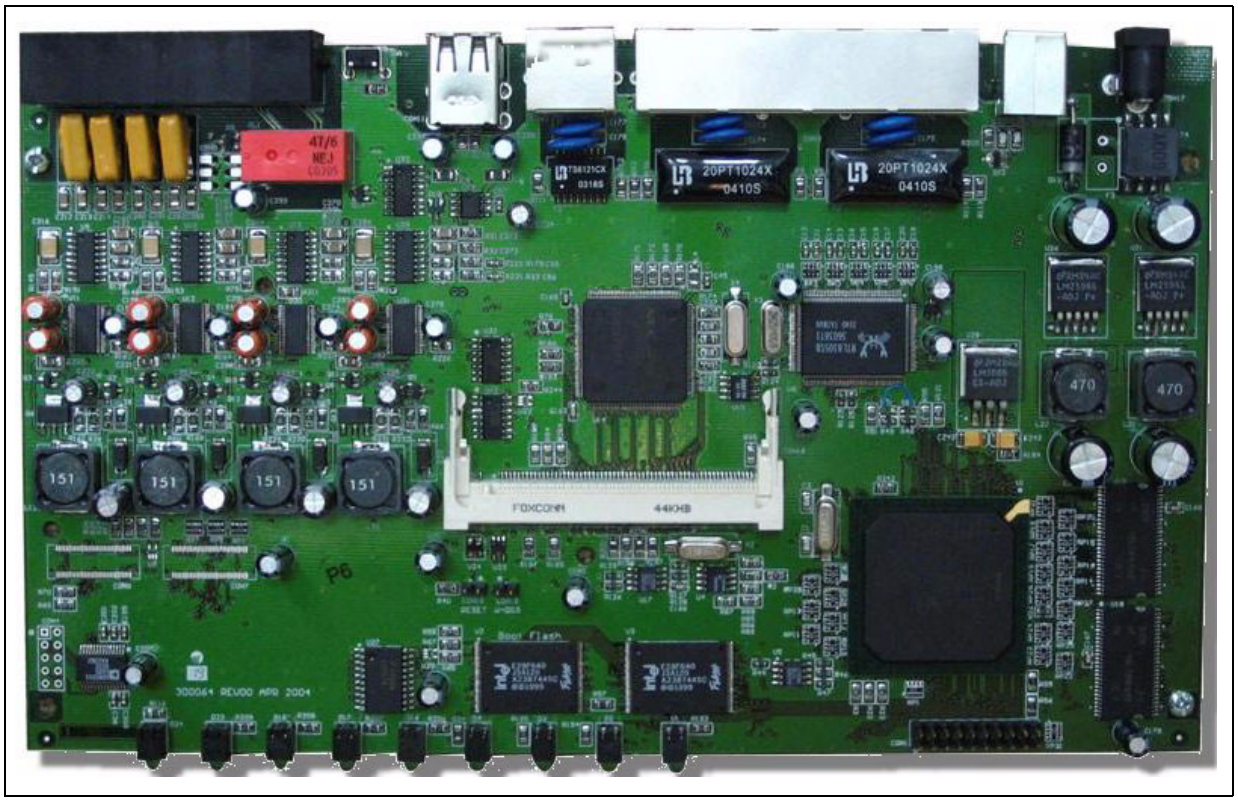


Figure 2. Intel® IXDPG425 Network Gateway Reference Platform Photograph



2.1 Intel® IXP425 Network Processor

The IXP425 network processor can operate at clock speeds of 266, 400, or 533 MHz. The IXDPG425 is the reference platform for the IXP425 network processor. An external 33.33-MHz crystal acts as the input clock signal for the IXP425 network processor.

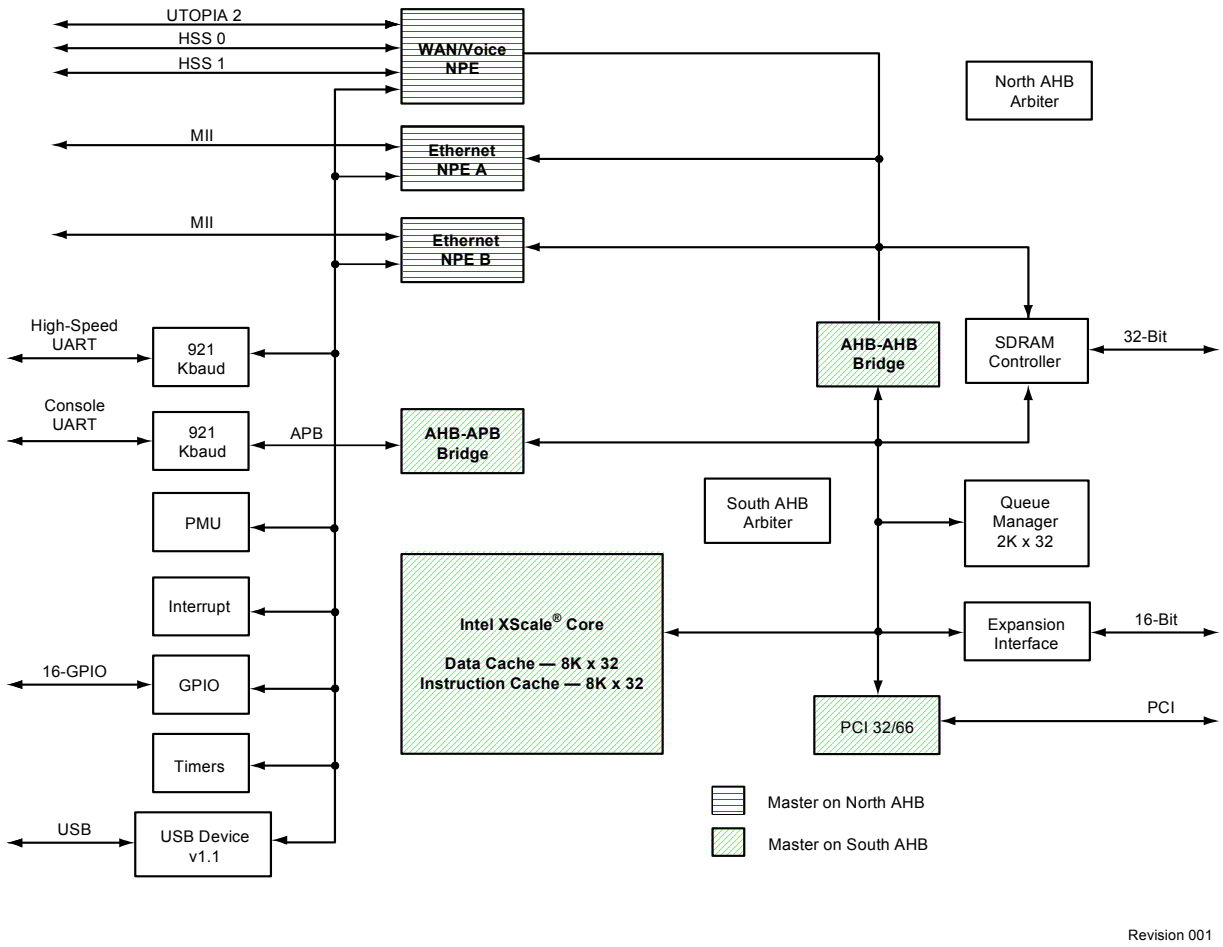
The IXP425 network processor's primary features include:

- Intel XScale® Core running the system clock rate of 133 MHz at ratios of x2, x3, and x4
- Three NPEs for Layer-2 packet/frame network processing
- Two 10/100-Mbps, full-duplex IEEE-802.3 MAC with MII interface
- Dedicated SDRAM with 32-bit memory interface operating at 133 MHz (equal to system-clock frequency)
  - — Supports up to two banks — each with two chips — of two- and three-cycle CAS latency
  - — 13-bit address — maximum: 256 Mbyte; minimum: 8 Mbyte.
- Expansion Bus
  - — 24-bit address
  - — 16-bit data
  - — Eight chip selects

  - Glueless interface to Intel flash and Motorola*- and Intel-mode peripherals
- DSP support for:
  - Texas Instruments* DSPs supporting HPI-8 bus cycles
  - Texas Instruments* DSPs supporting HPI-16 bus cycles
- UTOPIA-2 interface, 8-bit data path
- Two high-speed, serial TDM buses: HSS-0 and HSS-1
- Two UARTs, each supporting 921 Kbaud
- PCI 2.2 bus
  - 32-bit address/data bus
  - 33 and 66 MHz
  - Built-in arbiter supports up to four external bus masters
- 16 GPIOs
- USB 1.1 device controller supporting full-speed, USB v1.1 data rate

The high-level view of the IXP425 network processor is shown in Figure 3. The internal bus is partitioned into three segments and data transactions between the network processing elements SDRAM and CPU may be performed concurrently. The SDRAM controller can support fast SDRAMs with different memory sizes and bank organizations.

Figure 3. Intel® IXP425 Network Processor High-Level Block Diagram



2.2 Memory Map

The IXP425 network processor implements a single address map used for all internal memory and register space. The complete address space consists of 2^{32}-byte, addressable locations.

Table 3. Intel® IXP425 Network Processor Memory Map (Sheet 1 of 2)

Start Address	End Address	Size	Description
0000_0000	0FFF_FFFF	256 MB	Expansion Bus Data†
0000_0000	2FFF_FFFF	756 MB	SDRAM Data†
3000_0000	3FFF_FFFF	256 MB	(Reserved)
4000_0000	47FF_FFFF	128 MB	(Reserved)

Table 3. Intel® IXP425 Network Processor Memory Map (Sheet 2 of 2)

Start Address	End Address	Size	Description
4800_0000	4FFF_FFFF	128 MB	PCI Data
5000_0000	5FFF_FFFF	256 MB	Expansion Bus Data
6000_0000	63FF_FFFF	64 MB	Queue manager
6400_0000	BFFF_FFFF		(Reserved)
C000_0000	C3FF_FFFF	64 MB	PCI Controller Configuration and Status Registers
C400_0000	C7FF_FFFF	64 MB	Expansion Bus Configuration Registers
C800_0000	C800_0FFF	1 KB	High-Speed UART
C800_1000	C800_1FFF	1 KB	Console UART
C800_2000	C800_2FFF	1 KB	Internal Bus Performance Monitoring Unit
C800_3000	C800_3FFF	1 KB	Interrupt Controller
C800_4000	C800_4FFF	1 KB	GPIO Controller
C800_5000	C800_5FFF	1 KB	Timers
C800_6000	C800_6FFF	1 KB	WAN/Voice NPE = NPE-A (IXP400 software Definition)– Not User Programmable
C800_7000	C800_7FFF	1 KB	Ethernet NPE A = NPE-B (IXP400 software Definition) – Not User Programmable
C800_8000	C800_8FFF	1 KB	Ethernet NPE B = NPE-C (IXP400 software Definition) – Not User Programmable
C800_9000	C800_9FFF	1 KB	Ethernet MAC A
C800_A000	C800_AFFF	1 KB	Ethernet MAC B
C800_B000	C800_BFFF	1 KB	USB Controller
C800_C000	C800_FFFF		(Reserved)
C801_0000	CBFF_FFFF		(Reserved)
CC00_0000	CC00_00FF	256 Byte	SDRAM Configuration Registers
CC00_0100	FFFF_FFFF		(Reserved)

† The lowest 256 MB of address space is configurable based on the value of a configuration register located in the Expansion Bus Controller.

- When the configuration register is set to logic 1, the Expansion Bus occupies the lowest 256 MB of address space.
- When the configuration register is set to logic 0 the SDRAM occupies the lowest 256 MB of address.

  In both cases, the SDRAM occupies the 768 MB immediately following the lowest 256 MB and the Expansion Bus can be accessed starting at address 5000_0000.

  The largest SDRAM memory size supported by the Intel® IXP42X product line and IXC1100 control plane processors is 256 MB. The actual memory implemented in any given configuration will be aliased (repeated) to fill the 1 GB SDRAM address space. Due to aliasing, all of the SDRAM will be accessible even when the Expansion Bus occupies the lowest 256 MB of address space. On reset, the configuration register in the Expansion Bus will be set to logic 1. This setting is required because the dedicated boot memory is flash memory located on the Expansion Bus.

2.3 SDRAM Memory

The IXP425 network processor supports PC-133-compatible SDRAM only for both 16-bit-wide and 32-bit-wide devices. The banks are accessed 32 bits at a time. The IXDPG425 supports 32 Mbyte, using two chips each of 2M x 16 x 4 banks internal configuration.

The SDRAM controller is optimized for handling 8-word bursts from the SDRAM. The SDRAM controller throttles the data throughput by controlling the CKE pin of the SDRAM and the Wait signal of internal bus.

Byte-handling is performed — only for write operations to the SDRAM — by controlling the DQM pins of the SDRAM. All read operations are performed by reading the complete bus width of data.

The SDRAM controller has a policy to keep up to eight pages open simultaneously (four per SDRAM bank). If a request is received for an open page, the row access (RAS) address cycle is not performed. If the requested page is not currently open, the SDRAM controller first closes the currently open page in that bank, then opens the new page.

2.4 Expansion Bus

The expansion bus in the IXP425 network processor has 16-bit data and 24-bit address for each of its eight independent chip selects. This allows an addressing range of 512 byte to 16 Mbyte and connection of up to eight independent, external devices.

2.4.1 Devices on the Expansion Bus

Table 4 shows the chip selects of IXDPG425 devices that are connected to the expansion bus.

Table 4. Chip Selects For Devices Connected to Expansion Bus

Chip Select	Assignment
CS0	Flash 0 (Boot device)
CS1	Flash 1 (Optional Flash)
CS2	Front Panel LED Latch
CS3	Not used
CS4	ADSL CTRLE Interface
CS5	Not used
CS6	Not used
CS7	Not used

On the IXDPG425, GPIO 15 provides a programmable CLK output (CLK_GPIO15) to the expansion bus clock input (EXP_CLK) — at speeds of up to 33 MHz — through a clock driver. This same clock signal is used by the UTOPIA interface.

2.4.2 Configuration Straps

The expansion bus address lines (EXP_A [23:0]) are used for configuration strapping options during boot-up or whenever the reset is de-asserted. At the first cycle after the de-assertion of reset, the values on these lines are read (the expansion bus address outputs are switched to inputs) to determine the configuration of the IXDPG425 and its plug-in cards.

These values are stored in Configuration Register 0, bit [23:0]. All defined configuration strappings are shown in Table 5.

For more information about Configuration Register 0, see the *Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Developer's Manual*.

Table 5. Intel® IXDPG425 Network Gateway Reference Platform Configuration Strappings

Bit	Name	Description
23:21	Intel XScale® Core Clock Set[2:0]	Processor speed select 23, 22, 21 = Processor frequency core speed selected. The IXDPG425 is fitted with a 533-MHz IXP425. The core speed may be regulated by fitting pull-down resistors on Expansion address lines 23:21. 1 0 0 = 533 MHz 0 0 1 = 400 MHz 0 1 1 = 266 MHz The pull-down resistors will be included in the schematics, allowing test and debug at different speeds, though not assembled on the platform.
20:17	—	(Not currently used.)
16:5		(Reserved)
4	PCI_CLK	Clock speed of the PCI Interface 0 = 33 MHz (IXDPG425 setting) 1 = 66 MHz
3	—	(Reserved)
2	PCI_ARB	Enables the PCI Arbiter 0 = PCI arbiter disabled 1 = PCI arbiter enabled (IXDPG425 setting)
1	PCI_HOST	Configures the IXP425 network processor as PCI Bus Host 0 = IXP425 network processor as non-host 1 = IXP425 network processor as host (IXDPG425 setting)
0	8/16 flash	Specifies the data bus width of the flash memory device 0 = 16-bit data bus (IXDPG425 setting) 1 = 8-bit data bus

2.5 Flash / Boot ROM

The boot ROM for the IXDPG425 is the Intel StrataFlash® E28F128J3x-150 16-Mbyte memory connected through the expansion bus. The flash is organized as 16 Mbytes (or 8 Mwords by 16 bits) or 128 128-Kbyte (131,072 bytes) erase blocks. The E28F128J3x supports the common flash interface (CFI).

For more information about the E28F128J3x Intel StrataFlash Memory, see the *3-Volt Intel StrataFlash® Memory Datasheet*.

There are two flash devices on the IXDPG425: Flash 0, which is the Boot flash; and Flash 1, which is not currently used. The IXDPG425 may only boot from the Flash 0 device. The designer needs to be sure to program the CS1 output before any attempt is made to access the Flash 1 address space.

The size of the data transfer (8- or 16-bit) is set on the board using the expansion-bus address 0 strapping jumper. The EXP_A0 strap is set to 0 at the de-assertion of reset to select 16-bit data bus. The FLASH_STS pin on the flash is unused on the IXP425 network processor.

2.6 ADSL WAN Port

The main features of the ADSL interface include:

- Control Interface (CTRLE) — Expansion bus
- Data Interface — UTOPIA Level 2
- Chip Select — EXP_CS4_N
- Ready Signal — On IO_WAIT_N
- Interrupt — GPIO 16 Mbytes 12, active low
- Clock — External, 33-MHz, UTP_IP_CLK and UTP_OP_CLK

The ADSL WAN interface is provided by a mezzanine card plugged into the ADSL board socket. The ADSL chipset is interfaced with the host, through the expansion bus, for control and initialization purposes. The chip set needs nine address lines and its data bus is eight bits wide.

The ADSL CTRLE interface is enabled by the expansion-bus Chip-Select 4 output. The ADSL interrupt is recognized by the IXP425 network processor on GPIO 12. The user data interface is provided through the UTOPIA Level 2 interface. The ADSL mezzanine card requires 3.3-V and 12-V supplies. Table 6 shows the mezzanine card pin numbers and functions.

Table 6. CON 7 ADSL Mezzanine Board Connector

Pin	Function
1	CTRLE-A6
2	CTRLE-A8
3	Ground
4	Ground
5	CTRLE-A3
6	CTRLE-A4
7	Ground
8	Ground
9	CTRLE-A1
10	CTRLE -ADSL_SEL#
11	Ground
12	Ground
13	CTRLE-D4
14	CTRLE-A7
15	Ground
16	Ground
17	CTRLE-RDY#
18	CTRLE-A2
19	Ground
20	Ground
21	CTRLE-A0
22	CTRLE-D6
23	Ground
24	Ground
25	CTRLE-D5
26	CTRLE-D2
27	Ground
28	Ground
29	CTRLE-D3
30	CTRLE-D1
31	Ground
32	Ground
33	CTRLE-D0
34	CTRLE-WR#
35	Ground
36	Ground
37	CTRLE-RD#
38	CTRLE-ADSL-IRQ#
39	Ground
40	Ground
41	MODE
42	CTRLE-A5
43	Ground
44	Ground
45	CTRLE-D7
46	UTP_RX_D6
47	Ground
48	Ground
49	ADSL_CLK
50	UTP_RX_D0
51	Ground
52	Ground
53	UTP_TX_D2
54	UTP_TX_CLAV
55	Ground
56	Ground
57	UTP_TX_D1
58	UTP_TX_D4
59	Ground
60	Ground
61	UTP_TX_A1
62	UTP_TX_A0
63	Ground
64	Ground
65	UTP_TX_D3
66	UTP_RX_D2
67	Ground
68	Ground
69	UTP_RX_D5
70	UTP_RX_D3
71	Ground
72	Ground
73	UTP_TX_D6
74	ADSL_CLK
75	Ground

Pin	Function
76	Ground
77	UTP_RX_SOC
78	UTP_RX_D0
79	Ground
80	Ground
81	UTP_RX_D7
82	UTP_RX_D7
83	Ground
84	Ground
85	UTP_TX_EN
86	UTP_RX_D4
87	Ground
88	Ground

Pin	Function
89	UTP_RX_D1
90	UTP_TX_SOC
91	Ground
92	Ground
93	UTP_RX_A1
94	UTP_TX_D5
95	Ground
96	Ground
97	UTP_RX_CLAV
98	UTP_RX_EN
99	UTP_RX_A0
100	+12V

2.7 PCI Interface

The IXDPG425 is equipped with a PCI interface (only 33-MHz PCI is supported). The PCI peripherals include a USB 2.0 controller, and a miniPCI socket (CON 16). An optional second miniPCI socket (CON 15) can be mounted on the rear of the IXDPG425 printed circuit assembly.

Reset of the PCI bus is under control of the power-on reset controller and GPIO8. Table 7 lists the ID selects assignments used during PCI reset and initialization.

Table 7. PCI Reset ID Select and Interrupt Assignments

PCI Peripheral	IDSEL	Interrupt	GPIO
MiniPCI Slot	AD19	INTB	GPIO7
Optional MiniPCI Slot	AD20	INTB	GPIO7
USB 2.0 Controller	AD18	INTA	GPIO6

2.8 Ethernet Interfaces — Four-Port LAN, One-Port WAN

Interface:MDC/MDIO

Interface:NPE Ethernet 0 to 4x switch
Clock: External, 25 MHz

Interface:NPE Ethernet 1 to 1x Ethernet WAN
Clock:External, 25 MHz

The IXP425 network processor has two Ethernet 10/100BaseT interfaces, implemented with Ethernet coprocessors built into the NPEs.

The coprocessors provide support for an MII interface to the external PHY. They support both full-duplex and half-duplex mode of operation and also contain two 256-byte FIFOs, one for transmit data, and the other for receive data.

The IXP425 network processor includes a single management data interface — Management Data Input Output (MDIO) — and Management Data Clock (MDC) to program the Ethernet PHYs.

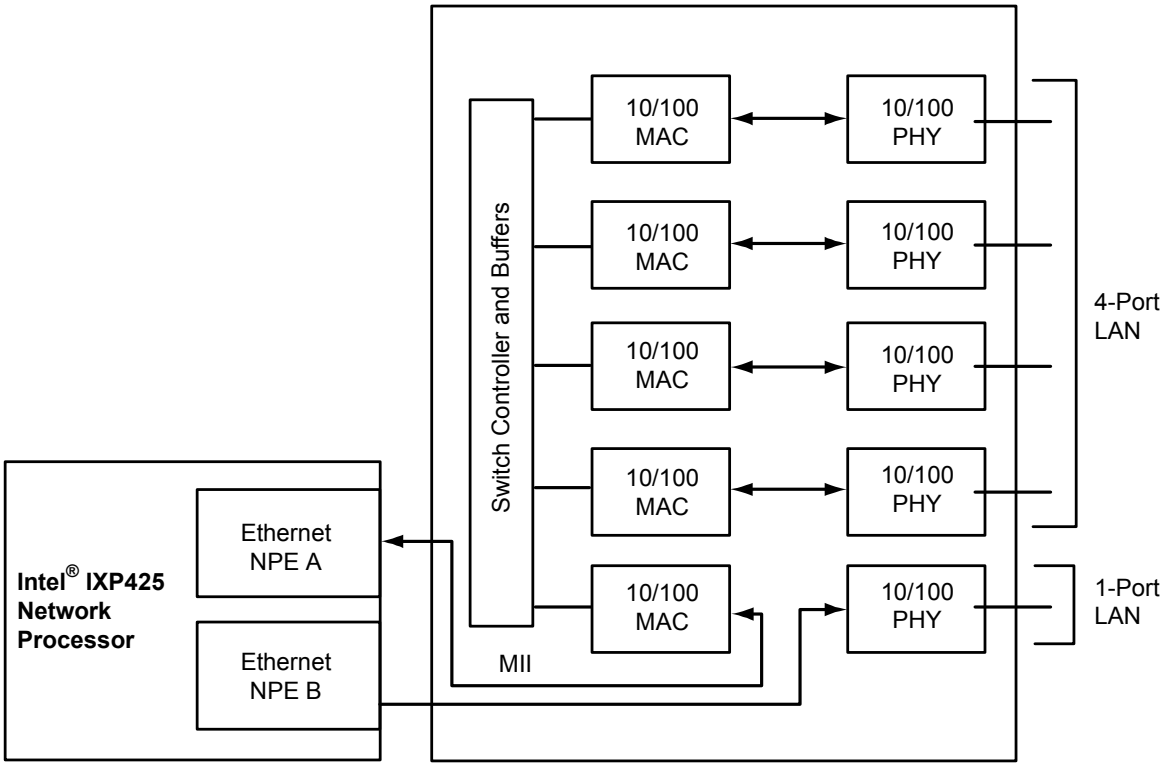
On the platform, the Realtek RTL8305-SBVD component is used. This component contains five physical-layer transceivers and five MAC units with an integrated Layer-2 switch.

On the platform, the integrated five-port switch provides the interface for up to four devices on the LAN. The LAN portion of the switch is connected to the IXP425 Ethernet Controller 0, via the MII-0 interface. The fifth port is directly connected to the IXP425 Ethernet Controller 1 via the MII-1 interface. Such configuration allows implementation of Ethernet bridge and router modes in software, and — at the same time — filters out the local traffic on the LAN to reduce the load on the Intel XScale core, as shown in Figure 4.

Each of the RJ45 connectors for each of the Ethernet ports have integrated LEDs that illuminate as follows:

Green: Link/activity
Amber: 10/100 Mbps; illuminates when connected to a 100-Mbps network

Figure 4. Software Implementation of Ethernet Bridging and Router Modes



Revision 001

2.9 Voice Ports

Table 8. Voice Ports

Attributes	Port	Port
Interface	SPI to Si3210-0 to Si3210-3	HSS0 – PCM to Si3210–0 to Si3210-3
Chip Select#	GPIO5 active low	
Clock	GPIO2 (HSS0_TXCLK)	
Ready Signal		
Interrupt#	GPIO11	
Data IN	SDI GPIO3 to Si3210-0, then Si3210-1, 2, 3. (Data to CODEC)	
Data OUT	SDO GPIO4 (Data from CODEC)	
Programmed Reset#	GPIO13 active low	

The line interface is implemented using four of the Silicon Laboratories* ProSLIC* Si3210 components that integrate a DC-DC converter for ring voltages, the A- and µ-law linear companding, DTMF decoders, and dual-tone generators for a single telephone line. The Si3210 components are connected to the IXP425 network processor using the SPI and PCM buses. The voice data is sent to and from the codec on the PCM time-slotted, synchronous, serial interface.

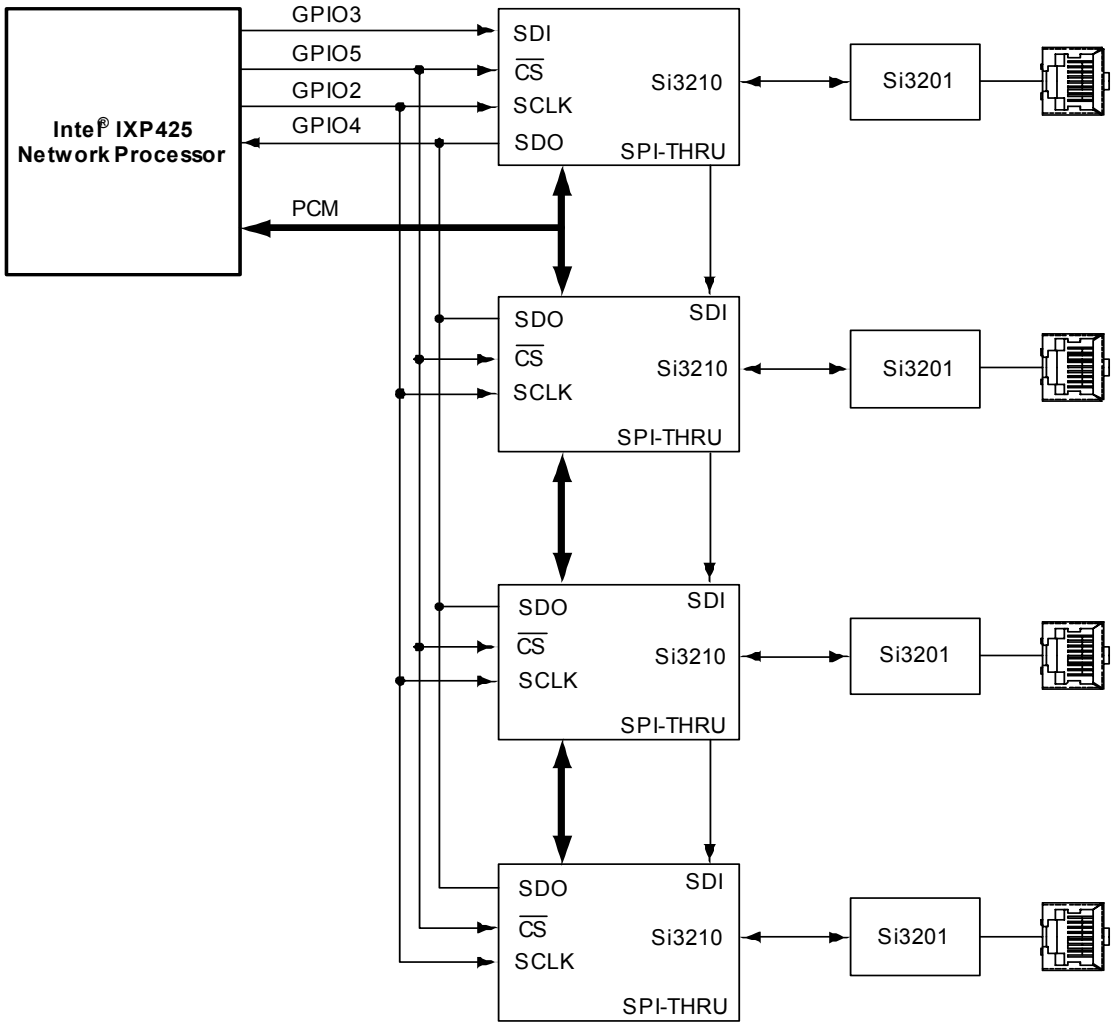
The SLIC is programmed through the SPI interface that can work in 8-bit serial mode. The SPI is connected to the four SLICs in the daisy-chain mode, as shown in Figure 5.

The PCM common bus, with the time-slotted protocol, allows support of local line-looping and inserts data-processing elements into the data flow to support a variety of compression algorithms.

A fifth telephone connector is provided to allow a conventional telephone exchange line to be plugged in. In the event of power failure or software failure, the telephone plugged into voice port 4, will automatically fail-over to the exchange line, allowing continued operation of this telephone service.

The failover relay is organized such that the Normally-Closed contacts will connect the exchange line to port 4 when there is no power to the IXDPG425. Additionally, a retriggerable monostable is used to control the relay, such that if the monostable does not receive retrigger signals before its time-out period (approximately 600 ms), it will cause the relay to revert to its un-powered state and port 4 will fail over to the exchange line. The re-trigger signal used is the same signal used for the watchdog retrigger (GPIO10). This will ensure that a telephone call is still possible even if there has been a software failure on the IXDPG425.

Figure 5. Four Voice Ports (Two Shown)



The PCM works under control of NPE firmware, which is loaded at startup to configure the IXDPG425 HSS ports.

The DTMF signaling decoding is implemented in the SLICs, and the call progress and dialing is supported by the IXP425 network processor and the voice driver.

During initialization, the SLICs require a series of ordered steps for reset:

1. After the power-on reset is completed, I/O-reset pin GPIO13 needs to be kept active.
2. The HSS port must be initialized to provide a 2- or 1.5-MHz clock and an 8-KHz frame signal.
3. The PCM clock and frame signals must be present and stable prior to de-asserting the I/O-reset signal.

4. At this point, the I/O-reset pin GPIO13 can be de-asserted (high) along with the SPI clock signal, set to “high.” Before this point (GPIO13 going high), no other I/O can be initialized.
5. In platform configurations where voice features are not required, the voice port should be disabled by keeping the PCM_CLK (clock) and PCM_FRAME (frame) signals and the SPI_SCK (clock) signals “low” and the SPI_CS0_N signal “high.”

2.10 USB Ports

The USB 1.1 interface utilizes the IXP425 network processor on-chip USB controller, and can work only as the USB peripheral at a 12-Mbps data rate.

A Type-B, USB ‘device’ receptacle is provided at the board edge. A 1.5-K, pull-up resistor is applied on the D+ USB pin to indicate that the IXP425 network processor is a full-speed USB device.

The USB board design meets USB-specification requirements.

The USB 2.0 interface is built around the NEC* µPD720101 PCI USB 2.0 host adaptor chip. Two USB 2.0 host interfaces are implemented. Automatic voltage supply and over-current protection is included.

USB Version	USB Connector Number
USB 1.1 Slave	CON 20
USB 2.0 Host (2 Ports)	CON 11

2.11 Console Serial Port

The IXP425 network processor provides two dedicated, asynchronous, serial, I/O ports (UART0 and UART1). These UARTs are 16550-compliant with flow control and enhanced with larger 64-byte transmit and receive buffers. Only UART0 is used on the IXDPG425.

The console serial interface is connected to (UART0) Port 0. Port 0 is routed to the 10-pin header connectors (CON 4) with RTS and CTS flow control. Additional signaling lines (DTR and DCD) are provided by GPIO port pins 0 and 1, respectively. Port 0 is wired according to the RS-232 specification for data terminal equipment. A cross-over serial cable will be used to connect to a host PC.

A simple 10-pin header-to-DB9 converter assembly can be created with a 10-pin socket and a 9-pin DB9 socket and a short section of 10-way ribbon cable.

Table 9. Serial Port, CON 4, 10-Pin, Dual-Row Header (Sheet 1 of 2)

Pin Number	Signal Name
1	DCD# (GPIO 1)
2	N/C
3	RXD
4	RTS#
5	TXD

Table 9. Serial Port, CON 4, 10-Pin, Dual-Row Header (Sheet 2 of 2)

Pin Number	Signal Name
6	CTS#
7	DTR# (GPIO 0)
8	N/C
9	GND
10	N/C

2.12 JTAG Emulator Interface

During debug, the IXP425 network processor can be controlled through a JTAG interface to the Intel XScale core. The Macraigor* Raven* and Wind River Systems* visionPROBE* / visionICE* systems plug into the JTAG interface through a 20-pin connector (CON 1), defined in Table 10.

Table 10. JTAG Interface Connector Signals (Sheet 1 of 2)

Pin Number	Signal Name	Connect to:
1	VTREF	3 V3
2	VSUPPLY	+3V3
3	TRST_N	10KΩ pull-down – The JTG_TRST_N signal must be asserted (driven low) during power-up, otherwise the TAP controller may not be initialized properly, and the processor may be locked. When the JTAG interface is not being used, the signal must be pulled low using a 10-K. resistor.
4	GND	GND
5	TDI	10KΩ pull-up
6	GND	GND
7	TMS	10KΩ pull-up
8	GND	GND
9	TCK	10KΩ pull-up
10	GND	GND
11	RTCK	GND
12	GND	GND
13	TDO	10KΩ pull-up
14	GND	GND

Table 10. JTAG Interface Connector Signals (Sheet 2 of 2)

Pin Number	Signal Name	Connect to:
15	SRST_N	Reset circuitry (/BDMR)
16	GND	GND
17	DBGRQ	
18	GND	GND
19	DGBACK	
20	GND	GND

2.13 Front-Panel Indicator LEDs

The IXDPG425 has LEDs (light-emitting diodes) indicating the activities shown in Table 11. The LEDs are controlled by an 8-bit, memory-mapped latch. Writing a 0 to a specific LED latch bit will cause the LED to illuminate. The base address for the LED latch is set by CS3#. The latch is write-only and it is not possible to read back the status of the latch.

Table 11. Intel® IXDPG425 Network Gateway Reference Platform LEDs

LED Latch (CS3#)	LED	Color	Description
	D24	Green	Power to the system is on.
Bit 0	D23	Green	LED1
Bit 1	D18	Green	LED2
Bit 2	D17	Green	LED3
Bit 3	D16	Green	LED4
Bit 4	D4	Green	LED5
Bit 5	D3	Green	LED6
Bit 6	D2	Green	LED7
Bit 7	D1	Green	LED8

2.14 Platform-Reset Circuitry

The board generates a power-on reset when the required voltages reach valid levels. The power-on reset signal resets all the circuitry. A reset link (CON8) provided on the IXDPG425 also resets the entire board. Shorting the two pins of CON 8 together will cause a Reset.

The PCI and 10/100 Ethernet switch have a separate reset control. PCI bus peripherals and the switch will remain in a reset state until GPIO 8 is set as an output and driven high. It is possible to manually reset these resources by toggling the GPIO 8 line.

The reset for the SLIC devices is under control of GPIO 13. GPIO13 must be set up as an output and driven high for normal operation. Toggle GPIO 13 to reset the SLICs.

The watchdog reset function is enabled by fitting a shorting link to CON19. If the watchdog function is enabled, the entire system will be reset unless a watchdog retrigger signal is issued to the watchdog controller within its time-out period (minimum time-out period for TPS3823 is 0.9 seconds). GPIO 10 must be toggled at slightly more than 1 Hz to provide the retrigger signal. If the link is not fitted to CON 19, the watchdog reset function is disabled.

2.14.1 Erase Button

The rear-panel push button switch (SW1) can be used as a software reset or “configuration erase” button. It is connected to GPIO9. The input signal from the push button is normally pulled high and pressing the push button will cause the signal to go low. The push button signal is not de-bounced in hardware.

2.15 General-Purpose I/O

The IXP425 network processor GPIO pins are assigned as shown in Table 12

Table 12. GPIO Pin Assignments

GPIO	Direction	Function
0	Out	Serial Port DTR signal
1	In	Serial Port DCD signal
2	Out	SPI Clock
3	Out	SPI Data In (Data to CODEC)
4	In	SPI Data out (Data from CODEC)
5	Out	SPI Chip Select#
6	In	PCI INT A#
7	In	PCI INT B#
8	Out	PCI, 10/100 Switch-controlled reset
9	In	Erase push button
10	Out	Watch re-trigger signal
11	In	SLIC Interrupt#
12	In	ADSL Interrupt#
13	Out	SLIC Reset#
14	Out	33-MHz PCI clock
15	Out	33-MHz Expansion bus clock

2.16 Power Supplies, Regulators

The input power to the platform is through a brick power supply at +12 V DC, 1 A nominal. There are three power regulators on the platform rated at:

- 5.0 V at 1.5 A
- 3.3 V at 1.5 A
- 1.3 V at 1.0 A

2.17 Intel® IXDPG425 Network Gateway Reference Platform Hardware Design Kit

A complete IXDPG425 hardware design kit, including board schematics, layout, Gerber files, and a bill of materials, is available upon request. Contact your local Intel representative for more information.

The IXDPG425's printed circuit board (PCB) is 135 mm by 230 mm.

3.0 Installation and Configuration Overview

The Intel® IXDPG425 Network Gateway Reference Platform is pre-installed with the RedBoot boot loader (version 1.92 or higher). The following sections of this document describe the configuration, setup, and use of the IXDPG425 and its various peripheral interfaces.

3.1 Installing and Configuring the Hardware

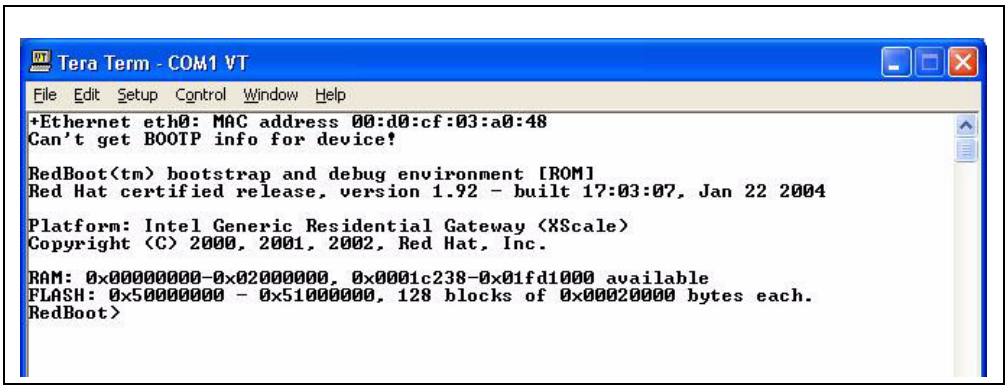
The primary and most basic communications with the IXDPG425 are through its serial port console. The basic setup requires the use of a terminal emulator on a host PC to interact with the IXDPG425.

1. Using the supplied serial cable attachment, connect the DB9 serial port connector of the IXDPG425 to the serial port of the host PC.
2. To communicate with the platform, open a communication session for the host-PC serial port connected to the IXDPG425, by doing one of the following:
   a. In the Windows operating system, begin a HyperTerminal session.
   b. In the Linux operating system, begin a minicom session.
3. Configure the terminal as follows:

Parameter	Value
Bits per second	115,200
Data bits	8
Parity	None
Stop bits	1
Flow control	None

3.2 Verifying RedBoot* Operation

On applying power to the IXDPG425, the following RedBoot boot banner should appear:



Note: The RedHat boot banner above shows version 1.92, although newer versions may be observed.

By default, RedBoot can be somewhat slow to boot, taking 30 seconds or more from power-on until the initial boot banner is displayed. RedBoot (by default) tries to acquire an address for its first Ethernet port using the DHCP protocol, and this causes the initial long boot delay.

3.3 Download Software

After verifying RedBoot operation, the platform is now ready for third-party application and OS downloads. Please refer to the following IXDPG425 Web page for information on available software solutions:

http://developer.intel.com/design/network/products/npfamily/ixdpg425.htm

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