



Performance of the Intel® IXP23XX Product Line of Network Processors for Access and Edge Network Applications

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Introduction

Manufacturers of access and edge equipment have long sought the ideal balance of performance and programming flexibility in a processing platform. The fact is, applications such as ATM-based Radio Access Networks, DSL Access Multiplexers (DSLAMs), Wireless Local Area Network (WLAN) access points, WAN multi-service switches, and others, must support a range of protocols and line rates to meet application requirements. Standards-based interfaces and reusable code can help ensure reliable performance as well as accelerate time-to-market and leverage software assets across multiple solutions. And for equipment manufacturers to maximize profitability they must choose the right network processor—one that is neither over-powered nor under-powered, yet offers plenty of headroom in which to innovate.

Intel offers an ideal solution with the Intel® IXP23XX product line of network processors, designed to enable a broad range of access and edge applications. Built on the same hardware and software architecture as the entire Intel® IXP2XXX product line, the IXP23XX network processors support deep packet inspection, traffic management, and forwarding at up to 2 Gbps line rates in a single chip, while providing the headroom developers need to deliver value-added network services.

Product line overview

The IXP23XX product line includes the Intel® IXP2325 network processor, which supports up to 2.5 giga-operations per second with two 32-bit independent multi-threaded microengines, and the Intel® IXP2350 network processor, which supports up to 4.9 giga-operations per second with four 32-bit independent multi-threaded microengines. Variants of

each network processor are available with Intel XScale® core operating frequencies ranging from 600 MHz to 1200 MHz, and fast path microengine operating frequencies ranging from 300 MHz to 900 MHz. Both network processors are fully programmable, yet have the processing power to run applications that previously required expensive, high-speed ASICs and external control plane processors.

As with all network processors in the entire Intel IXP2XXX product line, the IXP23XX network processors execute data plane tasks in parallel across individual microengines. The Intel® Internet Exchange Architecture (Intel® IXA) Software Framework complements the IXP2XXX modular hardware architecture by providing tested software building blocks, called microblocks, that developers can use to quickly assemble functional sequences, or pipelines, that perform specific network functions. These microblocks are highly reusable across applications; for example, an IP forwarding microblock could be used in a DSLAM application with an ATM media interface, as well as in a WAN multi-service switch.

In this white paper, Intel presents a performance assessment of the Intel IXP2350 network processor for a variety of common access and edge applications. In the application examples discussed, packets are processed in microblocks and executed across the microengines within the IXP2350 network processor, processing a comprehensive set of functions for a variety of data rates and communications protocols. As the performance assessment will show, the IXP2350 network processor offers robust performance with substantial headroom even under the most demanding conditions.

Performance metrics and IP forwarding example

When examining the performance capabilities of a network processor, it is important to first consider the performance metrics used. Two of the primary performance metrics used in the communications and networking industry are packet rate and data rate (see Table 1).

Data rate is the total number of Megabits-per-second (Mbps) that a networking element can handle. Packet rate is the number of million-packets-per-sec (Mpps) that the networking element can handle. The relation between the data rate and packet rate is simple:	
Packet rate (Mpps) =	$\frac{\text{Data rate (Mbps)}}{8 \cdot \text{Packet size (bytes)}}$

Table 1: Packet Rates vs. Data Rates

In network processors, the unit of work is a packet and, therefore, packet size is a critical parameter in characterizing performance. For example, smaller packets will require a greater number of packets per second to be processed at a given data rate. Since a certain amount of overhead is associated with each packet (e.g., table lookups, header updates, enqueues/dequeues), a greater number of smaller packets being processed per second will mean more work for the network processor and, consequently, less headroom available for value-added features. Conversely, with a fewer number of larger packets at the same data rate, the network processor can complete the same task with less work, thereby retaining greater headroom to support value-added features.

A simple application such as IP forwarding for Ethernet packets illustrates this point. An IP forwarding application can be implemented in three stages: packet receive, IP forwarding based on longest prefix match and packet transmit. Table 2 presents estimated performance and packet processing headroom for the Intel® IXP2350 network processor in this application.

Communications protocols, such as Gigabit Ethernet and OC-12, each support different minimum-sized packets

and carry different levels of overhead. Therefore, for any given data rate, performance—measured in ‘million packets per second’—will ultimately be a factor of packet size and overhead. With maximum data rates of 3.6 Gbps in the IPv4 forwarding example in Table 2, it is evident that the percentage of headroom in the IXP2350 network processor increases as the packet size grows.

Performance assessment of the Intel® IXP2350 network processor

In assessing the performance of the IXP2350 network processor, Intel chose to use minimum packet sizes in all application examples. By taking this approach, the IXP2350 network processor is subjected to the most demanding conditions likely to be encountered in the real world. Even in these “worst case” scenarios, the IXP2350 network processor demonstrates robust performance with ample headroom in which equipment vendors can add value.

To determine performance capabilities for the IXP2350 network processor, Intel calculated the headroom available with all four microengines processing minimum-sized packets with a robust set of application functions at a given data rate. These calculations are based on data from an Intel IXP23XX cycle and data accurate simulator and on previously measured data for the Intel® IXP2400 network processor extrapolated to match the specifications of the IXP2350 network processor.

Ethernet Packet Size	Intel® IXP2350 Network Processor
	<ul style="list-style-type: none"> • Intel XScale® core – 900 MHz • Microengines (ME) – 900 MHz
64 B	25% ME headroom (5.35 Mpps**)
128 B	58% ME headroom (3.04 Mpps**)
512 B	75% ME headroom (0.85 Mpps**)
1518 B	78% ME headroom (0.30 Mpps**)

Table 2: IPv4 Forwarding over Ethernet Performance

** Based on maximum bus frequency and associated data rate of 3.6 Gbps on the media interface.

ATM RAN application example

The ATM RAN application is intended for transport line cards in the 3 GPP UTRAN network. In this application, the Intel® IXP2350 network processor is tasked with processing packets from the line interface to the backplane and out a second line interface. Figures 1 and 2 illustrate the full set of functions

performed by the microengines within the IXP2350 network processor for the ATM RAN application.

In this performance assessment, two configurations of the line interface are analyzed: 2xOC-3, which is best suited for the lub interface of the RNC, and 16 T1/E1, which is best suited for the lub interface of Node B. In both configurations,

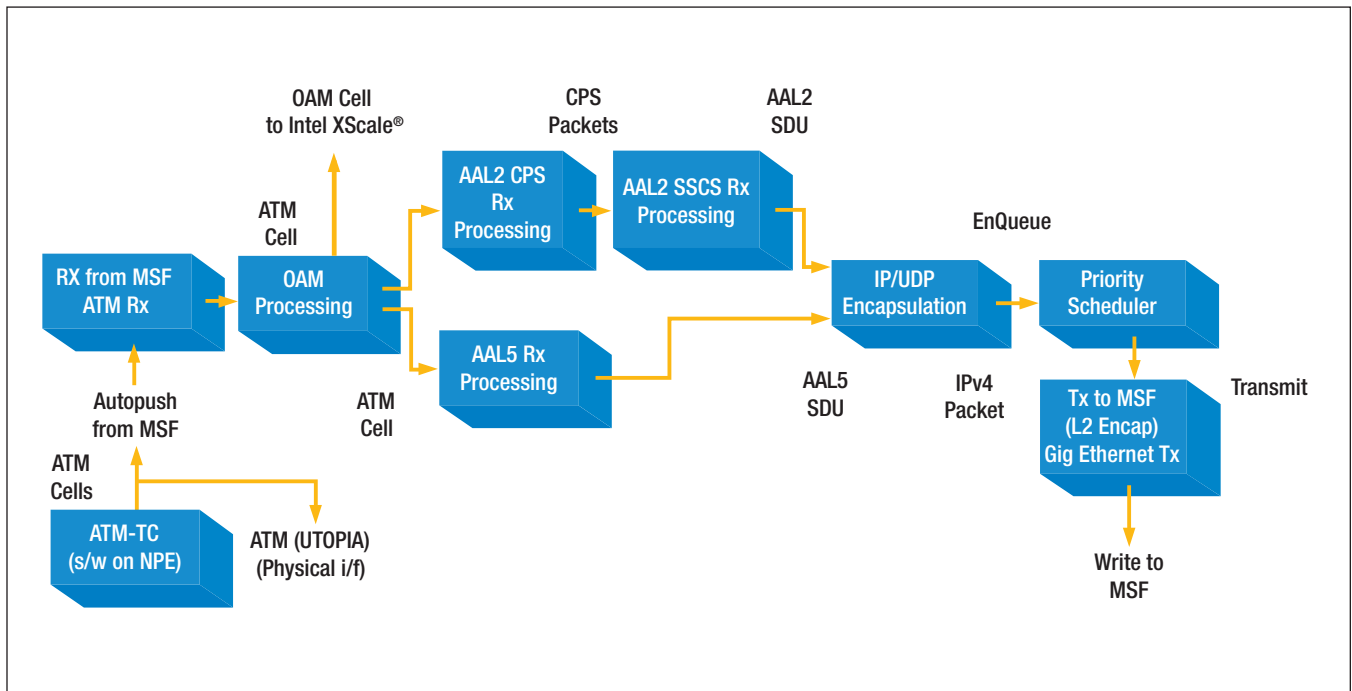


Figure 1: Data flow from the line interface to backplane. These software blocks are implemented on the microengines of the IXP2350 network processor.

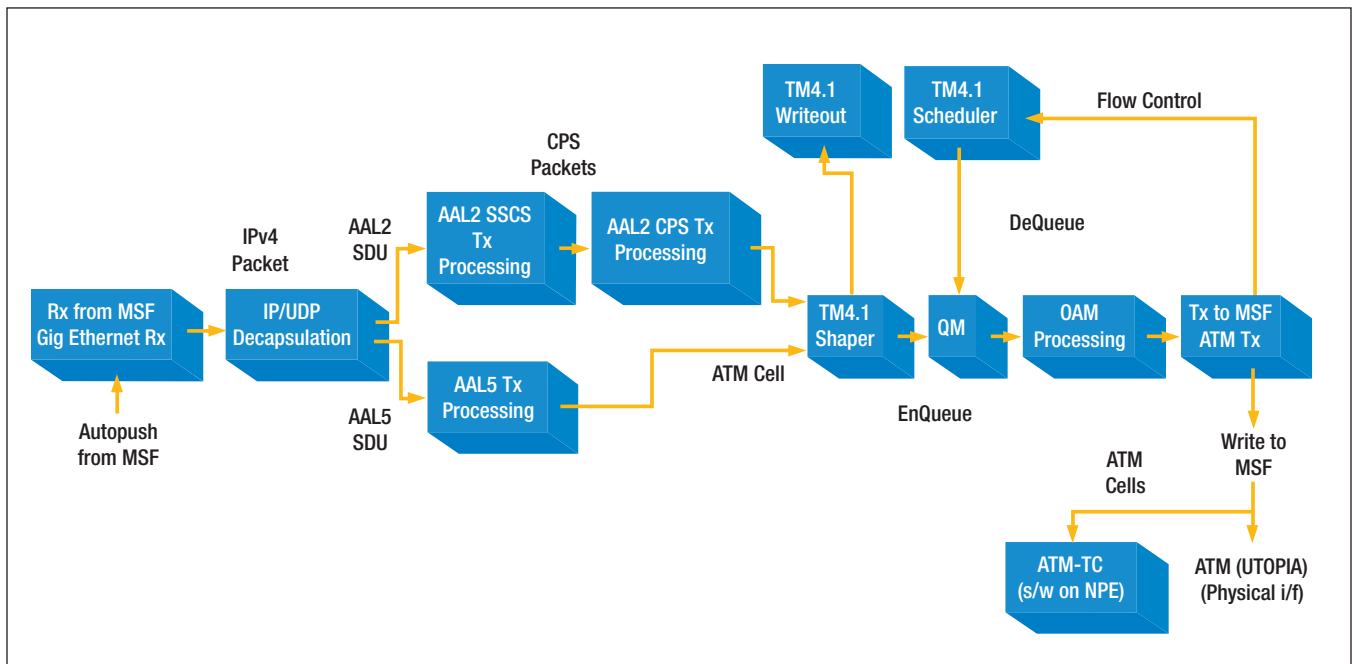


Figure 2: Data flow from the backplane to the line interface. These software blocks are implemented on the microengines of the IXP2350 network processor.

performance is quoted under “worst-case,” minimum-sized packet conditions. Additional specifications include:

- 100% AAL2 traffic
- One AAL2 cell embedded with two 20 B CPS packets
- One 20 B CPS packet is mapped to an Ethernet packet on the backplane

Under these conditions, the Intel® IXP2350 network processor provided performance results as shown in Table 3.

Line Interface Configuration	Intel® IXP2350 Network Processor Variant	Microengine Headroom
2xOC-3	900 MHz Intel® XScale core 900 MHz Microengines	28%
16 T1/E1	600 MHz Intel XScale core 300 MHz Microengines	56%

Table 3: Performance results for the ATM RAN application

Even when subjected to the most rigorous performance conditions in this ATM RAN application example, the IXP2350 network processor delivers ample headroom to perform additional packet classification, Quality of Service algorithms, or other value-added functions.

Additional application examples

In addition to ATM RAN, Intel has assessed the performance capabilities of the IXP2350 network processor for several other common access and edge applications, including

- IP RAN
- ATM+IP RAN
- Wi-Fi Aggregator/L2 Switches
- IP Routers
- DSLAM
- Metro/Edge RPR
- Wi-Fi to Ethernet Bridge

In each case, running a comprehensive range of application functions using minimum-sized packets, the IXP2350 network processor delivered line rate performance at up to 2 Gbps with sufficient headroom to support additional application services.¹ With each packet undergoing multiple individual processes on the microengines, these results illustrate that the IXP2350 network processor has the processing power needed to support a broad range of access and edge network applications.

Conclusion

The Intel® IXP23XX product line of network processors offers network equipment manufacturers a powerful mid-range platform that extends the fully programmable Intel® IXA architecture to new, lower cost/performance points for access and edge applications, including broadband access devices, wireless infrastructure systems, routers and multi-service switches. Robust processing performance for demanding, minimum-size packet applications means that customers can use these network processors with confidence to deliver value-added network services.² Because the IXP23XX product line integrates key architectural features from the Intel® IXP2XXX product line, developers can take advantage of seamless performance scalability and software reuse from T1/E1 to OC-192/10 Gbps line rates.

¹ Actual results will vary depending on how individual vendor applications are written.

² Performance comparisons should be based on minimum-sized packets.

Intel® Internet Exchange Architecture (Intel® IXA)

Intel® IXA is a packet processing architecture that provides a foundation for software portability across multiple generations of network processors. Intel IXA is based on programmable microengines, Intel XScale® technology and the Intel IXA Software Framework. Additional information on Intel IXA and the Intel network processor product lines is available at the addresses listed below.

Intel Access

Intel® Network Processors Web page	www.intel.com/go/networkprocessors
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