

Intel® IXP2400 Network Processor:

Flexible, High-Performance Solution
for Access and Edge Applications

White Paper



Overview

Many trends are driving the need for intelligence and flexibility in network systems. Intel has developed next-generation network processors optimized for applications from the customer premises to the core of the network. Intel® IXP2400 network processor delivers a new level of intelligence and performance for access and edge applications, enabling the realization of Quality-of-Service (QoS), enforcement of Service Level Agreements (SLAs), and traffic engineering at OC-48/2.5 Gbps data rates. These capabilities will allow OEMs and Service Providers to offer differentiated and tiered services to their customers while efficiently managing their network resources and bandwidth.

Target applications for the IXP2400 include multi-service switches, broadband access equipment, and wireless infrastructure. The flexible architecture and interfaces, low power consumption, and small footprint of the IXP2400 make it ideal for the target markets. This paper highlights the performance of the IXP2400 network processor for two key applications. It shows that the IXP2400 can perform (1) routing with QoS and (2) ATM Segmentation and Reassembly (SARing) with traffic management at OC-48 performance level while leaving headroom for meaningful customer applications to be executed.

Target market segment overview

Increasingly, packet processing requirements vary significantly by market segment. For example, access networking equipment must support multiple interfaces and protocols. At the same time this equipment needs to meet tight power and real estate requirements dictated by space constraints in wiring closets. Equipment deployed at the edge of the network must support rapid provisioning of services, scalable performance to provide support for emerging services at wire rate and smooth migration to emerging standards. For all applications, minimizing costs and maximizing time-in-market are also critical concerns.

The IXP2400 has the ideal set of features to support these access and edge requirements at line rates up to OC-48/2.5 Gbps. The IXP2400 performance and flexibility make it desirable for a wide variety of high-performance applications such as multi-service switches, DSLAMs (DSL access multiplexers), CMTS (cable modem termination system) equipment, 2.5G and 3G wireless infrastructure and Layer 4-7 switches including content-based load balancers, and firewalls. The programmability of the IXP2400 also makes it well suited for VoIP Gateways, multi-service access platforms, edge routers, remote access concentrators, and Virtual Private Network (VPN) Gateways.

Usage models for IXP2400 Network Processor in the target market segments listed above are as follows:

- Aggregation, QoS, ATM SARing, traffic shaping, policing, forwarding, and protocol conversion in DSLAM equipment
- Aggregation, QoS, forwarding, and protocol conversion in CMTS equipment
- ATM SARing, encryption, and forwarding in base station controllers/radio network controllers (BSC/RNC)
- General Packet Radio Services (GPRS) Tunneling Protocol tunneling and IPv6 in wireless infrastructure
- ATM SARing, Multi-protocol Label Switching (MPLS), QoS, traffic shaping, policing, protocol conversion, and aggregation for multi-service switches
- Content-aware load balancing, forwarding, and policing for edge server offload

Intel® IXP2400 network processor features and benefits

IXP2400 is a highly integrated and power efficient next-generation network processor. It offers wire-speed OC-48 networking data plane processing as well as control plane capability on a single chip. As shown in Figure 1, each IXP2400 contains eight multi-threaded packet-processing microengines, a low-power general-purpose Intel® XScale™ microarchitecture core, network media and switch fabric interfaces, memory and PCI controllers, and interfaces to flash PROM and peripheral devices. The media and switch fabric interfaces readily connect to industry-standard framers, MAC devices, or switch fabric. These interfaces get networking data into and out of the IXP2400 efficiently.

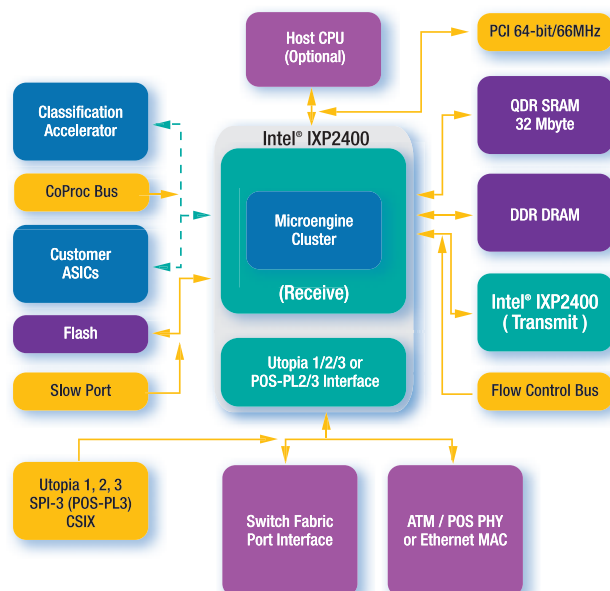


Figure 1. Intel® IXP2400 Network Processor External Features

The eight microengines are highly programmable packet processors, and support multi-threading up to eight threads each. These microengines provide a variety of network processing functions in hardware, and process data at OC-48 wire speed. Moreover, IXP2400 offers extensive communication mechanisms between all on-chip processing units, and enables the microengines to readily form different topologies of software pipelines that can be customized for various target applications and network traffic patterns. The memory controllers facilitate efficient accesses to SRAM and DRAM, which hold routing table, networking data, and various data structures like queues and data contexts. The integrated Intel XScale core offers ample processing power for running control plane software. The PCI controller facilitates communication with external host processors and other chips that are connected through the PCI bus.

The IXP2400 microengine design implements additional, hardware-assisted features to increase performance and simplify development. These new features include:

- A multiplier to improve performance and code density for QoS algorithms like metering and traffic shaping.
- A pseudo random number generator to accelerate congestion avoidance algorithms like WRED (Weighted Random Early Discard).
- Cyclic Redundancy Check (CRC) generator to automate CRC generation for ATM AAL5, Ethernet, Frame Relay, and HDLC applications.
- 16-entry Content Addressable Memory (CAM) configured as a distributed cache. The CAM facilitates efficient data sharing among microengine threads, resulting in greater performance as well as reduced consumption of precious memory bandwidth.
- A 64-bit local timer with programmable time-out signaling to enhance traffic scheduling and shaping.
- Memory features to accelerate updates to shared memory locations among all on-chip processing elements.

IXP2400 offers a variety of low latency communication mechanisms among the microengines and the integrated Intel XScale core. These communication mechanisms consist of dedicated high-speed data-paths between neighboring microengines, data-paths between all microengines, shared on-chip Scratchpad memory, and shared FIFO ring buffers in Scratchpad memory and SRAM. These innovations enable the microengines to form various topologies of software pipelines flexibly and efficiently, allowing processing to be tuned to specific applications and traffic patterns. This combination of programming flexibility and efficient inter-process communication ensures performance headroom while minimizing processing latency.

Network processing typically involves extensive queue management. Depending on the applications and algorithms used, the network processor may manage many thousands of packet queues. Moreover, the network processor must execute the desired scheduling algorithm, and select the appropriate packets out of these queues for transmission at wire speed. As a result, effective queue management is key to high-performance network processing and to reducing development complexity. IXP2400 features high-performance queue management hardware that automates adding data to and removing data from queues. Queues can be accessed simultaneously by multiple threads, and there is no limit on the size or total number of queues which can be managed.

IXP2400 system configurations and performance analysis

IP forwarding, IP DiffServ and QoS, ATM SARing, ATM policing and shaping are key functions performed by equipment in the target market segment for the IXP2400. Understanding the performance of these applications is critical for vendors when choosing a network processor. The following sections highlight the performance of the IXP2400 network processor for these applications.

Figure 2 shows a full duplex OC-48 line card configuration with two IXP2400 processors in a typical multi-service switch/router used in edge equipment. The network interface is based on industry standards and can be either SPI-3 (for PoS/IP traffic) or Utopia (for ATM traffic). The fabric interface is standards-based CSIX. Both interfaces can be clocked up to 125 MHz to provide sufficient head-room for encapsulation overhead. This configuration was used to estimate the performance of the IPv4 forwarding + DiffServ application and the ATM AAL5 SARing and Traffic Management applications that follow.

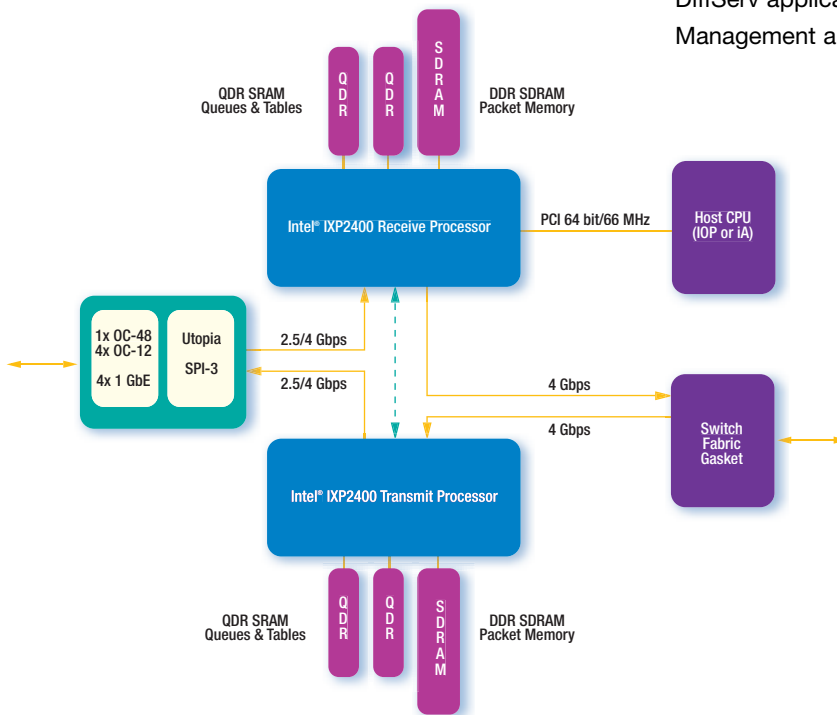


Figure 2. OC-48 line card configuration

IXP2400 performance summary

The following table summarizes performance of the IXP2400 running applications representative of the target market segments described in this white paper. The table also shows the performance comparison to the current generation IXP1200.

Table 1 illustrates:

- IXP2400 supports OC-48 line rate (2.5 Gb/s) executing an IPv4/IPv6 forwarding + DiffServ application for minimum sized Packet over Sonet (PoS) packets. IXP2400 also supports 4.1 Gb/s line rate for this application with 64 byte minimum size Ethernet packets.
- IXP2400 supports ATM AAL5 segmentation and re-assembly and TM4.1 compliant Constant Bit Rate (CBR), Variable Bit Rate (VBR), and Unspecified Bit Rate (UBR) traffic shapers for minimum sized AAL5 frames (53 bytes) at OC-48 line rate.
- IXP2400 provides a 4X to 16X performance boost compared to the current generation IXP1200, making it a compelling processor to meet the demanding needs of the next-generation OC-48 edge and access market segment applications.

IPv4 forwarding + DiffServ application

In order to meet OC-48 line rate for minimum PoS packet of 46 byte (40 byte IP payload + 6 byte PPP/HDL overhead), the IXP2400 microengines, running at 600 MHz, execute each pipeline stage of this application in 88 cycles (the minimum size packet inter-arrival time).

The ingress IXP2400 processor receives PoS frames that carry IP payload. Since the IXP2400 supports up to 16 logical ports on the framer, the IP packet segments can arrive interleaved. The first pipeline stage reassembles these segments into complete IP packets in the DDR packet memory. In the subsequent pipe stages, the ingress processor performs the following tasks:

- Route lookup to determine the next hop forwarding information by executing a Longest Prefix Match (LPM) algorithm on the destination IP address.
- IP packet classification into flows and queues using either a 5-tuple or a 7-tuple lookup—i.e., classification based on IP source and destination address, TCP source and destination ports, protocol field, L2 port etc.
- Execution of a single rate three color marker (SrTCM) meter pipeline stage to meter the traffic on a per flow basis and mark the packet as green, yellow or red based on the flow parameters and arrival rate.
- Execution of a congestion avoidance algorithm such as WRED (Weighted Random Early Discard) that will randomly drop packets when the queue lengths exceed certain thresholds with the goal of minimizing congestion in the fabric.

Table 1—Intel® IXP2400 Performance

Application	Media Interface	Minimum Packet Size	IXP2400 Performance	IXP1200 Performance
IPv4 forwarding + IP DiffServ	PoS	46 bytes	OC-48, 2.5 Gb/s	OC-12, 622 Mb/s
IPv4 forwarding + IP DiffServ	Ethernet	64 bytes	4 Gb/s	1 Gb/s
ATM AAL5 SAR + TM4.1 compliant traffic shapers	Utopia	53 bytes	OC-48, 2.5 Gb/s	OC-3, 155 Mb/s
IPv6 forwarding + IP DiffServ	PoS	66 bytes	OC-48, 2.5 Gb/s	OC-12, 622 Mb/s

IPv4 forwarding + DiffServ application *(continued)*

One of the key challenges to meeting OC-48 line rate performance is the ability to perform queue add and delete operations at twice the line rate and still support large number of queues. IXP2400 provides specialized on-chip hardware assist to achieve this level of performance.

The transmit pipeline includes fully programmable support for schedulers to schedule traffic into the fabric, and a transmit engine to add fabric encapsulation to the packet data, move packet data from memory and to the transmit buffers, and enable data transmission on the CSIX interface.

The pipeline stages of the egress processor receive the CSIX traffic, reassemble the original IP payload, perform further classification if required, and execute metering and congestion avoidance algorithms to provide QoS guarantees to the traffic going back to the network. Sophisticated scheduling algorithms can be implemented on the egress processor to provide further QoS capabilities for the network-bound traffic.

For purposes of performance analysis, Weighted Round Robin was used as the scheduling algorithm for the ingress stage, and Deficit Round Robin was used for the egress stage.

ATM AAL5 segmentation, reassembly and TM4.1-compliant traffic shaping application

The line card configuration used above can also support a full duplex OC-48 ATM application that performs AAL5 SAR + TM4.1-compliant shaping. In this configuration, budget for each pipeline stage is determined by the ATM cell size of 53 bytes that can carry a minimum AAL5 frame (40 bytes of IP payload + 8 bytes of AAL5 trailer + 5 bytes of ATM header). In order to meet the OC-48 line rate requirement, each stage of this application executes in 100 cycles.

While executing this application, the first pipeline stage of the ingress IXP2400 reassembles the received ATM cells into AAL5 frames, and performs the CRC-32 check required by the AAL5 protocol using the dedicated CRC hardware in each microengine. Subsequent pipeline stages on the ingress processor all operate on the AAL5 IP frame and are similar to the blocks described in the IPv4 forwarding + DiffServ application above. The IP traffic is transmitted over the CSIX fabric to other line cards.

The egress processor on the ATM line card receives AAL5 frames over the CSIX interface. These AAL5 frames are classified further if required. The egress processor also executes IP QoS blocks such as meter and/or congestion avoidance on the AAL5 frame prior to queuing up the frames. The transmit pipeline on this processor executes the TM4.1-compliant traffic policing (Generic Cell Rate Algorithm) and shaping algorithm such as CBR, real time-Variable Bit Rate (rt-VB), non-real time-Variable Bit Rate (nrt-VB), and UBR to police and shape the outgoing ATM traffic. The final pipeline stage performs the AAL5 segmentation operation (CRC-32 computation, AAL5 trailer generation, etc.) and transfers ATM cells over the ATM interface.

OC-12 line card configuration for DSLAM and RNC

The flexibility of the IXP2400 media interface allows each of the two 32-bit interfaces to be independently partitioned into either 8-bit or 16-bit channels that can be either receive or transmit interfaces using industry-standard PoS-PHY or Utopia protocol. This allows a single IXP2400 chip to support either one or two full duplex OC-12 applications.

The following figure shows a typical single chip IXP2400 configuration. Examples of such configurations are an RNC card in a wireless application, a resource card used in a VoIP application, and a line card in a CMTS application.

In this configuration, the media receive and transmit interfaces can be PoS or Utopia. The IXP2400 will handle PoS frames, Ethernet frames or ATM cells.

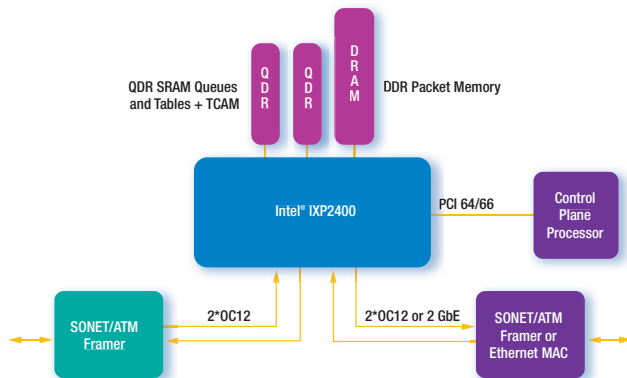


Figure 3. The above configuration was used to estimate the performance of OC-12 applications

IPv4 forwarding + DiffServ application at 2*OC12

A single IXP2400 can support the entire IPv4 forwarding + DiffServ applications described earlier at a data rate of full duplex 2*OC-12. The total receive and transmit data bandwidth at full duplex 2*OC-12 is the same as the data bandwidth of half duplex OC-48 (5 Gb/s). Since the inter-packet arrival time at 2*OC-12 is double the OC-48 rate, the budget for each pipeline stage executing on the IXP2400 microengine is 176 cycles, assuming the minimum PoS packet size of 46 bytes. Thus the eight microengines on the single IXP2400 can execute the entire ingress and egress pipeline stages described earlier to deliver wire-speed full duplex performance at 2*OC-12.

VoIP or VoATM application at OC-12

A typical voice gateway application requires some or all of the following operations to be executed on the incoming packets/cells:

- AAL2 and/or AAL5 segmentation and reassembly
- Connection table lookup based on ATM Virtual Circuit/Virtual Path (VC/VP), Channel ID, IP, TCP, UDP, RTP header fields
- Encapsulation/de-encapsulation of payload for different media types
- LPM or table-based route lookup, n-tuple packet classification
- QoS blocks such as metering, WRED, DRR/WRR scheduler, ATM traffic shapers.

The IXP2400, with eight, 600 MHz microengines and all the features described previously, provides sufficient horsepower to execute this class of application and deliver full duplex wire-speed performance at OC-12 data rate.

Summary

Next-generation access and edge equipment require flexible programming, high performance, low power consumption, and small real estate. These applications require support for diverse functions such as IP forwarding with QoS, ATM AAL5 Segmentation and Reassembly and traffic shaping.

The IXP2400 network processor has been optimized to meet these requirements. The eight microengines provide fully flexible programming and processing power to meet OC-48/2.5 Gbps wire-rate performance. The flexible media interface allows a variety of media devices to be connected without glue logic to the IXP2400 for easier design and lower system cost. Performance analysis demonstrates that the Intel IXP2400 network processor is an ideal product for meeting these requirements at OC-12 to OC-48 wire-rate.

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