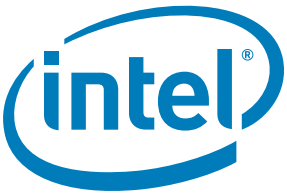

# Intel® Celeron® Processor 200Δ Sequence

## Datasheet

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# Revision History

| Revision Number | Description | Date |
|---|---|---|
| -001 | • Initial Release | October 2007 |

# Intel® Celeron® Processor 200 Sequence Features

- Available at 1.2 GHz
- Supports Intel® 64 architecture
- Supports Execute Disable Bit capability
- Binary compatible with applications running on previous members of the Intel microprocessor line
- FSB frequency at 533 MHz
- Advance Dynamic Execution
- Very deep out-of-order execution
- Enhanced branch prediction
- Optimized for 32-bit applications running on advanced 32-bit operating systems
- Two 32-KB Level 1 data caches
- 512 KB Advanced Smart Cache
- Advanced Digital Media Boost
- Enhanced floating point and multimedia unit for enhanced video, audio, encryption, and 3D performance
- Power Management capabilities
- System Management mode
- 8-way cache associativity provides improved cache hit rate on load/store operations
- 479-pin FC-BGA6 Package

The Intel Celeron processor 200 sequence delivers Intel's advanced low-powered processors for desktop PCs. The processor is designed to deliver PC experience across applications and usages. These applications include Internet browsing, send and receive emails, keeping track of personal finance, and multimedia applications.

Intel® 64 architecture enables the processor to execute operating systems and applications written to take advantage of the Intel 64 architecture. The Intel Celeron processor 200 sequence also includes the Execute Disable Bit capability. This feature, combined with a supported operating system, allows memory to be marked as executable or non-executable.

§

# 1 Introduction

The Intel® Celeron® processor 200 sequence is a desktop processor that combines the performance of the previous generation of desktop products with the power efficiencies of a low-power microarchitecture to enable smaller, quieter systems. The Intel Celeron processor 200 sequence is a 64-bit processor that maintains compatibility with IA-32 software.

The Intel Celeron processor 200 sequence uses a Flip-Chip Ball Grid Array (FC-BGA6) package technology that direct solder down to a 479-pin footprint on PCB surface. The processor can be used on SiS662 and SiS964L Chipset family-based systems.

***Note:*** In this document the Intel Celeron processor 200 sequence is also referred to as "the processor".

***Note:*** In this document the Intel Celeron processor 200 sequence refers to the Intel Celeron processor 220.

Based on 65 nm process technology, the Intel Celeron processor 200 sequence is a single-core processor that features an 533 MHz front side bus (FSB) and 512 KB L2 cache. The processor also supports the Execute Disable Bit and Intel® 64 architecture.

The processor front side bus (FSB) uses a split-transaction, deferred reply protocol like the Intel® Pentium® 4 processor. The FSB uses Source-Synchronous Transfer (SST) of address and data to improve performance by transferring data four times per bus clock (4X data transfer rate, as in AGP 4X). Along with the 4X data bus, the address bus can deliver addresses two times per bus clock and is referred to as a "double-clocked" or 2X address bus. Working together, the 4X data bus and 2X address bus provide a data bus bandwidth of up to 6.4 GB/s.

Intel will enable support components for the processor including heatsink, and heatsink retention mechanism. Supported platforms may need to be refreshed to ensure the correct voltage regulation. Manufacturability is a high priority; hence, mechanical assembly may be completed from the top of the baseboard and should not require any special tooling.

## 1.1 Terminology

A ‘#’ symbol after a signal name refers to an active low signal, indicating a signal is in the active state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the ‘#’ symbol implies that the signal is inverted. For example, D[3:0] = ‘HLHL’ refers to a hex ‘A’, and D[3:0]# = ‘LHLH’ also refers to a hex ‘A’ (H= High logic level, L= Low logic level).

Front Side Bus” refers to the interface between the processor and system core logic (a.k.a. the chipset components). The FSB is a multiprocessing interface to processors, memory, and I/O.



### 1.1.1 Processor Packaging Terminology

Commonly used terms are explained here for clarification:

- **Intel Celeron Processor 200 Sequence** — Single core processor in the FC-BGA6 package with a 512 KB L2 cache.
- **Processor** — For this document, the term processor is the generic form of the Intel Celeron processor 200 sequence. The processor is a single package that contains one exectution unit.
- **Keep-out zone** — The area on or near the processor that system design can not use.
- **Processor core** — Processor core die with integrated L2 cache.
- **FSB (Front Side Bus)** — The electrical interface that connects the processor to the chipset. Also referred to as the processor system bus or the system bus. All memory and I/O transactions as well as interrupt messages pass between the processor and chipset over the FSB.
- **Storage conditions** — Refers to a non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor pins should not be connected to any supply voltages, have any I/Os biased, or receive any clocks. Upon exposure to “free air”(i.e., unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
- **Functional operation** — Refers to normal operating conditions in which all processor specifications, including DC, AC, system bus, signal quality, mechanical and thermal are satisfied.
- **Execute Disable Bit** — The Execute Disable bit allows memory to be marked as executable or non-executable, when combined with a supporting operating system. If code attempts to run in non-executable memory the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer over run vulnerabilities and can, thus, help improve the overall security of the system. See the Intel® Architecture Software Developer's Manual for more detailed information.
- **Intel® 64 Architecture** — An enhancement to Intel's IA-32 architecture, allowing the processor to execute operating systems and applications written to take advantage of the Intel® 64 architecture. Further details on Intel® 64 architecture and programming model can be found in the Intel Extended Memory 64 Technology Software Developer Guide at http://developer.intel.com/technology/64bitextensions/.

## 1.2 References

Material and concepts available in the following documents may be beneficial when reading this document.

| Document | Location |
|---|---|
| *Intel® Celeron® Processor 200 Sequence Specification Update* | http://developer.intel.com/design/processor/specupdt/318547.htm |
| *Intel® Celeron® Processor 200 Sequence Thermal and Mechanical Design Guidelines* | http://developer.intel.com/design/processor/designex/318548.htm |
| *Intel® 64 and IA-32 Architecture Software Developer's Manuals*<br>*Intel® 64 and IA-32 Architecture Software Developer's Manual Volume 1: Basic Architecture*<br>*Intel® 64 and IA-32 Architecture Software Developer's Manual Volume 2A: Instruction Set Reference Manual A–M*<br>*Intel® 64 and IA-32 Architecture Software Developer's Manual Volume 2B: Instruction Set Reference Manual, N–Z*<br>*Intel® 64 and IA-32 Architecture Software Developer's Manual Volume 3A: System Programming Guide*<br>*Intel® 64 and IA-32 Architecture Software Developer's Manual Volume 3B: System Programming Guide* | http://www.intel.com/products/processor/manuals/ |

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# 2 Low Power Features

## 2.1 Power-On Configuration Options

Several configuration options can be configured by hardware. The processor samples the hardware configuration at reset, on the active-to-inactive transition of RESET#. For specifications on these options, refer to Table 1.

The sampled information configures the processor for subsequent operation. These configuration options cannot be changed except by another reset. All resets reconfigure the processor; for reset purposes, the processor does not distinguish between a "warm" reset and a "power-on" reset.

**Table 1. Power-On Configuration Option Signals**

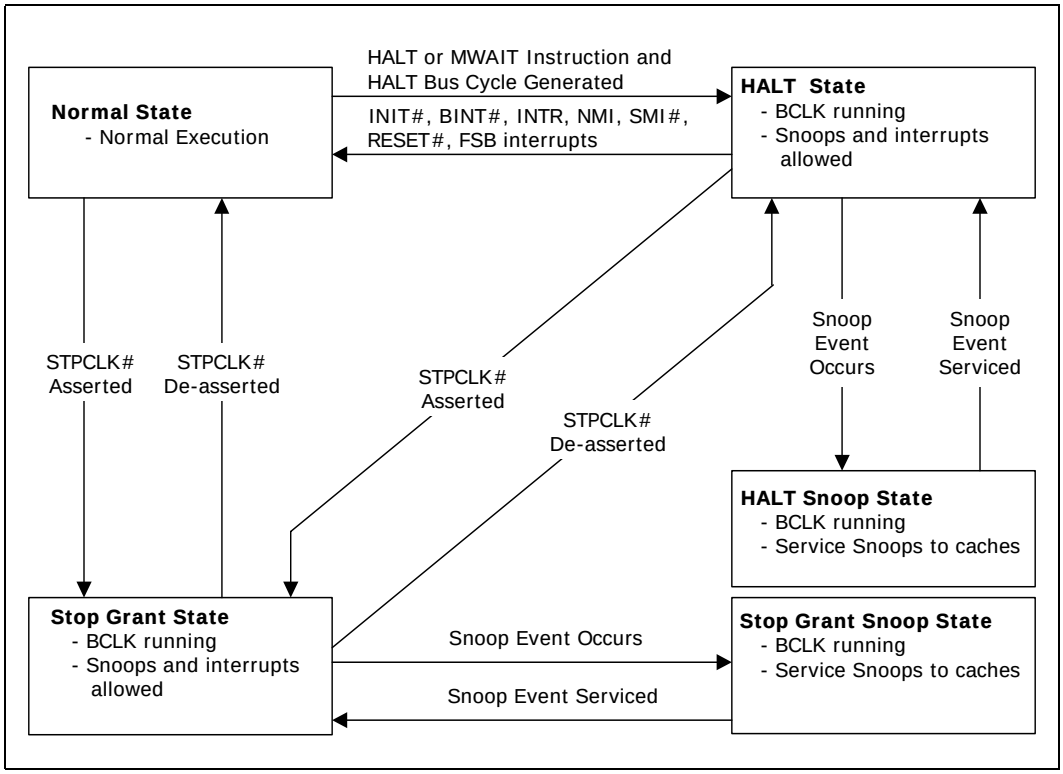
| Configuration Option | Signal[1,2] |
|---|---|
| Output tristate | SMI# |
| Execute BIST | A3# |
| Symmetric agent arbitration ID | BR0# |
| RESERVED | A[8:4]#, A[24:11]#, A[35:26]# |

**NOTE:**
1. Asserting this signal during RESET# will select the corresponding option.
2. Address signals not identified in this table as configuration options should not be asserted during RESET#.

## 2.2 Clock Control and Low Power States

The processor allows the use of AutoHALT and Stop-Grant states which may reduce power consumption by stopping the clock to internal sections of the processor, depending on each particula r state. See Figure 2.1 for a visual representation of the processor low power states.

**Figure 1. Processor Low Power State Machine**




## 2.2.1 Normal State

This is the normal operating state for the processor.

### 2.2.1.1 HALT Powerdown State

HALT is a low power state entered when all the processor cores have executed the HALT or MWAIT instructions. When one of the processor cores executes the HALT instruction, that processor core is halted, however, the other processor continues normal operation. The processor will transition to the Normal state upon the occurrence of SMI#, INIT#, or LINT[1:0] (NMI, INTR). RESET# will cause the processor to immediately initialize itself.

The return from a System Management Interrupt (SMI) handler can be to either Normal Mode or the HALT Power Down state. See the *Intel Architecture Software Developer's Manual, Volume III: System Programmer's Guide* for more information.

The system can generate a STPCLK# while the processor is in the HALT Power Down state. When the system de-asserts the STPCLK# interrupt, the processor will return execution to the HALT state.

While in HALT Power Down state, the processor will process bus snoops.

### 2.2.2 Stop Grant State

When the STPCLK# signal is asserted, the Stop Grant state of the processor is entered 20 bus clocks after the response phase of the processor-issued Stop Grant Acknowledge special bus cycle.

Since the GTL+ signals receive power from the FSB, these signals should not be driven (allowing the level to return to $V_{CCP}$) for minimum power drawn by the termination resistors in this state. In addition, all other input signals on the FSB should be driven to the inactive state.

RESET# will cause the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. A transition back to the Normal state will occur with the de-assertion of the STPCLK# signal.

A transition to the Grant Snoop state will occur when the processor detects a snoop on the FSB (see Section 2.2.3).

While in the Stop-Grant State, SMI#, INIT#, and LINT[1:0] will be latched by the processor, and only serviced when the processor returns to the Normal State. Only one occurrence of each event will be recognized upon return to the Normal state.

While in Stop-Grant state, the processor will process a FSB snoop.

### 2.2.3 HALT Snoop State and Stop Grant Snoop State

The processor will respond to snoop transactions on the FSB while in Stop-Grant state or in HALT Power Down state. During a snoop transaction, the processor enters the HALT Snoop State:Stop Grant Snoop state. The processor will stay in this state until the snoop on the FSB has been serviced (whether by the processor or another agent on the FSB). After the snoop is serviced, the processor will return to the Stop Grant state or HALT Power Down state, as appropriate.

# 3 Electrical Specifications

This chapter describes the electrical characteristics of the processor interfaces and signals. DC electrical characteristics are provided.

## 3.1 Power and Ground Pins

The processor has VCC (power), VCCP and VSS (ground) inputs for on-chip power distribution. All power pins must be connected to $V_{CC}$, while all VSS pins must be connected to a system ground plane. The processor VCC pins must be supplied by the voltage determined by the **V**oltage **ID**entification (VID) pins.

The signals denoted as VCCP, provide termination for the front side bus and power to the I/O buffers. A separate supply must be implemented for these pins, that meets the $V_{CCP}$ specifications outlined in Table 5.

## 3.2 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the processor is capable of generating large current swings. This may cause voltages on power planes to sag below their minimum specified values if bulk decoupling is not adequate. Larger bulk storage ($C_{BULK}$), such as electrolytic or aluminum-polymer capacitors, supply current during longer lasting changes in current demand by the component, such as coming out of an idle condition. Similarly, they act as a storage well for current when entering an idle condition from a running condition. The motherboard must be designed to ensure that the voltage provided to the processor remains within the specifications listed in Table 5. Failure to do so can result in timing violations or reduced lifetime of the component.

### 3.2.1 $V_{CC}$ Decoupling

$V_{CC}$ regulator solutions need to provide sufficient decoupling capacitance to satisfy the processor voltage specifications. This includes bulk capacitance with low effective series resistance (ESR) to keep the voltage rail within specifications during large swings in load current. In addition, ceramic decoupling capacitors are required to filter high frequency content generated by the front side bus and processor activity. Consult the *Intel(R) IMVP-6 Mobile Processor Voltage Regulation Specification* and appropriate platform design guidelines for further information.

### 3.2.2 $V_{CCP}$ Decoupling

Decoupling must be provided on the motherboard. Decoupling solutions must be sized to meet the expected load. To ensure compliance with the specifications, various factors associated with the power delivery solution must be considered including regulator type, power plane and trace sizing, and component placement. A conservative decoupling solution would consist of a combination of low ESR bulk capacitors and high frequency ceramic capacitors.

### 3.2.3 FSB Decoupling

The processor integrates signal termination on the die. In addition, some of the high frequency capacitance required for the FSB is included on the processor package. However, additional high frequency capacitance must be added to the motherboard to properly decouple the return currents from the front side bus. Bulk decoupling must also be provided by the motherboard for proper [A]GTL+ bus operation.

## 3.3 Voltage Identification

The Voltage Identification (VID) specification for the processor is defined by the *Intel(R) IMVP-6 Mobile Processor Voltage Regulation Specification*. The voltage set by the VID signals is the reference VR output voltage to be delivered to the processor $V_{CC}$ pins. Refer to Table 13 for the DC specifications for these signals. Voltages for each processor frequency is provided in Table 5.

Individual processor VID values may be calibrated during manufacturing such that two devices at the same core speed may have different default VID settings. This is reflected by the VID Range values provided in Table 5.

The processor uses seven voltage identification signals, VID[6:0], to support automatic selection of power supply voltages. Table 2 specifies the voltage level corresponding to the state of VID[6:0]. A '1' in this table refers to a high voltage level and a '0' refers to a low voltage level. If the processor socket is empty (VID[6:0] = 1111111), or the voltage regulation circuit cannot supply the voltage that is requested, it must disable itself.

The processor provides the ability to operate while transitioning to an adjacent VID and its associated processor core voltage ($V_{CC}$). This will represent a DC shift in the load line. It should be noted that a low-to-high or high-to-low voltage state change may result in as many VID transitions as necessary to reach the target core voltage. Transitions above the specified VID are not permitted. Table 5 includes VID step sizes and DC shift ranges. Minimum and maximum voltages must be maintained as shown in Table 6 and Figure 2 as measured across the VCC_SENSE and VSS_SENSE pins.

The VRM or VRD used must be capable of regulating its output to the value defined by the new VID. DC specifications for dynamic VID transitions are included in Table 5 and Table 6. Refer to the *Intel(R) IMVP-6 Mobile Processor Voltage Regulation Specification* for further details.

**Table 2. Voltage Identification Definition (Sheet 1 of 4)**

| VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | $V_{CC}$ (V) |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1.5000 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1.4875 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1.4750 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1.4625 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1.4500 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1.4375 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1.4250 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1.4125 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1.4000 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1.3875 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1.3750 |

## Table 2. Voltage Identification Definition (Sheet 2 of 4)

| VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | $V_{CC}$ (V) |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1.3625 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1.3500 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1.3375 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1.3250 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1.3125 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1.3000 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1.2875 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1.2750 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1.2625 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1.2500 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1.2375 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1.2250 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1.2125 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1.2000 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1.1875 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1.1750 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1.1625 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1.1500 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1.1375 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1.1250 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1.1125 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1.1000 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1.0875 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1.0750 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1.0625 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1.0500 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1.0375 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1.0250 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1.0125 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1.0000 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0.9875 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0.9750 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0.9625 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0.9500 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0.9375 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0.9250 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0.9125 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0.9000 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0.8875 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0.8750 |

**Table 2. Voltage Identification Definition (Sheet 3 of 4)**

| VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | $V_{CC}$ (V) |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0.8625 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0.8500 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0.8375 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0.8250 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0.8125 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0.8000 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0.7875 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0.7750 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0.7625 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0.7500 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0.7375 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0.7250 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0.7125 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0.7000 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0.6875 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0.6750 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0.6625 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0.6500 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0.6375 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0.6250 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0.6125 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0.6000 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0.5875 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0.5750 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0.5625 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0.5500 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0.5375 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0.5250 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0.5125 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0.5000 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0.4875 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0.4750 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0.4625 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0.4500 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0.4375 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0.4250 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0.4125 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0.4000 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0.3875 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0.3750 |

**Table 2. Voltage Identification Definition (Sheet 4 of 4)**

| VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | $V_{CC}$ (V) |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0.3625 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0.3500 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0.3375 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0.3250 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0.3125 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0.3000 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0.2875 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0.2750 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0.2625 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0.2500 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0.2375 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0.2250 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0.2125 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0.2000 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0.1875 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0.1750 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0.1625 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0.1500 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0.1375 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0.1250 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0.1125 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0.1000 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0.0875 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0.0750 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0.0625 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0.0500 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0.0375 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0.0250 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0.0125 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0.0000 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0.0000 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0.0000 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0.0000 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0.0000 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0.0000 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0.0000 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0.0000 |

## 3.4 Catastrophic Thermal Protection

The Celeron processor supports the THERMTRIP# signal for catastrophic thermal protection. An external thermal sensor should also be used to protect the processor and the system against excessive temperatures. Even with the activation of THERMTRIP#, which halts all processor internal clocks and activity, leakage current can be high enough such that the processor cannot be protected in all conditions without the removal of power to the processor. If the external thermal sensor detects a catastrophic processor temperature of 125 °C (maximum), or if the THERMTRIP# signal is asserted, the $V_{CC}$ supply to the processor must be turned off within 500 ms to prevent permanent silicon damage due to thermal runaway of the processor. THERMTRIP# functionality is not ensured if the PWRGOOD signal is not asserted.

## 3.5 Reserved and Unused Pins

All RESERVED (RSVD) pins must remain unconnected. Connection of these pins to $V_{CC}$, $V_{SS}$, or to any other signal (including each other) can result in component malfunction or incompatibility with future Celeron processors. See Section 4.2 for a pin listing of the processor and the location of all RSVD pins.

For reliable operation, always connect unused inputs or bidirectional signals to an appropriate signal level. Unused active low GTL+ inputs may be left as no connects if GTL+ termination is provided on the processor silicon. Unused active high inputs should be connected through a resistor to ground ($V_{SS}$). Unused outputs can be left unconnected.

The TEST1 and TEST2 pins must have a stuffing option of separate pulldown resistors to $V_{SS}$. For testing purposes, route the TEST3 and TEST5 signals through a ground referenced $Z_0$ = 55-Ω trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

## 3.6 FSB Frequency Select Signals (BSEL[2:0])

The BSEL[2:0] signals are used to select the frequency of the processor input clock (BCLK[1:0]). These signals should be connected to the clock chip and the chipset system on the platform. The BSEL encoding for BCLK[1:0] is shown in Table 3.

**Table 3. BSEL[2:0] Encoding for BCLK Frequency**

| BSEL[2] | BSEL[1] | BSEL[0] | BCLK Frequency |
|---|---|---|---|
| L | L | L | RESERVED |
| L | L | H | 133 MHz |

# 3.7 Voltage and Current Specification

## 3.7.1 Absolute Maximum and Minimum Ratings

Table 4 specifies absolute maximum and minimum ratings only and lie outside the functional limits of the processor. Within functional operation limits, functionality and long-term reliability can be expected.

At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time then, when returned to conditions within the functional operating condition limits, it will either not function, or its reliability will be severely degraded.

Although the processor contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

**Table 4. Absolute Maximum and Minimum Ratings**

| Symbol | Parameter | Min | Max | Unit | Notes[1, 2] |
|---|---|---|---|---|---|
| $V_{CC}$ | Core voltage with respect to $V_{SS}$ | –0.3 | 1.55 | V | - |
| $V_{CCP}$ | FSB termination voltage with respect to $V_{SS}$ | –0.3 | 1.55 | V | - |
| $V_{inGTL+}$ | GTL+ buffer DC input voltage with respect to $V_{SS}$ | -0.1 | 1.55 | V | |
| $T_{STORAGE}$ | Processor storage temperature | –40 | 85 | °C | 3, 4, 5 |

**NOTES:**
1. For functional operation, all processor electrical, signal quality, mechanical and thermal specifications must be satisfied.
2. Excessive overshoot or undershoot on any signal will likely result in permanent damage to the processor.
3. Storage temperature is applicable to storage conditions only. In this scenario, the processor must not receive a clock, and no pins can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. For functional operation, refer to the processor junction temperature specifications.
4. This rating applies to the processor and does not include any tray or packaging.
5. Failure to adhere to this specification can affect the long term reliability of the processor.

## 3.7.2 DC Voltage and Current Specification

### Table 5. Voltage and Current Specifications

| Symbol | Parameter | | Min | Typ | Max | Unit | Notes[2, 15] |
|---|---|---|---|---|---|---|---|
| VID Range | VID | | 1.0000 | — | 1.3375 | V | 3 |
| $V_{CC}$ | Processor Number 220 | Core $V_{CC}$ 1.20 GHz | Refer to Table 6 and Figure 2 | | | V | 4, 5, 6 |
| $V_{CC\_BOOT}$ | Default $V_{CC}$ voltage for initial power up | | — | 1.20 | — | V | |
| $V_{CCA}$ | PLL $V_{CC}$ | | - 5% | 1.50 | + 5% | | |
| $I_{CC}$ | Processor Number 220 | 1.20 GHz | — | — | 24 | A | 7 |
| $V_{CCP}$ | FSB termination voltage (DC + AC specifications) | | 1.00 | 1.05 | 1.3 | V | 8 |
| $I_{TT}$ | $I_{CC}$ for $V_{CCP}$ supply before $V_{CC}$ stable<br>$I_{CC}$ for $V_{CCP}$ supply after $V_{CC}$ stable | | — | — | 4.5<br>4.6 | A | 9 |
| $I_{CC\_VCCA}$ | $I_{CC}$ for PLL pin | | — | — | 130 | mA | |
| $I_{CC\_GTLREF}$ | $I_{CC}$ for GTLREF | | — | — | 200 | µA | |

**NOTES:**

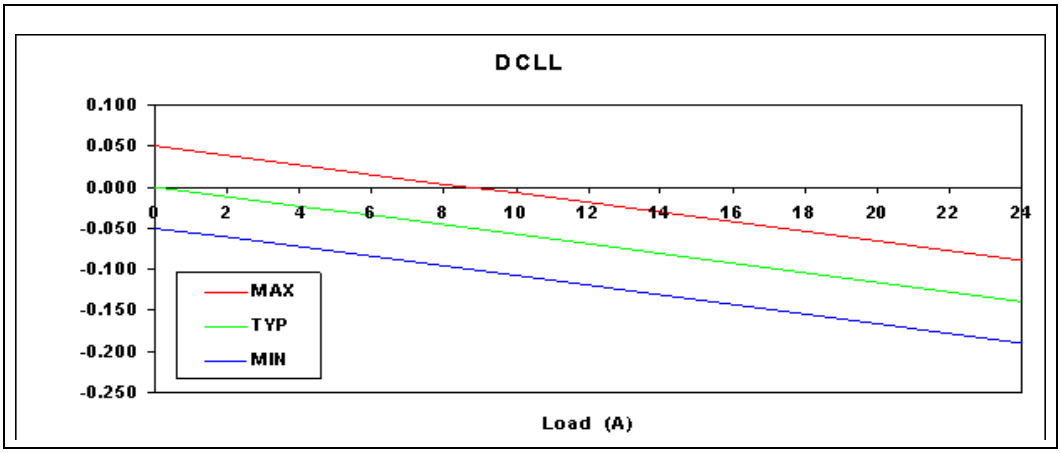
1. Unless otherwise noted, all specification in this table are based on estimates and simulation or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Adherence to the voltage specification for the processor are required to ensure reliable processor operation.
3. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and can not be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range.
4. These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required. See Section 3.3 and Table 2 for more information.
5. The voltage specification requirements are measured across VCC_SENSE and VSS_SENSE pins at the socket with a 100 MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
6. Refer to Table 6 and Figure 2 for the minimum, typical, and maximum $V_{CC}$ allowed for a given current. The processor should not be subjected to any $V_{CC}$ and $I_{CC}$ combination wherein $V_{CC}$ exceeds $V_{CC\_MAX}$ for a given current.
7. $I_{CC\_MAX}$ specification is based on the $V_{CC\_MAX}$ loadline. Refer to Figure 2 for details.
8. $V_{CCP}$ must be provided via a separate voltage source and not be connected to $V_{CC}$. This specification is measured at the pin and recommended to set at 1.05 V typical.
9. This is maximum total current drawn from $V_{CCP}$ plane by only the processor. This specification does not include the current coming from $R_{TT}$ (through the signal line). Refer to the *Intel(R) IMVP-6 Mobile Processor Voltage Regulation Specification* to determine the total $I_{TT}$ drawn by the system. This parameter is based on design characterization and is not tested.
10. Adherence to the voltage specifications for the processor are required to ensure reliable processor operation.

## Table 6. $V_{CC}$ Static and Transient Tolerance

| $I_{CC}$ (A) | Voltage Deviation from VID Setting (V)[1, 2, 3, 4] 5.80 mΩ | | |
|---|---|---|---|
| | Maximum Voltage | Typical Voltage | Minimum Voltage |
| 0 | 0.050 | 0.000 | -0.050 |
| 2 | 0.038 | -0.012 | -0.062 |
| 4 | 0.027 | -0.023 | -0.073 |
| 6 | 0.015 | -0.035 | -0.085 |
| 8 | 0.004 | -0.046 | -0.096 |
| 10 | -0.008 | -0.058 | -0.108 |
| 12 | -0.020 | -0.070 | -0.120 |
| 14 | -0.031 | -0.081 | -0.131 |
| 16 | -0.043 | -0.093 | -0.143 |
| 18 | -0.054 | 0.104 | -0.154 |
| 20 | -0.066 | -0.116 | -0.166 |
| 22 | -0.078 | -0.128 | -0.178 |
| 24 | -0.089 | -0.139 | -0.189 |

**NOTES:**
1. The loadline specification includes both static and transient limits except for overshoot allowed as shown in Section 3.7.3.
2. This table is intended to aid in reading discrete points on Figure 2.
3. The loadlines specify voltage limits at the die measured at the VCC_SENSE and VSS_SENSE pins. Voltage regulation feedback for voltage regulator circuits must be taken from processor VCC and VSS pins. Refer to the *Intel(R) IMVP-6 Mobile Processor Voltage Regulation Specification* for socket loadline guidelines and VR implementation details.
4. Adherence to this loadline specification is required to ensure reliable processor operation.

## Figure 2. $V_{CC}$ Static and Transient Tolerance




**NOTES:**
1. The loadline specification includes both static and transient limits except for overshoot allowed as shown in Section 3.7.3.
2. This loadline specification shows the deviation from the VID set point.

The loadlines specify voltage limits at the die measured at the VCC_SENSE and VSS_SENSE pins. Voltage regulation feedback for voltage regulator circuits must be taken from processor VCC and VSS pins. Refer to the *Intel(R) IMVP-6 Mobile Processor Voltage Regulation Specification* for socket loadline guidelines and VR implementation details.

### 3.7.3 $V_{CC}$ Overshoot

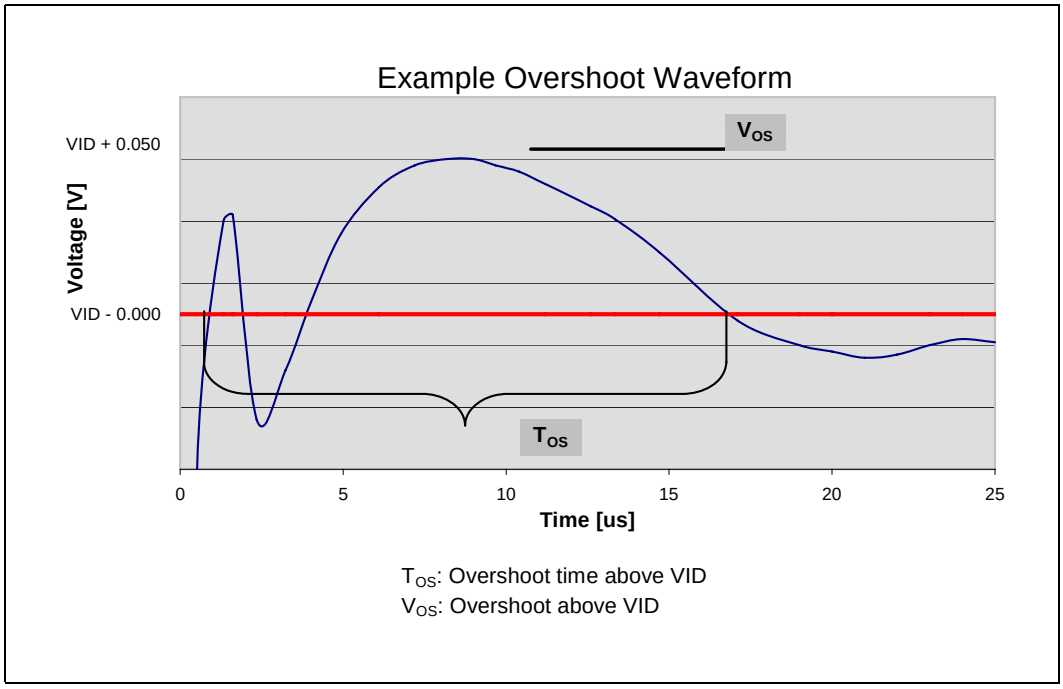
The processor can tolerate short transient overshoot events where $V_{CC}$ exceeds the VID voltage when transitioning from a high to low current load condition. This overshoot cannot exceed VID + $V_{OS\_MAX}$ ($V_{OS\_MAX}$ is the maximum allowable overshoot voltage). The time duration of the overshoot event must not exceed $T_{OS\_MAX}$ ($T_{OS\_MAX}$ is the maximum allowable time duration above VID). These specifications apply to the processor die voltage as measured across the VCC_SENSE and VSS_SENSE pins.

**Table 7. $V_{CC}$ Overshoot Specifications**

| Symbol | Parameter | Min | Max | Unit | Figure | Notes |
|---|---|---|---|---|---|---|
| $V_{OS\_MAX}$ | Magnitude of $V_{CC}$ overshoot above VID | — | 50 | mV | 3 | 1 |
| $T_{OS\_MAX}$ | Time duration of $V_{CC}$ overshoot above VID | — | 25 | µs | 3 | 1 |

**NOTES:**
1. Adherence to these specifications is required to ensure reliable processor operation.

**Figure 3. $V_{CC}$ Overshoot Example Waveform**




**NOTES:**
1. $V_{OS}$ is measured overshoot voltage.
2. $T_{OS}$ is measured time duration above VID.

### 3.7.4 Die Voltage Validation

Overshoot events on processor must meet the specifications in Table 7 when measured across the VCC_SENSE and VSS_SENSE pins. Overshoot events that are < 10 ns in duration may be ignored. These measurements of processor die level overshoot must be taken with a bandwidth limited oscilloscope set to a greater than or equal to 100 MHz bandwidth limit.

## 3.8 Signaling Specifications

Most processor Front Side Bus signals use Gunning Transceiver Logic (GTL+) signaling technology. This technology provides improved noise margins and reduced ringing through low voltage swings and controlled edge rates. Platforms implement a termination voltage level for GTL+ signals defined as $V_{CCP}$. Because platforms implement separate power planes for each processor (and chipset), separate $V_{CC}$ and $V_{CCP}$ supplies are necessary. This configuration allows for improved noise tolerance as processor frequency increases. Speed enhancements to data and address busses have caused signal integrity considerations and platform design methods to become even more critical than with previous processor families.

The GTL+ inputs require a reference voltage (GTLREF) which is used by the receivers to determine if a signal is a logical 0 or a logical 1. GTLREF must be generated on the motherboard (see Table 14 for GTLREF specifications). Termination resistors ($R_{TT}$) for GTL+ signals are provided on the processor silicon and are terminated to $V_{CCP}$. Intel chipsets will also provide on-die termination; thus, eliminating the need to terminate the bus on the motherboard for most GTL+ signals.

### 3.8.1 FSB Signal Groups

The front side bus signals have been combined into groups by buffer type. GTL+ input signals have differential input buffers, which use GTLREF[1:0] as a reference level. In this document, the term “GTL+ Input” refers to the GTL+ input group as well as the GTL+ I/O group when receiving. Similarly, “GTL+ Output” refers to the GTL+ output group as well as the GTL+ I/O group when driving.

With the implementation of a source synchronous data bus comes the need to specify two sets of timing parameters. One set is for common clock signals which are dependent upon the rising edge of BCLK0 (ADS#, HIT#, HITM#, etc.) and the second set is for the source synchronous signals which are relative to their respective strobe lines (data and address) as well as the rising edge of BCLK0.

Asychronous signals are still present (A20M#, IGNNE#, etc.) and can become active at any time during the clock cycle. Table 8 identifies which signals are common clock, source synchronous, and asynchronous.

## Table 8. FSB Pin Groups

| Signal Group | Type | Signals[1] |
|---|---|---|
| GTL+ Common Clock Input | Synchronous to BCLK[1:0] | BPRI#, DEFER#, PREQ#[5], RESET#, RS[2:0]#, DPWR#, TRDY# |
| GTL+ Common Clock I/O | Synchronous to BCLK[1:0] | ADS#, BNR#, BPM[3:0]#[3], BR0#, DBSY#, DRDY#, HIT#, HITM#, LOCK#, PRDY#[3] |
| GTL+ Source Synchronous I/O | Synchronous to Associated Strobe | **Signals** / **Associated Strobe**<br>REQ[4:0]#, A[16:3]# / ADSTB[0]#<br>A[35:17]#[6] / ADSTB[1]#<br>D[15:0]#, DINV0# / DSTBP0#, DSTBN0#<br>D[31:16]#, DINV1# / DSTBP1#, DSTBN1#<br>D[47:32]#, DINV2# / DSTBP2#, DSTBN2#<br>D[63:48]#, DINV3# / DSTBP3#, DSTBN3# |
| GTL+ Strobes | Synchronous to BCLK[1:0] | ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]# |
| CMOS Input | Asynchronous | A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, SLP#, STPCLK# |
| Open Drain Output | Asynchronous | FERR#, IERR#, THERMTRIP# |
| Open Drain I/O | Asynchronous | PROCHOT#[4] |
| CMOS Output | Asynchronous | PSI#, VID[6:0], BSEL[2:0] |
| CMOS Input | Synchronous to TCK | TCK, TDI, TMS, TRST# |
| Open Drain Output | Synchronous to TCK | TDO |
| FSB Clock | Clock | BCLK[1:0] |
| Power/Other | | COMP[3:0], DBR#[2], GTLREF, RSVD, TEST2, TEST1, THERMDA, THERMDC, VCC, VCCA, VCCP, VCC_SENSE, VSS, VSS_SENSE |

**NOTES:**
1. Refer to Chapter 4 for signal descriptions and termination requirements.
2. In processor systems where there is no debug port implemented on the system board, these signals are used to support a debug port interposer. In systems with the debug port implemented on the system board, these signals are no connects.
3. BPM[2:1]# and PRDY# are GTL+ output only signals.
4. PROCHOT# signal type is open drain output and CMOS input.
5. On die termination differs from other GTL+ signals.
6. When paired with a chipset limited to 32-bit addressing, A[35:32] should remain unconnected.

**Table 9. Signal Characteristics**

| Signals with $R_{TT}$ | Signals with No $R_{TT}$ |
|---|---|
| A[35:3]#, ADS#, ADSTB[1:0]#, BNR#, BPRI#, D[63:0]#, DBI[3:0]#, DBSY#, DEFER#, DRDY#, DSTBN[3:0]#, DSTBP[3:0]#, HIT#, HITM#, LOCK#, PROCHOT#, REQ[4:0]#, RS[2:0]#, TRDY# | A20M#, BCLK[1:0], BSEL[2:0], COMP[8,3:0], IGNNE#, INIT#, ITP_CLK[1:0], LINT0/INTR, LINT1/NMI, PWRGOOD, RESET#, SMI#, STPCLK#, TESTHI[13:0], VID[6:0], GTLREF[1:0], TCK, TDI, TMS, TRST# |
| **Open Drain Signals[1]** | |
| THERMTRIP#, FERR#/PBE#, IERR#, BPM[5:0]#, BR0#, TDO, FCx | |

**NOTES:**
1. Signals that do not have $R_{TT}$, nor are actively driven to their high-voltage level.

**Table 10. Signal Reference Voltages**

| GTLREF | $V_{CCP}/2$ |
|---|---|
| BPM[5:0]#, RESET#, BNR#, HIT#, HITM#, BR0#, A[35:0]#, ADS#, ADSTB[1:0]#, BPRI#, D[63:0]#, DBI[3:0]#, DBSY#, DEFER#, DRDY#, DSTBN[3:0]#, DSTBP[3:0]#, LOCK#, REQ[4:0]#, RS[2:0]#, TRDY# | A20M#, LINT0/INTR, LINT1/NMI, IGNNE#, INIT#, PROCHOT#, PWRGOOD[1], SMI#, STPCLK#, TCK[1], TDI[1], TMS[1], TRST#[1] |

**NOTE:**
1. These signals also have hysteresis added to the reference voltage. See Table 12 for more information.

## 3.8.2 CMOS and Open Drain Signals

Legacy input signals such as A20M#, IGNNE#, INIT#, SMI#, and STPCLK# use CMOS input buffers. All of the CMOS and Open Drain signals are required to be asserted/de-asserted for at least four BCLKs for the processor to recognize the proper signal state. See Section 3.8.3 for the DC specifications. See Section 2.2 for additional timing requirements for entering and leaving the low power states.

## 3.8.3 Processor DC Specifications

The processor DC specifications in this section are defined at the processor core (pads), unless otherwise stated. All specifications apply to all frequencies and cache sizes unless otherwise stated.

### Table 11. GTL+ Signal Group DC Specifications

| Symbol | Parameter | Min | Max | Unit | Notes[1] |
|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | -0.10 | GTLREF – 0.10 | V | 2, 5 |
| $V_{IH}$ | Input High Voltage | GTLREF + 0.10 | $V_{CCP}$ + 0.10 | V | 3, 4, 5 |
| $V_{OH}$ | Output High Voltage | $V_{CCP}$ – 0.10 | $V_{CCP}$ | V | 4, 5 |
| $I_{OL}$ | Output Low Current | N/A | $V_{CCP\_MAX}$/ [($R_{TT\_MIN}$) + ($R_{ON\_MIN}$)] | A | - |
| $I_{LI}$ | Input Leakage Current | N/A | ± 100 | µA | 6 |
| $I_{LO}$ | Output Leakage Current | N/A | ± 100 | µA | 7 |
| $R_{ON}$ | Buffer On Resistance | 10 | 13 | Ω | |

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. $V_{IL}$ is defined as the voltage range at a receiving agent that will be interpreted as a logical low value.
3. $V_{IH}$ is defined as the voltage range at a receiving agent that will be interpreted as a logical high value.
4. $V_{IH}$ and $V_{OH}$ may experience excursions above $V_{CCP}$.
5. The $V_{CCP}$ referred to in these specifications is the instantaneous $V_{CCP}$.
6. Leakage to $V_{SS}$ with pin held at $V_{CCP}$.
7. Leakage to $V_{CCP}$ with pin held at 300 mV.

### Table 12. Open Drain and TAP Output Signal Group DC Specifications

| Symbol | Parameter | Min | Typ | Max | Unit | Notes[1] |
|---|---|---|---|---|---|---|
| $V_{OL}$ | Output Low Voltage | 0 | — | 0.20 | V | |
| $I_{OL}$ | Output Low Current | 16 | — | 50 | mA | 1 |
| $I_{LO}$ | Output Leakage Current | — | — | ±200 | µA | 3 |
| $C_{PAD}$ | Pad Capacitance | 1.9 | 2.2 | 2.45 | pF | 4 |

**NOTES:**
1. Measured at 0.2 V.
2. $V_{OH}$ is determined by value of the external pul-lup resistor to $V_{CCP}$.
3. For Vin between 0 V and $V_{OH}$.
4. $C_{PAD}$ includes die capacitance only. No package parasitics are included.

### Table 13. CMOS Signal Group DC Specifications

| Symbol | Parameter | Min | Max | Unit | Notes[1] |
|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | -0.10 | $V_{CCP}$ * 0.30 | V | 2, 3 |
| $V_{IH}$ | Input High Voltage | $V_{CCP}$ * 0.70 | $V_{CCP}$ + 0.10 | V | 4, 5, 3 |
| $V_{OL}$ | Output Low Voltage | -0.10 | $V_{CCP}$ * 0.10 | V | 3 |
| $V_{OH}$ | Output High Voltage | 0.90 * $V_{CCP}$ | $V_{CCP}$ + 0.10 | V | 6, 5, 3 |
| $I_{OL}$ | Output Low Current | 1.70 | 4.70 | mA | 3, 7 |
| $I_{OH}$ | Output High Current | 1.70 | 4.70 | mA | 3, 7 |
| $I_{LI}$ | Input Leakage Current | N/A | ± 100 | µA | 8 |
| $I_{LO}$ | Output Leakage Current | N/A | ± 100 | µA | 9 |

**NOTES:**
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. $V_{IL}$ is defined as the voltage range at a receiving agent that will be interpreted as a logical low value.
3. The $V_{CCP}$ referred to in these specifications refers to instantaneous $V_{CCP}$.
4. $V_{IH}$ is defined as the voltage range at a receiving agent that will be interpreted as a logical high value.
5. $V_{IH}$ and $V_{OH}$ may experience excursions above $V_{CCP}$.
6. All outputs are open drain.
7. $I_{OL}$ is measured at 0.10 * $V_{CCP}$. $I_{OH}$ is measured at 0.90 * $V_{CCP}$.
8. Leakage to $V_{SS}$ with pin held at $V_{CCP}$.
9. Leakage to $V_{CCP}$ with pin held at 300 mV

### 3.8.3.1 GTL+ Front Side Bus Specifications

In most cases, termination resistors are not required as these are integrated into the processor silicon. See Table 9 for details on which GTL+ signals do not include on-die termination.

Valid high and low levels are determined by the input buffers by comparing with a reference voltage called GTLREF. Table 14 lists the GTLREF specifications for 50 Ohm platform. The GTL+ reference voltage (GTLREF) should be generated on the system board using high precision voltage divider circuits.

### Table 14. GTL Bus Voltage Definitions

| Symbol | Parameter | Min | Typ | Max | Units | Notes[1] |
|---|---|---|---|---|---|---|
| GTLREF_PU | GTLREF pull up resistor | -1% | 1000 | +1% | Ω | |
| GTLREF_PD | GTLREF pull down resistor | -1% | 2000 | +1% | Ω | 2, 4 |
| $R_{TT}$ | Termination Resistance | 48 | 50 | 62 | Ω | 3 |
| COMP[0,2] | Termination Resistance | -1% | 27.4 | +1% | Ω | 4 |
| COMP[1,3] | Termination Resistance | -1% | 54.9 | +1% | Ω | 4 |

**NOTES:**
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. GTLREF is to be generated from $V_{CCP}$ by a voltage divider of 1% resistors (one divider for each GTLEREF pin).
3. $R_{TT}$ is the on-die termination resistance measured at $V_{CCP}$/3 of the GTL+ output driver.
4. COMP resistance must be provided on the system board with 1% resistors. COMP[3:0] resistors are tied to $V_{SS}$.

# 3.9 Clock Specifications

## 3.9.1 Front Side Bus Clock (BCLK[1:0]) and Processor Clocking

BCLK[1:0] directly controls the FSB interface speed as well as the core frequency of the processor. As in previous generation processors, the processor's core frequency is a multiple of the BCLK[1:0] frequency. The processor bus ratio multiplier will be set at its default ratio during manufacturing. Refer to Table 15 for the processor supported ratios.

The processor uses a differential clocking implementation. For more information on the processor clocking, contact your Intel Field representative.

**Table 15. Core Frequency to FSB Multiplier Configuration**

| Multiplication of System Core Frequency to FSB Frequency | Core Frequency (133 MHz BCLK/533 MHz FSB) | Notes[1, 2] |
|---|---|---|
| 1/9 | 1.20 GHz | - |
| 1/10 | 1.33 GHz | - |

**NOTES:**
1. Individual processors operate only at or below the rated frequency.
2. Listed frequencies are not necessarily committed production frequencies.

§ §

# 4 Package Mechanical Specifications and Pin Information

## 4.1 Package Mechanical Specifications

The Celeron processor 200 sequence is available in a 479-pin Micro-FCBGA package shown in Figure 4.

### 4.1.1 Processor Component Keep-Out Zones

The processor may contain components on the substrate that define component keep-out zone requirements. A thermal and mechanical solution design must not intrude into the required keep-out zones. Decoupling capacitors are typically mounted in the keep-out areas. The location and quantity of the capacitors may change but will remain within the component keep-in. See Figure 5 for keep-out zones.

### 4.1.2 Package Loading Specifications

Maximum mechanical package loading specifications are given in Figure 4. These specifications are static compressive loading in the direction normal to the processor. This maximum load limit should not be exceeded during shipping conditions, standard use condition, or by the thermal solution. In addition, there are additional load limitations against transient bend, shock, and tensile loading. These limitations are more platform specific and should be obtained by contacting your field support. Moreover, the processor package substrate should not be used as a mechanical reference or load-bearing surface for the thermal or mechanical solution.

### 4.1.3 Processor Mass Specifications

The typical mass is given in Figure 4 and Table 16. This mass includes all the components that are included in the package.

**Table 16. Micro-FCBGA Package Mechanical Specifications**

| Symbol | Parameter | Min | Max | Unit | Figure |
|---|---|---|---|---|---|
| B1 | Package substrate width | 34.95 | 35.05 | mm | Figure 4 |
| B2 | Package substrate length | 34.95 | 35.05 | mm | Figure 4 |
| C1 | Die width | 11.1 | | mm | Figure 4 |
| C2 | Die length | 8.2 | | mm | Figure 4 |
| F2 | Die height (with underfill) | 0.89 | | mm | Figure 4 |
| F3 | Package overall height (package substrate to die) | 2.022 Max | | mm | Figure 4 |
| G1 | Width (first ball center to lass ball center) | 31.75 Basic | | mm | Figure 4 |
| G2 | Length (first ball center to last ball center) | 31.75 Basic | | mm | Figure 4 |
| J1 | Ball pitch (horizontal) | 1.27 Basic | | mm | Figure 4 |
| J2 | Ball pitch (vertical) | 1.27 Basic | | mm | Figure 4 |
| M | Solder Resist Opening | 0.61 | 0.69 | mm | Figure 4 |
| N | Ball height | 0.6 | 0.8 | mm | Figure 4 |
| — | Corener Keep-out zone at corner (4X) | 7 x 7 | | mm | Figure 5 |
| — | Keep-out from edge of package (4x) | 5 | | mm | Figure 5 |
| — | Package edge to first ball center | 1.625 | | mm | Figure 5 |
| $P_{die}$ | Allowable pressure on the die for thermal solution | 689 | | kPa | |
| W | Package weight | 6 | | g | |

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**Figure 4. Micro-FCBGA Processor Package Drawing (1 of 2)**

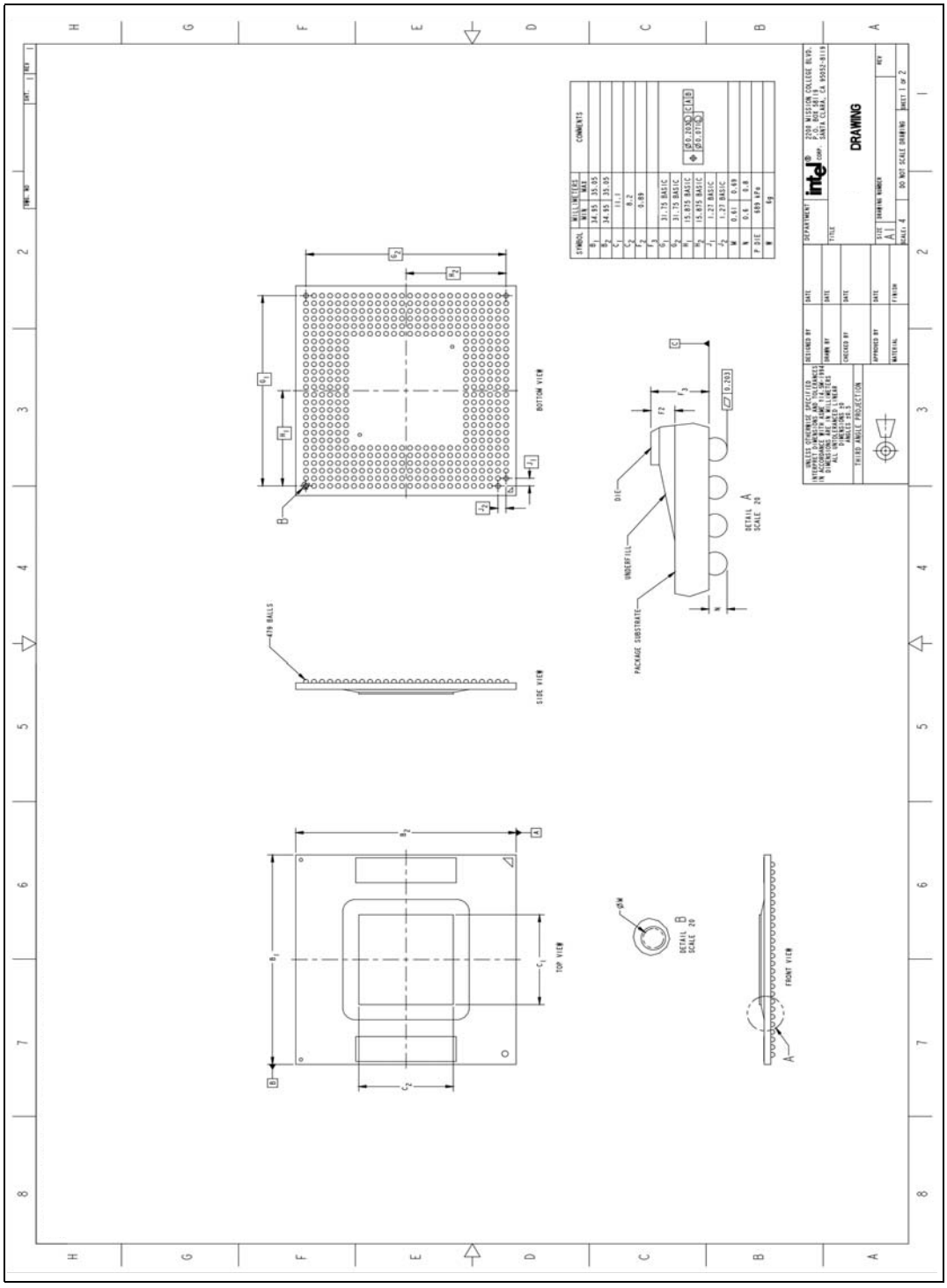
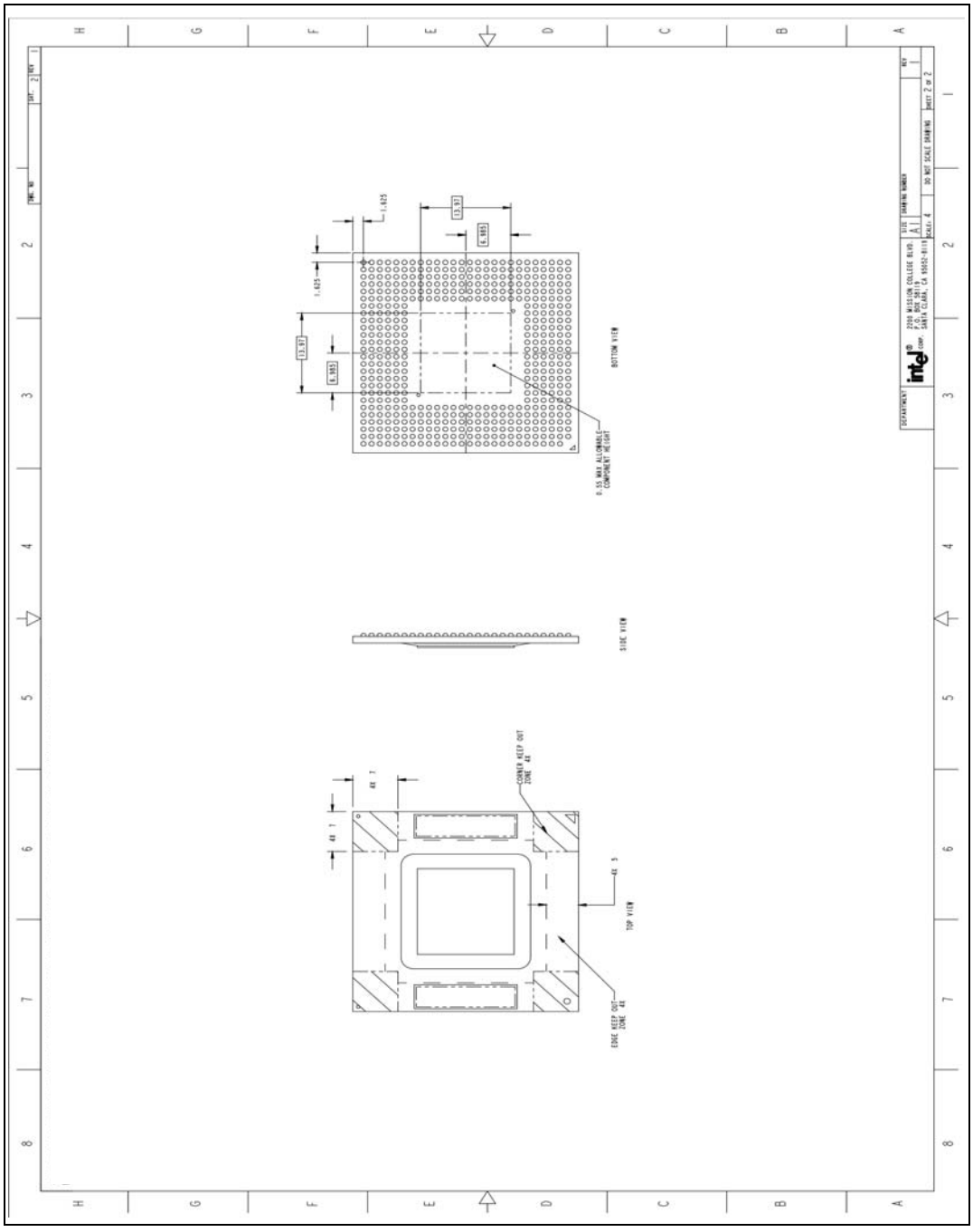


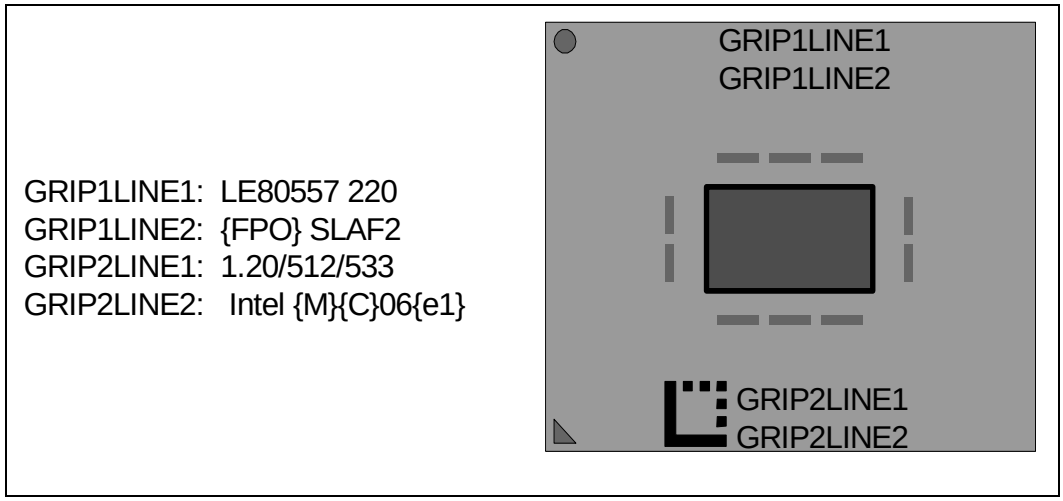
**Figure 5. Micro-FCBGA Processor Package Drawing (2 of 2)**



### 4.1.4 Processor Markings

Figure 6 shows the topside markings on the processor. This diagram is to aid in the identification of the processor.

**Figure 6. Processor Top-Side Marking Example**




## 4.2 Processor Pinout and Pin List

Figure 7 and Figure 8 show the top view pinout of the Celeron processor.

## Figure 7. Processor Pinout (Top View — Left Side)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | | VSS | SMI# | VSS | FERR# | A20M# | VCC | VSS | VCC | VCC | VSS | VCC | VCC | A |
| B | RESET# | RSVD | INIT# | LINT1 | DPSLP# | VSS | VCC | VSS | VCC | VCC | VSS | VCC | VSS | B |
| C | RSVD | VSS | RSVD | IGNNE# | VSS | LINT0 | THERMTRIP# | VSS | VCC | VCC | VSS | VCC | VCC | C |
| D | VSS | RSVD | RSVD | VSS | STPCLK# | PWRGOOD | SLP# | VSS | VCC | VCC | VSS | VCC | VSS | D |
| E | DBSY# | BNR# | VSS | HITM# | DPRSTP# | VSS | VCC | VSS | VCC | VCC | VSS | VCC | VCC | E |
| F | BR0# | VSS | RS[0]# | RS[1]# | VSS | RSVD | VCC | VSS | VCC | VCC | VSS | VCC | VSS | F |
| G | VSS | TRDY# | RS[2]# | VSS | BPRI# | HIT# | | | | | | | | G |
| H | ADS# | REQ[1]# | VSS | LOCK# | DEFER# | VSS | | | | | | | | H |
| J | A[9]# | VSS | REQ[3]# | A[3]# | VSS | VCCP | | | | | | | | J |
| K | VSS | REQ[2]# | REQ[0]# | VSS | A[6]# | VCCP | | | | | | | | K |
| L | A[13]# | ADSTB[0]# | VSS | A[4]# | REQ[4]# | VSS | | | | | | | | L |
| M | A[7]# | VSS | A[5]# | RSVD | VSS | VCCP | | | | | | | | M |
| N | VSS | A[8]# | A[10]# | VSS | RSVD | VCCP | | | | | | | | N |
| P | A[15]# | A[12]# | VSS | A[14]# | A[11]# | VSS | | | | | | | | P |
| R | A[16]# | VSS | A[19]# | A[24]# | VSS | VCCP | | | | | | | | R |
| T | VSS | RSVD | A[26]# | VSS | A[25]# | VCCP | | | | | | | | T |
| U | COMP[2] | A[23]# | VSS | A[21]# | A[18]# | VSS | | | | | | | | U |
| V | COMP[3] | VSS | RSVD | ADSTB[1]# | VSS | VCCP | | | | | | | | V |
| W | VSS | A[30]# | A[27]# | VSS | A[28]# | A[20]# | | | | | | | | W |
| Y | A[31]# | A[17]# | VSS | A[29]# | A[22]# | VSS | | | | | | | | Y |
| AA | A[32]# | VSS | A[35]# | A[33]# | VSS | TDI | VCC | VSS | VCC | VCC | VSS | VCC | VCC | AA |
| AB | VSS | A[34]# | TDO | VSS | TMS | TRST# | VCC | VSS | VCC | VCC | VSS | VCC | VSS | AB |
| AC | PREQ# | PRDY# | VSS | BPM[3]# | TCK | VSS | VCC | VSS | VCC | VCC | VSS | VCC | VCC | AC |
| AD | BPM[2]# | VSS | BPM[1]# | BPM[0]# | VSS | VID[0] | VCC | VSS | VCC | VCC | VSS | VCC | VSS | AD |
| AE | VSS | VID[6] | VID[4] | VSS | VID[2] | PSI# | VSS_SENSE | VSS | VCC | VCC | VSS | VCC | VCC | AE |
| AF | TEST3 | VID[5] | VSS | VID[3] | VID[1] | VSS | VCC_SENSE | VSS | VCC | VCC | VSS | VCC | VSS | AF |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | |

## Figure 8. Processor Pinout (Top View — Right Side)

| | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | VSS | VCC | VSS | VCC | VCC | VSS | VCC | BCLK[1] | BCLK[0] | VSS | RSVD | RSVD | VSS | A |
| B | VCC | VCC | VSS | VCC | VCC | VSS | VCC | VSS | BSEL[0] | BSEL[1] | VSS | TEST4 | VCCA | B |
| C | VSS | VCC | VSS | VCC | VCC | VSS | DBR# | BSEL[2] | VSS | RSVD | RSVD | VSS | TEST1 | C |
| D | VCC | VCC | VSS | VCC | VCC | VSS | IERR# | PROCHOT# | RSVD | VSS | DPWR# | TEST2 | VSS | D |
| E | VSS | VCC | VSS | VCC | VCC | VSS | VCC | VSS | D[0]# | D[7]# | VSS | D[6]# | D[2]# | E |
| F | VCC | VCC | VSS | VCC | VCC | VSS | VCC | DRDY# | VSS | D[4]# | D[1]# | VSS | D[13]# | F |
| G | | | | | | | | VCCP | DSTBP[0]# | VSS | D[9]# | D[5]# | VSS | G |
| H | | | | | | | | VSS | D[3]# | DSTBN[0]# | VSS | D[15]# | D[12]# | H |
| J | | | | | | | | VCCP | VSS | D[11]# | D[10]# | VSS | DINV[0]# | J |
| K | | | | | | | | VCCP | D[14]# | VSS | D[8]# | D[17]# | VSS | K |
| L | | | | | | | | VSS | D[21]# | D[22]# | VSS | D[20]# | D[29]# | L |
| M | | | | | | | | VCCP | VSS | D[23]# | DSTBN[1]# | VSS | DINV[1]# | M |
| N | | | | | | | | VCCP | D[16]# | VSS | D[31]# | DSTBP[1]# | VSS | N |
| P | | | | | | | | VSS | D[25]# | D[26]# | VSS | D[24]# | D[18]# | P |
| R | | | | | | | | VCCP | VSS | D[19]# | D[28]# | VSS | COMP [0] | R |
| T | | | | | | | | VCCP | RSVD | VSS | D[27]# | D[30]# | VSS | T |
| U | | | | | | | | VSS | D[39]# | D[37]# | VSS | D[38]# | COMP[1] | U |
| V | | | | | | | | VCCP | VSS | DINV[2]# | D[34]# | VSS | D[35]# | V |
| W | | | | | | | | VCCP | D[41]# | VSS | DSTBN[2]# | D[36]# | VSS | W |
| Y | | | | | | | | VSS | D[45]# | D[42]# | VSS | DSTBP[2]# | D[44]# | Y |
| AA | VSS | VCC | VSS | VCC | VCC | VSS | VCC | D[51]# | VSS | D[32]# | D[47]# | VSS | D[43]# | AA |
| AB | VCC | VCC | VSS | VCC | VCC | VSS | VCC | D[52]# | D[50]# | VSS | D[33]# | D[40]# | VSS | AB |
| AC | VSS | VCC | VSS | VCC | VCC | VSS | DINV[3]# | VSS | D[48]# | D[49]# | VSS | D[53]# | D[46]# | AC |
| AD | VCC | VCC | VSS | VCC | VCC | VSS | D[54]# | D[59]# | VSS | DSTBN[3]# | D[57]# | VSS | GTLREF | AD |
| AE | VSS | VCC | VSS | VCC | VCC | VSS | VCC | D[58]# | D[55]# | VSS | DSTBP[3]# | D[60]# | VSS | AE |
| AF | VCC | VCC | VSS | VCC | VCC | VSS | VCC | VSS | D[62]# | D[56]# | VSS | D[61]# | D[63]# | AF |
| | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | |

## Table 17. Pin Listing by Pin Name (Sheet 1 of 12)

| Pin Name | Pin # | Signal Buffer Type | Direction |
|---|---|---|---|
| A[3]# | J4 | Source Synch | Input/Output |
| A[4]# | L4 | Source Synch | Input/Output |
| A[5]# | M3 | Source Synch | Input/Output |
| A[6]# | K5 | Source Synch | Input/Output |
| A[7]# | M1 | Source Synch | Input/Output |
| A[8]# | N2 | Source Synch | Input/Output |
| A[9]# | J1 | Source Synch | Input/Output |
| A[10]# | N3 | Source Synch | Input/Output |
| A[11]# | P5 | Source Synch | Input/Output |
| A[12]# | P2 | Source Synch | Input/Output |
| A[13]# | L1 | Source Synch | Input/Output |
| A[14]# | P4 | Source Synch | Input/Output |
| A[15]# | P1 | Source Synch | Input/Output |
| A[16]# | R1 | Source Synch | Input/Output |
| A[17]# | Y2 | Source Synch | Input/Output |
| A[18]# | U5 | Source Synch | Input/Output |
| A[19]# | R3 | Source Synch | Input/Output |
| A[20]# | W6 | Source Synch | Input/Output |
| A[21]# | U4 | Source Synch | Input/Output |
| A[22]# | Y5 | Source Synch | Input/Output |
| A[23]# | U2 | Source Synch | Input/Output |
| A[24]# | R4 | Source Synch | Input/Output |
| A[25]# | T5 | Source Synch | Input/Output |
| A[26]# | T3 | Source Synch | Input/Output |
| A[27]# | W3 | Source Synch | Input/Output |
| A[28]# | W5 | Source Synch | Input/Output |
| A[29]# | Y4 | Source Synch | Input/Output |
| A[30]# | W2 | Source Synch | Input/Output |
| A[31]# | Y1 | Source Synch | Input/Output |
| A[32]# | AA1 | Source Synch | Input/Output |
| A[33]# | AA4 | Source Synch | Input/Output |
| A[34]# | AB2 | Source Synch | Input/Output |
| A[35]# | AA3 | Source Synch | Input/Output |
| A20M# | A6 | CMOS | Input |
| ADS# | H1 | Common Clock | Input/Output |
| ADSTB[0]# | L2 | Source Synch | Input/Output |
| ADSTB[1]# | V4 | Source Synch | Input/Output |
| BCLK[0] | A22 | Bus Clock | Input |
| BCLK[1] | A21 | Bus Clock | Input |
| BNR# | E2 | Common Clock | Input/Output |
| BPM[0]# | AD4 | Common Clock | Input/Output |
| BPM[1]# | AD3 | Common Clock | Output |

## Table 17. Pin Listing by Pin Name (Sheet 2 of 12)

| Pin Name | Pin # | Signal Buffer Type | Direction |
|---|---|---|---|
| BPM[2]# | AD1 | Common Clock | Output |
| BPM[3]# | AC4 | Common Clock | Input/Output |
| BPRI# | G5 | Common Clock | Input |
| BR0# | F1 | Common Clock | Input/Output |
| BSEL[0] | B22 | CMOS | Output |
| BSEL[1] | B23 | CMOS | Output |
| BSEL[2] | C21 | CMOS | Output |
| COMP[0] | R26 | Power/Other | Input/Output |
| COMP[1] | U26 | Power/Other | Input/Output |
| COMP[2] | U1 | Power/Other | Input/Output |
| COMP[3] | V1 | Power/Other | Input/Output |
| D[0]# | E22 | Source Synch | Input/Output |
| D[1]# | F24 | Source Synch | Input/Output |
| D[2]# | E26 | Source Synch | Input/Output |
| D[3]# | H22 | Source Synch | Input/Output |
| D[4]# | F23 | Source Synch | Input/Output |
| D[5]# | G25 | Source Synch | Input/Output |
| D[6]# | E25 | Source Synch | Input/Output |
| D[7]# | E23 | Source Synch | Input/Output |
| D[8]# | K24 | Source Synch | Input/Output |
| D[9]# | G24 | Source Synch | Input/Output |
| D[10]# | J24 | Source Synch | Input/Output |
| D[11]# | J23 | Source Synch | Input/Output |
| D[12]# | H26 | Source Synch | Input/Output |
| D[13]# | F26 | Source Synch | Input/Output |
| D[14]# | K22 | Source Synch | Input/Output |
| D[15]# | H25 | Source Synch | Input/Output |
| D[16]# | N22 | Source Synch | Input/Output |
| D[17]# | K25 | Source Synch | Input/Output |
| D[18]# | P26 | Source Synch | Input/Output |
| D[19]# | R23 | Source Synch | Input/Output |
| D[20]# | L25 | Source Synch | Input/Output |
| D[21]# | L22 | Source Synch | Input/Output |
| D[22]# | L23 | Source Synch | Input/Output |
| D[23]# | M23 | Source Synch | Input/Output |
| D[24]# | P25 | Source Synch | Input/Output |
| D[25]# | P22 | Source Synch | Input/Output |
| D[26]# | P23 | Source Synch | Input/Output |
| D[27]# | T24 | Source Synch | Input/Output |
| D[28]# | R24 | Source Synch | Input/Output |
| D[29]# | L26 | Source Synch | Input/Output |
| D[30]# | T25 | Source Synch | Input/Output |

**Table 17. Pin Listing by Pin Name (Sheet 3 of 12)**

| Pin Name | Pin # | Signal Buffer Type | Direction |
|---|---|---|---|
| D[31]# | N24 | Source Synch | Input/Output |
| D[32]# | AA23 | Source Synch | Input/Output |
| D[33]# | AB24 | Source Synch | Input/Output |
| D[34]# | V24 | Source Synch | Input/Output |
| D[35]# | V26 | Source Synch | Input/Output |
| D[36]# | W25 | Source Synch | Input/Output |
| D[37]# | U23 | Source Synch | Input/Output |
| D[38]# | U25 | Source Synch | Input/Output |
| D[39]# | U22 | Source Synch | Input/Output |
| D[40]# | AB25 | Source Synch | Input/Output |
| D[41]# | W22 | Source Synch | Input/Output |
| D[42]# | Y23 | Source Synch | Input/Output |
| D[43]# | AA26 | Source Synch | Input/Output |
| D[44]# | Y26 | Source Synch | Input/Output |
| D[45]# | Y22 | Source Synch | Input/Output |
| D[46]# | AC26 | Source Synch | Input/Output |
| D[47]# | AA24 | Source Synch | Input/Output |
| D[48]# | AC22 | Source Synch | Input/Output |
| D[49]# | AC23 | Source Synch | Input/Output |
| D[50]# | AB22 | Source Synch | Input/Output |
| D[51]# | AA21 | Source Synch | Input/Output |
| D[52]# | AB21 | Source Synch | Input/Output |
| D[53]# | AC25 | Source Synch | Input/Output |
| D[54]# | AD20 | Source Synch | Input/Output |
| D[55]# | AE22 | Source Synch | Input/Output |
| D[56]# | AF23 | Source Synch | Input/Output |
| D[57]# | AD24 | Source Synch | Input/Output |
| D[58]# | AE21 | Source Synch | Input/Output |
| D[59]# | AD21 | Source Synch | Input/Output |
| D[60]# | AE25 | Source Synch | Input/Output |
| D[61]# | AF25 | Source Synch | Input/Output |
| D[62]# | AF22 | Source Synch | Input/Output |
| D[63]# | AF26 | Source Synch | Input/Output |
| DBR# | C20 | CMOS | Output |
| DBSY# | E1 | Common Clock | Input/Output |
| DEFER# | H5 | Common Clock | Input |
| DINV[0]# | J26 | Source Synch | Input/Output |
| DINV[1]# | M26 | Source Synch | Input/Output |
| DINV[2]# | V23 | Source Synch | Input/Output |
| DINV[3]# | AC20 | Source Synch | Input/Output |
| DPRSTP# | E5 | CMOS | Input |
| DPSLP# | B5 | CMOS | Input |

**Table 17. Pin Listing by Pin Name (Sheet 4 of 12)**

| Pin Name | Pin # | Signal Buffer Type | Direction |
|---|---|---|---|
| DPWR# | D24 | Common Clock | Input |
| DRDY# | F21 | Common Clock | Input/Output |
| DSTBN[0]# | H23 | Source Synch | Input/Output |
| DSTBN[1]# | M24 | Source Synch | Input/Output |
| DSTBN[2]# | W24 | Source Synch | Input/Output |
| DSTBN[3]# | AD23 | Source Synch | Input/Output |
| DSTBP[0]# | G22 | Source Synch | Input/Output |
| DSTBP[1]# | N25 | Source Synch | Input/Output |
| DSTBP[2]# | Y25 | Source Synch | Input/Output |
| DSTBP[3]# | AE24 | Source Synch | Input/Output |
| FERR# | A5 | Open Drain | Output |
| GTLREF | AD26 | Power/Other | Input |
| HIT# | G6 | Common Clock | Input/Output |
| HITM# | E4 | Common Clock | Input/Output |
| IERR# | D20 | Open Drain | Output |
| IGNNE# | C4 | CMOS | Input |
| INIT# | B3 | CMOS | Input |
| LINT0 | C6 | CMOS | Input |
| LINT1 | B4 | CMOS | Input |
| LOCK# | H4 | Common Clock | Input/Output |
| PRDY# | AC2 | Common Clock | Output |
| PREQ# | AC1 | Common Clock | Input |
| PROCHOT# | D21 | Open Drain | Input/Output |
| PSI# | AE6 | CMOS | Output |
| PWRGOOD | D6 | CMOS | Input |
| REQ[0]# | K3 | Source Synch | Input/Output |
| REQ[1]# | H2 | Source Synch | Input/Output |
| REQ[2]# | K2 | Source Synch | Input/Output |
| REQ[3]# | J3 | Source Synch | Input/Output |
| REQ[4]# | L5 | Source Synch | Input/Output |
| RESET# | B1 | Common Clock | Input |
| RS[0]# | F3 | Common Clock | Input |
| RS[1]# | F4 | Common Clock | Input |
| RS[2]# | G3 | Common Clock | Input |
| RSVD | B2 | Reserved | |
| RSVD | C1 | Reserved | |
| RSVD | C23 | Reserved | |
| RSVD | C24 | Reserved | |
| RSVD | C3 | Reserved | |
| RSVD | D2 | Reserved | |
| RSVD | D22 | Reserved | |
| RSVD | D3 | Reserved | |

**Table 17. Pin Listing by Pin Name (Sheet 5 of 12)**

| Pin Name | Pin # | Signal Buffer Type | Direction |
|---|---|---|---|
| RSVD | F6 | Reserved | |
| RSVD | M4 | Reserved | |
| RSVD | N5 | Reserved | |
| RSVD | T2 | Reserved | |
| RSVD | T22 | Reserved | |
| RSVD | V3 | Reserved | |
| SLP# | D7 | CMOS | Input |
| SMI# | A3 | CMOS | Input |
| STPCLK# | D5 | CMOS | Input |
| TCK | AC5 | CMOS | Input |
| TDI | AA6 | CMOS | Input |
| TDO | AB3 | Open Drain | Output |
| TEST1 | C26 | Test | |
| TEST2 | D25 | Test | |
| TEST3 | AF1 | Test | |
| TEST4 | B25 | Test | |
| THERMDA | A24 | Power/Other | |
| THERMDC | A25 | Power/Other | |
| THERMTRIP# | C7 | Open Drain | Output |
| TMS | AB5 | CMOS | Input |
| TRDY# | G2 | Common Clock | Input |
| TRST# | AB6 | CMOS | Input |
| VCC | A10 | Power/Other | |
| VCC | A12 | Power/Other | |
| VCC | A13 | Power/Other | |
| VCC | A15 | Power/Other | |
| VCC | A17 | Power/Other | |
| VCC | A18 | Power/Other | |
| VCC | A20 | Power/Other | |
| VCC | A7 | Power/Other | |
| VCC | A9 | Power/Other | |
| VCC | AA10 | Power/Other | |
| VCC | AA12 | Power/Other | |
| VCC | AA13 | Power/Other | |
| VCC | AA15 | Power/Other | |
| VCC | AA17 | Power/Other | |
| VCC | AA18 | Power/Other | |
| VCC | AA20 | Power/Other | |
| VCC | AA7 | Power/Other | |
| VCC | AA9 | Power/Other | |
| VCC | AB10 | Power/Other | |
| VCC | AB12 | Power/Other | |

**Table 17. Pin Listing by Pin Name (Sheet 6 of 12)**

| Pin Name | Pin # | Signal Buffer Type | Direction |
|---|---|---|---|
| VCC | AB14 | Power/Other | |
| VCC | AB15 | Power/Other | |
| VCC | AB17 | Power/Other | |
| VCC | AB18 | Power/Other | |
| VCC | AB20 | Power/Other | |
| VCC | AB7 | Power/Other | |
| VCC | AB9 | Power/Other | |
| VCC | AC10 | Power/Other | |
| VCC | AC12 | Power/Other | |
| VCC | AC13 | Power/Other | |
| VCC | AC15 | Power/Other | |
| VCC | AC17 | Power/Other | |
| VCC | AC18 | Power/Other | |
| VCC | AC7 | Power/Other | |
| VCC | AC9 | Power/Other | |
| VCC | AD10 | Power/Other | |
| VCC | AD12 | Power/Other | |
| VCC | AD14 | Power/Other | |
| VCC | AD15 | Power/Other | |
| VCC | AD17 | Power/Other | |
| VCC | AD18 | Power/Other | |
| VCC | AD7 | Power/Other | |
| VCC | AD9 | Power/Other | |
| VCC | AE10 | Power/Other | |
| VCC | AE12 | Power/Other | |
| VCC | AE13 | Power/Other | |
| VCC | AE15 | Power/Other | |
| VCC | AE17 | Power/Other | |
| VCC | AE18 | Power/Other | |
| VCC | AE20 | Power/Other | |
| VCC | AE9 | Power/Other | |
| VCC | AF10 | Power/Other | |
| VCC | AF12 | Power/Other | |
| VCC | AF14 | Power/Other | |
| VCC | AF15 | Power/Other | |
| VCC | AF17 | Power/Other | |
| VCC | AF18 | Power/Other | |
| VCC | AF20 | Power/Other | |
| VCC | AF9 | Power/Other | |
| VCC | B10 | Power/Other | |
| VCC | B12 | Power/Other | |
| VCC | B14 | Power/Other | |

**Table 17. Pin Listing by Pin Name (Sheet 7 of 12)**

| Pin Name | Pin # | Signal Buffer Type | Direction |
|---|---|---|---|
| VCC | B15 | Power/Other | |
| VCC | B17 | Power/Other | |
| VCC | B18 | Power/Other | |
| VCC | B20 | Power/Other | |
| VCC | B7 | Power/Other | |
| VCC | B9 | Power/Other | |
| VCC | C10 | Power/Other | |
| VCC | C12 | Power/Other | |
| VCC | C13 | Power/Other | |
| VCC | C15 | Power/Other | |
| VCC | C17 | Power/Other | |
| VCC | C18 | Power/Other | |
| VCC | C9 | Power/Other | |
| VCC | D10 | Power/Other | |
| VCC | D12 | Power/Other | |
| VCC | D14 | Power/Other | |
| VCC | D15 | Power/Other | |
| VCC | D17 | Power/Other | |
| VCC | D18 | Power/Other | |
| VCC | D9 | Power/Other | |
| VCC | E10 | Power/Other | |
| VCC | E12 | Power/Other | |
| VCC | E13 | Power/Other | |
| VCC | E15 | Power/Other | |
| VCC | E17 | Power/Other | |
| VCC | E18 | Power/Other | |
| VCC | E20 | Power/Other | |
| VCC | E7 | Power/Other | |
| VCC | E9 | Power/Other | |
| VCC | F10 | Power/Other | |
| VCC | F12 | Power/Other | |
| VCC | F14 | Power/Other | |
| VCC | F15 | Power/Other | |
| VCC | F17 | Power/Other | |
| VCC | F18 | Power/Other | |
| VCC | F20 | Power/Other | |
| VCC | F7 | Power/Other | |
| VCC | F9 | Power/Other | |
| VCCA | B26 | Power/Other | |
| VCCP | G21 | Power/Other | |
| VCCP | J21 | Power/Other | |
| VCCP | J6 | Power/Other | |

**Table 17. Pin Listing by Pin Name (Sheet 8 of 12)**

| Pin Name | Pin # | Signal Buffer Type | Direction |
|---|---|---|---|
| VCCP | K21 | Power/Other | |
| VCCP | K6 | Power/Other | |
| VCCP | M21 | Power/Other | |
| VCCP | M6 | Power/Other | |
| VCCP | N21 | Power/Other | |
| VCCP | N6 | Power/Other | |
| VCCP | R21 | Power/Other | |
| VCCP | R6 | Power/Other | |
| VCCP | T21 | Power/Other | |
| VCCP | T6 | Power/Other | |
| VCCP | V21 | Power/Other | |
| VCCP | V6 | Power/Other | |
| VCCP | W21 | Power/Other | |
| VCC_SENSE | AF7 | Power/Other | |
| VID[0] | AD6 | CMOS | Output |
| VID[1] | AF5 | CMOS | Output |
| VID[2] | AE5 | CMOS | Output |
| VID[3] | AF4 | CMOS | Output |
| VID[4] | AE3 | CMOS | Output |
| VID[5] | AF2 | CMOS | Output |
| VID[6] | AE2 | CMOS | Output |
| VSS | A11 | Power/Other | |
| VSS | A14 | Power/Other | |
| VSS | A16 | Power/Other | |
| VSS | A19 | Power/Other | |
| VSS | A2 | Power/Other | |
| VSS | A23 | Power/Other | |
| VSS | A26 | Power/Other | |
| VSS | A4 | Power/Other | |
| VSS | A8 | Power/Other | |
| VSS | AA11 | Power/Other | |
| VSS | AA14 | Power/Other | |
| VSS | AA16 | Power/Other | |
| VSS | AA19 | Power/Other | |
| VSS | AA2 | Power/Other | |
| VSS | AA22 | Power/Other | |
| VSS | AA25 | Power/Other | |
| VSS | AA5 | Power/Other | |
| VSS | AA8 | Power/Other | |
| VSS | AB1 | Power/Other | |
| VSS | AB11 | Power/Other | |
| VSS | AB13 | Power/Other | |

**Table 17. Pin Listing by Pin Name (Sheet 9 of 12)**

| Pin Name | Pin # | Signal Buffer Type | Direction |
|---|---|---|---|
| VSS | AB16 | Power/Other | |
| VSS | AB19 | Power/Other | |
| VSS | AB23 | Power/Other | |
| VSS | AB26 | Power/Other | |
| VSS | AB4 | Power/Other | |
| VSS | AB8 | Power/Other | |
| VSS | AC11 | Power/Other | |
| VSS | AC14 | Power/Other | |
| VSS | AC16 | Power/Other | |
| VSS | AC19 | Power/Other | |
| VSS | AC21 | Power/Other | |
| VSS | AC24 | Power/Other | |
| VSS | AC3 | Power/Other | |
| VSS | AC6 | Power/Other | |
| VSS | AC8 | Power/Other | |
| VSS | AD11 | Power/Other | |
| VSS | AD13 | Power/Other | |
| VSS | AD16 | Power/Other | |
| VSS | AD19 | Power/Other | |
| VSS | AD2 | Power/Other | |
| VSS | AD22 | Power/Other | |
| VSS | AD25 | Power/Other | |
| VSS | AD5 | Power/Other | |
| VSS | AD8 | Power/Other | |
| VSS | AE1 | Power/Other | |
| VSS | AE11 | Power/Other | |
| VSS | AE14 | Power/Other | |
| VSS | AE16 | Power/Other | |
| VSS | AE19 | Power/Other | |
| VSS | AE23 | Power/Other | |
| VSS | AE26 | Power/Other | |
| VSS | AE4 | Power/Other | |
| VSS | AE8 | Power/Other | |
| VSS | AF11 | Power/Other | |
| VSS | AF13 | Power/Other | |
| VSS | AF16 | Power/Other | |
| VSS | AF19 | Power/Other | |
| VSS | AF21 | Power/Other | |
| VSS | AF24 | Power/Other | |
| VSS | AF3 | Power/Other | |
| VSS | AF6 | Power/Other | |
| VSS | AF8 | Power/Other | |

**Table 17. Pin Listing by Pin Name (Sheet 10 of 12)**

| Pin Name | Pin # | Signal Buffer Type | Direction |
|---|---|---|---|
| VSS | B11 | Power/Other | |
| VSS | B13 | Power/Other | |
| VSS | B16 | Power/Other | |
| VSS | B19 | Power/Other | |
| VSS | B21 | Power/Other | |
| VSS | B24 | Power/Other | |
| VSS | B6 | Power/Other | |
| VSS | B8 | Power/Other | |
| VSS | C11 | Power/Other | |
| VSS | C14 | Power/Other | |
| VSS | C16 | Power/Other | |
| VSS | C19 | Power/Other | |
| VSS | C2 | Power/Other | |
| VSS | C22 | Power/Other | |
| VSS | C25 | Power/Other | |
| VSS | C5 | Power/Other | |
| VSS | C8 | Power/Other | |
| VSS | D1 | Power/Other | |
| VSS | D11 | Power/Other | |
| VSS | D13 | Power/Other | |
| VSS | D16 | Power/Other | |
| VSS | D19 | Power/Other | |
| VSS | D23 | Power/Other | |
| VSS | D26 | Power/Other | |
| VSS | D4 | Power/Other | |
| VSS | D8 | Power/Other | |
| VSS | E11 | Power/Other | |
| VSS | E14 | Power/Other | |
| VSS | E16 | Power/Other | |
| VSS | E19 | Power/Other | |
| VSS | E21 | Power/Other | |
| VSS | E24 | Power/Other | |
| VSS | E3 | Power/Other | |
| VSS | E6 | Power/Other | |
| VSS | E8 | Power/Other | |
| VSS | F11 | Power/Other | |
| VSS | F13 | Power/Other | |
| VSS | F16 | Power/Other | |
| VSS | F19 | Power/Other | |
| VSS | F2 | Power/Other | |
| VSS | F22 | Power/Other | |
| VSS | F25 | Power/Other | |

**Table 17. Pin Listing by Pin Name (Sheet 11 of 12)**

| Pin Name | Pin # | Signal Buffer Type | Direction |
|---|---|---|---|
| VSS | F5 | Power/Other | |
| VSS | F8 | Power/Other | |
| VSS | G1 | Power/Other | |
| VSS | G23 | Power/Other | |
| VSS | G26 | Power/Other | |
| VSS | G4 | Power/Other | |
| VSS | H21 | Power/Other | |
| VSS | H24 | Power/Other | |
| VSS | H3 | Power/Other | |
| VSS | H6 | Power/Other | |
| VSS | J2 | Power/Other | |
| VSS | J22 | Power/Other | |
| VSS | J25 | Power/Other | |
| VSS | J5 | Power/Other | |
| VSS | K1 | Power/Other | |
| VSS | K23 | Power/Other | |
| VSS | K26 | Power/Other | |
| VSS | K4 | Power/Other | |
| VSS | L21 | Power/Other | |
| VSS | L24 | Power/Other | |
| VSS | L3 | Power/Other | |
| VSS | L6 | Power/Other | |
| VSS | M2 | Power/Other | |
| VSS | M22 | Power/Other | |
| VSS | M25 | Power/Other | |
| VSS | M5 | Power/Other | |
| VSS | N1 | Power/Other | |
| VSS | N23 | Power/Other | |
| VSS | N26 | Power/Other | |
| VSS | N4 | Power/Other | |
| VSS | P21 | Power/Other | |
| VSS | P24 | Power/Other | |
| VSS | P3 | Power/Other | |
| VSS | P6 | Power/Other | |
| VSS | R2 | Power/Other | |
| VSS | R22 | Power/Other | |
| VSS | R25 | Power/Other | |
| VSS | R5 | Power/Other | |
| VSS | T1 | Power/Other | |
| VSS | T23 | Power/Other | |
| VSS | T26 | Power/Other | |
| VSS | T4 | Power/Other | |

**Table 17. Pin Listing by Pin Name (Sheet 12 of 12)**

| Pin Name | Pin # | Signal Buffer Type | Direction |
|---|---|---|---|
| VSS | U21 | Power/Other | |
| VSS | U24 | Power/Other | |
| VSS | U3 | Power/Other | |
| VSS | U6 | Power/Other | |
| VSS | V2 | Power/Other | |
| VSS | V22 | Power/Other | |
| VSS | V25 | Power/Other | |
| VSS | V5 | Power/Other | |
| VSS | W1 | Power/Other | |
| VSS | W23 | Power/Other | |
| VSS | W26 | Power/Other | |
| VSS | W4 | Power/Other | |
| VSS | Y21 | Power/Other | |
| VSS | Y24 | Power/Other | |
| VSS | Y3 | Power/Other | |
| VSS | Y6 | Power/Other | |
| VSS_SENSE | AE7 | Power/Other | Output |

## Table 18. Pin Listing by Pin Number (Sheet 1 of 12)

| Pin # | Pin Name | Signal Buffer Type | Direction |
|---|---|---|---|
| A2 | VSS | Power/Other | |
| A3 | SMI# | CMOS | Input |
| A4 | VSS | Power/Other | |
| A5 | FERR# | Open Drain | Output |
| A6 | A20M# | CMOS | Input |
| A7 | VCC | Power/Other | |
| A8 | VSS | Power/Other | |
| A9 | VCC | Power/Other | |
| A10 | VCC | Power/Other | |
| A11 | VSS | Power/Other | |
| A12 | VCC | Power/Other | |
| A13 | VCC | Power/Other | |
| A14 | VSS | Power/Other | |
| A15 | VCC | Power/Other | |
| A16 | VSS | Power/Other | |
| A17 | VCC | Power/Other | |
| A18 | VCC | Power/Other | |
| A19 | VSS | Power/Other | |
| A20 | VCC | Power/Other | |
| A21 | BCLK[1] | Bus Clock | Input |
| A22 | BCLK[0] | Bus Clock | Input |
| A23 | VSS | Power/Other | |
| A24 | THERMDA | Power/Other | |
| A25 | THERMDC | Power/Other | |
| A26 | VSS | Power/Other | |
| B1 | RESET# | Common Clock | Input |
| B2 | RSVD | Reserved | |
| B3 | INIT# | CMOS | Input |
| B4 | LINT1 | CMOS | Input |
| B5 | DPSLP# | CMOS | Input |
| B6 | VSS | Power/Other | |
| B7 | VCC | Power/Other | |
| B8 | VSS | Power/Other | |
| B9 | VCC | Power/Other | |
| B10 | VCC | Power/Other | |
| B11 | VSS | Power/Other | |
| B12 | VCC | Power/Other | |
| B13 | VSS | Power/Other | |
| B14 | VCC | Power/Other | |
| B15 | VCC | Power/Other | |
| B16 | VSS | Power/Other | |
| B17 | VCC | Power/Other | |

## Table 18. Pin Listing by Pin Number (Sheet 2 of 12)

| Pin # | Pin Name | Signal Buffer Type | Direction |
|---|---|---|---|
| B18 | VCC | Power/Other | |
| B19 | VSS | Power/Other | |
| B20 | VCC | Power/Other | |
| B21 | VSS | Power/Other | |
| B22 | BSEL[0] | CMOS | Output |
| B23 | BSEL[1] | CMOS | Output |
| B24 | VSS | Power/Other | |
| B25 | TEST4 | Test | |
| B26 | VCCA | Power/Other | |
| C1 | RSVD | Reserved | |
| C2 | VSS | Power/Other | |
| C3 | RSVD | Reserved | |
| C4 | IGNNE# | CMOS | Input |
| C5 | VSS | Power/Other | |
| C6 | LINT0 | CMOS | Input |
| C7 | THERMTRIP# | Open Drain | Output |
| C8 | VSS | Power/Other | |
| C9 | VCC | Power/Other | |
| C10 | VCC | Power/Other | |
| C11 | VSS | Power/Other | |
| C12 | VCC | Power/Other | |
| C13 | VCC | Power/Other | |
| C14 | VSS | Power/Other | |
| C15 | VCC | Power/Other | |
| C16 | VSS | Power/Other | |
| C17 | VCC | Power/Other | |
| C18 | VCC | Power/Other | |
| C19 | VSS | Power/Other | |
| C20 | DBR# | CMOS | Output |
| C21 | BSEL[2] | CMOS | Output |
| C22 | VSS | Power/Other | |
| C23 | RSVD | Reserved | |
| C24 | RSVD | Reserved | |
| C25 | VSS | Power/Other | |
| C26 | TEST1 | Test | |
| D1 | VSS | Power/Other | |
| D2 | RSVD | Reserved | |
| D3 | RSVD | Reserved | |
| D4 | VSS | Power/Other | |
| D5 | STPCLK# | CMOS | Input |
| D6 | PWRGOOD | CMOS | Input |
| D7 | SLP# | CMOS | Input |

**Table 18. Pin Listing by Pin Number (Sheet 3 of 12)**

| Pin # | Pin Name | Signal Buffer Type | Direction |
|---|---|---|---|
| D8 | VSS | Power/Other | |
| D9 | VCC | Power/Other | |
| D10 | VCC | Power/Other | |
| D11 | VSS | Power/Other | |
| D12 | VCC | Power/Other | |
| D13 | VSS | Power/Other | |
| D14 | VCC | Power/Other | |
| D15 | VCC | Power/Other | |
| D16 | VSS | Power/Other | |
| D17 | VCC | Power/Other | |
| D18 | VCC | Power/Other | |
| D19 | VSS | Power/Other | |
| D20 | IERR# | Open Drain | Output |
| D21 | PROCHOT# | Open Drain | Input/Output |
| D22 | RSVD | Reserved | |
| D23 | VSS | Power/Other | |
| D24 | DPWR# | Common Clock | Input |
| D25 | TEST2 | Test | |
| D26 | VSS | Power/Other | |
| E1 | DBSY# | Common Clock | Input/Output |
| E2 | BNR# | Common Clock | Input/Output |
| E3 | VSS | Power/Other | |
| E4 | HITM# | Common Clock | Input/Output |
| E5 | DPRSTP# | CMOS | Input |
| E6 | VSS | Power/Other | |
| E7 | VCC | Power/Other | |
| E8 | VSS | Power/Other | |
| E9 | VCC | Power/Other | |
| E10 | VCC | Power/Other | |
| E11 | VSS | Power/Other | |
| E12 | VCC | Power/Other | |
| E13 | VCC | Power/Other | |
| E14 | VSS | Power/Other | |
| E15 | VCC | Power/Other | |
| E16 | VSS | Power/Other | |
| E17 | VCC | Power/Other | |
| E18 | VCC | Power/Other | |
| E19 | VSS | Power/Other | |
| E20 | VCC | Power/Other | |
| E21 | VSS | Power/Other | |
| E22 | D[0]# | Source Synch | Input/Output |
| E23 | D[7]# | Source Synch | Input/Output |

**Table 18. Pin Listing by Pin Number (Sheet 4 of 12)**

| Pin # | Pin Name | Signal Buffer Type | Direction |
|---|---|---|---|
| E24 | VSS | Power/Other | |
| E25 | D[6]# | Source Synch | Input/Output |
| E26 | D[2]# | Source Synch | Input/Output |
| F1 | BR0# | Common Clock | Input/Output |
| F2 | VSS | Power/Other | |
| F3 | RS[0]# | Common Clock | Input |
| F4 | RS[1]# | Common Clock | Input |
| F5 | VSS | Power/Other | |
| F6 | RSVD | Reserved | |
| F7 | VCC | Power/Other | |
| F8 | VSS | Power/Other | |
| F9 | VCC | Power/Other | |
| F10 | VCC | Power/Other | |
| F11 | VSS | Power/Other | |
| F12 | VCC | Power/Other | |
| F13 | VSS | Power/Other | |
| F14 | VCC | Power/Other | |
| F15 | VCC | Power/Other | |
| F16 | VSS | Power/Other | |
| F17 | VCC | Power/Other | |
| F18 | VCC | Power/Other | |
| F19 | VSS | Power/Other | |
| F20 | VCC | Power/Other | |
| F21 | DRDY# | Common Clock | Input/Output |
| F22 | VSS | Power/Other | |
| F23 | D[4]# | Source Synch | Input/Output |
| F24 | D[1]# | Source Synch | Input/Output |
| F25 | VSS | Power/Other | |
| F26 | D[13]# | Source Synch | Input/Output |
| G1 | VSS | Power/Other | |
| G2 | TRDY# | Common Clock | Input |
| G3 | RS[2]# | Common Clock | Input |
| G4 | VSS | Power/Other | |
| G5 | BPRI# | Common Clock | Input |
| G6 | HIT# | Common Clock | Input/Output |
| G21 | VCCP | Power/Other | |
| G22 | DSTBP[0]# | Source Synch | Input/Output |
| G23 | VSS | Power/Other | |
| G24 | D[9]# | Source Synch | Input/Output |
| G25 | D[5]# | Source Synch | Input/Output |
| G26 | VSS | Power/Other | |
| H1 | ADS# | Common Clock | Input/Output |

## Table 18. Pin Listing by Pin Number (Sheet 5 of 12)

| Pin # | Pin Name | Signal Buffer Type | Direction |
|---|---|---|---|
| H2 | REQ[1]# | Source Synch | Input/Output |
| H3 | VSS | Power/Other | |
| H4 | LOCK# | Common Clock | Input/Output |
| H5 | DEFER# | Common Clock | Input |
| H6 | VSS | Power/Other | |
| H21 | VSS | Power/Other | |
| H22 | D[3]# | Source Synch | Input/Output |
| H23 | DSTBN[0]# | Source Synch | Input/Output |
| H24 | VSS | Power/Other | |
| H25 | D[15]# | Source Synch | Input/Output |
| H26 | D[12]# | Source Synch | Input/Output |
| J1 | A[9]# | Source Synch | Input/Output |
| J2 | VSS | Power/Other | |
| J3 | REQ[3]# | Source Synch | Input/Output |
| J4 | A[3]# | Source Synch | Input/Output |
| J5 | VSS | Power/Other | |
| J6 | VCCP | Power/Other | |
| J21 | VCCP | Power/Other | |
| J22 | VSS | Power/Other | |
| J23 | D[11]# | Source Synch | Input/Output |
| J24 | D[10]# | Source Synch | Input/Output |
| J25 | VSS | Power/Other | |
| J26 | DINV[0]# | Source Synch | Input/Output |
| K1 | VSS | Power/Other | |
| K2 | REQ[2]# | Source Synch | Input/Output |
| K3 | REQ[0]# | Source Synch | Input/Output |
| K4 | VSS | Power/Other | |
| K5 | A[6]# | Source Synch | Input/Output |
| K6 | VCCP | Power/Other | |
| K21 | VCCP | Power/Other | |
| K22 | D[14]# | Source Synch | Input/Output |
| K23 | VSS | Power/Other | |
| K24 | D[8]# | Source Synch | Input/Output |
| K25 | D[17]# | Source Synch | Input/Output |
| K26 | VSS | Power/Other | |
| L1 | A[13]# | Source Synch | Input/Output |
| L2 | ADSTB[0]# | Source Synch | Input/Output |
| L3 | VSS | Power/Other | |
| L4 | A[4]# | Source Synch | Input/Output |
| L5 | REQ[4]# | Source Synch | Input/Output |
| L6 | VSS | Power/Other | |
| L21 | VSS | Power/Other | |

## Table 18. Pin Listing by Pin Number (Sheet 6 of 12)

| Pin # | Pin Name | Signal Buffer Type | Direction |
|---|---|---|---|
| L22 | D[21]# | Source Synch | Input/Output |
| L23 | D[22]# | Source Synch | Input/Output |
| L24 | VSS | Power/Other | |
| L25 | D[20]# | Source Synch | Input/Output |
| L26 | D[29]# | Source Synch | Input/Output |
| M1 | A[7]# | Source Synch | Input/Output |
| M2 | VSS | Power/Other | |
| M3 | A[5]# | Source Synch | Input/Output |
| M4 | RSVD | Reserved | |
| M5 | VSS | Power/Other | |
| M6 | VCCP | Power/Other | |
| M21 | VCCP | Power/Other | |
| M22 | VSS | Power/Other | |
| M23 | D[23]# | Source Synch | Input/Output |
| M24 | DSTBN[1]# | Source Synch | Input/Output |
| M25 | VSS | Power/Other | |
| M26 | DINV[1]# | Source Synch | Input/Output |
| N1 | VSS | Power/Other | |
| N2 | A[8]# | Source Synch | Input/Output |
| N3 | A[10]# | Source Synch | Input/Output |
| N4 | VSS | Power/Other | |
| N5 | RSVD | Reserved | |
| N6 | VCCP | Power/Other | |
| N21 | VCCP | Power/Other | |
| N22 | D[16]# | Source Synch | Input/Output |
| N23 | VSS | Power/Other | |
| N24 | D[31]# | Source Synch | Input/Output |
| N25 | DSTBP[1]# | Source Synch | Input/Output |
| N26 | VSS | Power/Other | |
| P1 | A[15]# | Source Synch | Input/Output |
| P2 | A[12]# | Source Synch | Input/Output |
| P3 | VSS | Power/Other | |
| P4 | A[14]# | Source Synch | Input/Output |
| P5 | A[11]# | Source Synch | Input/Output |
| P6 | VSS | Power/Other | |
| P21 | VSS | Power/Other | |
| P22 | D[25]# | Source Synch | Input/Output |
| P23 | D[26]# | Source Synch | Input/Output |
| P24 | VSS | Power/Other | |
| P25 | D[24]# | Source Synch | Input/Output |
| P26 | D[18]# | Source Synch | Input/Output |
| R1 | A[16]# | Source Synch | Input/Output |

**Table 18. Pin Listing by Pin Number (Sheet 7 of 12)**

| Pin # | Pin Name | Signal Buffer Type | Direction |
|---|---|---|---|
| R2 | VSS | Power/Other | |
| R3 | A[19]# | Source Synch | Input/Output |
| R4 | A[24]# | Source Synch | Input/Output |
| R5 | VSS | Power/Other | |
| R6 | VCCP | Power/Other | |
| R21 | VCCP | Power/Other | |
| R22 | VSS | Power/Other | |
| R23 | D[19]# | Source Synch | Input/Output |
| R24 | D[28]# | Source Synch | Input/Output |
| R25 | VSS | Power/Other | |
| R26 | COMP[0] | Power/Other | Input/Output |
| T1 | VSS | Power/Other | |
| T2 | RSVD | Reserved | |
| T3 | A[26]# | Source Synch | Input/Output |
| T4 | VSS | Power/Other | |
| T5 | A[25]# | Source Synch | Input/Output |
| T6 | VCCP | Power/Other | |
| T21 | VCCP | Power/Other | |
| T22 | RSVD | Reserved | |
| T23 | VSS | Power/Other | |
| T24 | D[27]# | Source Synch | Input/Output |
| T25 | D[30]# | Source Synch | Input/Output |
| T26 | VSS | Power/Other | |
| U1 | COMP[2] | Power/Other | Input/Output |
| U2 | A[23]# | Source Synch | Input/Output |
| U3 | VSS | Power/Other | |
| U4 | A[21]# | Source Synch | Input/Output |
| U5 | A[18]# | Source Synch | Input/Output |
| U6 | VSS | Power/Other | |
| U21 | VSS | Power/Other | |
| U22 | D[39]# | Source Synch | Input/Output |
| U23 | D[37]# | Source Synch | Input/Output |
| U24 | VSS | Power/Other | |
| U25 | D[38]# | Source Synch | Input/Output |
| U26 | COMP[1] | Power/Other | Input/Output |
| V1 | COMP[3] | Power/Other | Input/Output |
| V2 | VSS | Power/Other | |
| V3 | RSVD | Reserved | |
| V4 | ADSTB[1]# | Source Synch | Input/Output |
| V5 | VSS | Power/Other | |
| V6 | VCCP | Power/Other | |
| V21 | VCCP | Power/Other | |

**Table 18. Pin Listing by Pin Number (Sheet 8 of 12)**

| Pin # | Pin Name | Signal Buffer Type | Direction |
|---|---|---|---|
| V22 | VSS | Power/Other | |
| V23 | DINV[2]# | Source Synch | Input/Output |
| V24 | D[34]# | Source Synch | Input/Output |
| V25 | VSS | Power/Other | |
| V26 | D[35]# | Source Synch | Input/Output |
| W1 | VSS | Power/Other | |
| W2 | A[30]# | Source Synch | Input/Output |
| W3 | A[27]# | Source Synch | Input/Output |
| W4 | VSS | Power/Other | |
| W5 | A[28]# | Source Synch | Input/Output |
| W6 | A[20]# | Source Synch | Input/Output |
| W21 | VCCP | Power/Other | |
| W22 | D[41]# | Source Synch | Input/Output |
| W23 | VSS | Power/Other | |
| W24 | DSTBN[2]# | Source Synch | Input/Output |
| W25 | D[36]# | Source Synch | Input/Output |
| W26 | VSS | Power/Other | |
| Y1 | A[31]# | Source Synch | Input/Output |
| Y2 | A[17]# | Source Synch | Input/Output |
| Y3 | VSS | Power/Other | |
| Y4 | A[29]# | Source Synch | Input/Output |
| Y5 | A[22]# | Source Synch | Input/Output |
| Y6 | VSS | Power/Other | |
| Y21 | VSS | Power/Other | |
| Y22 | D[45]# | Source Synch | Input/Output |
| Y23 | D[42]# | Source Synch | Input/Output |
| Y24 | VSS | Power/Other | |
| Y25 | DSTBP[2]# | Source Synch | Input/Output |
| Y26 | D[44]# | Source Synch | Input/Output |
| AA1 | A[32]# | Source Synch | Input/Output |
| AA2 | VSS | Power/Other | |
| AA3 | A[35]# | Source Synch | Input/Output |
| AA4 | A[33]# | Source Synch | Input/Output |
| AA5 | VSS | Power/Other | |
| AA6 | TDI | CMOS | Input |
| AA7 | VCC | Power/Other | |
| AA8 | VSS | Power/other | |
| AA9 | VCC | Power/Other | |
| AA10 | VCC | Power/Other | |
| AA11 | VSS | Power/Other | |
| AA12 | VCC | Power/Other | |
| AA13 | VCC | Power/Other | |

**Table 18. Pin Listing by Pin Number (Sheet 9 of 12)**

| Pin # | Pin Name | Signal Buffer Type | Direction |
|---|---|---|---|
| AA14 | VSS | Power/Other | |
| AA15 | VCC | Power/Other | |
| AA16 | VSS | Power/Other | |
| AA17 | VCC | Power/Other | |
| AA18 | VCC | Power/Other | |
| AA19 | VSS | Power/Other | |
| AA20 | VCC | Power/Other | |
| AA21 | D[51]# | Source Synch | Input/Output |
| AA22 | VSS | Power/Other | |
| AA23 | D[32]# | Source Synch | Input/Output |
| AA24 | D[47]# | Source Synch | Input/Output |
| AA25 | VSS | Power/Other | |
| AA26 | D[43]# | Source Synch | Input/Output |
| AB1 | VSS | Power/Other | |
| AB2 | A[34]# | Source Synch | Input/Output |
| AB3 | TDO | Open Drain | Output |
| AB4 | VSS | Power/Other | |
| AB5 | TMS | CMOS | Input |
| AB6 | TRST# | CMOS | Input |
| AB7 | VCC | Power/Other | |
| AB8 | VSS | Power/Other | |
| AB9 | VCC | Power/Other | |
| AB10 | VCC | Power/Other | |
| AB11 | VSS | Power/Other | |
| AB12 | VCC | Power/Other | |
| AB13 | VSS | Power/Other | |
| AB14 | VCC | Power/Other | |
| AB15 | VCC | Power/Other | |
| AB16 | VSS | Power/Other | |
| AB17 | VCC | Power/Other | |
| AB18 | VCC | Power/Other | |
| AB19 | VSS | Power/Other | |
| AB20 | VCC | Power/Other | |
| AB21 | D[52]# | Source Synch | Input/Output |
| AB22 | D[50]# | Source Synch | Input/Output |
| AB23 | VSS | Power/Other | |
| AB24 | D[33]# | Source Synch | Input/Output |
| AB25 | D[40]# | Source Synch | Input/Output |
| AB26 | VSS | Power/Other | |
| AC1 | PREQ# | Common Clock | Input |
| AC2 | PRDY# | Common Clock | Output |
| AC3 | VSS | Power/Other | |

**Table 18. Pin Listing by Pin Number (Sheet 10 of**

| Pin # | Pin Name | Signal Buffer Type | Direction |
|---|---|---|---|
| AC4 | BPM[3]# | Common Clock | Input/Output |
| AC5 | TCK | CMOS | Input |
| AC6 | VSS | Power/Other | |
| AC7 | VCC | Power/Other | |
| AC8 | VSS | Power/Other | |
| AC9 | VCC | Power/Other | |
| AC10 | VCC | Power/Other | |
| AC11 | VSS | Power/Other | |
| AC12 | VCC | Power/Other | |
| AC13 | VCC | Power/Other | |
| AC14 | VSS | Power/Other | |
| AC15 | VCC | Power/Other | |
| AC16 | VSS | Power/Other | |
| AC17 | VCC | Power/Other | |
| AC18 | VCC | Power/Other | |
| AC19 | VSS | Power/Other | |
| AC20 | DINV[3]# | Source Synch | Input/Output |
| AC21 | VSS | Power/Other | |
| AC22 | D[48]# | Source Synch | Input/Output |
| AC23 | D[49]# | Source Synch | Input/Output |
| AC24 | VSS | Power/Other | |
| AC25 | D[53]# | Source Synch | Input/Output |
| AC26 | D[46]# | Source Synch | Input/Output |
| AD1 | BPM[2]# | Common Clock | Output |
| AD2 | VSS | Power/Other | |
| AD3 | BPM[1]# | Common Clock | Output |
| AD4 | BPM[0]# | Common Clock | Input/Output |
| AD5 | VSS | Power/Other | |
| AD6 | VID[0] | CMOS | Output |
| AD7 | VCC | Power/Other | |
| AD8 | VSS | Power/Other | |
| AD9 | VCC | Power/Other | |
| AD10 | VCC | Power/Other | |
| AD11 | VSS | Power/Other | |
| AD12 | VCC | Power/Other | |
| AD13 | VSS | Power/Other | |
| AD14 | VCC | Power/Other | |
| AD15 | VCC | Power/Other | |
| AD16 | VSS | Power/Other | |
| AD17 | VCC | Power/Other | |
| AD18 | VCC | Power/Other | |
| AD19 | VSS | Power/Other | |

**Table 18. Pin Listing by Pin Number (Sheet 11 of**

| Pin # | Pin Name | Signal Buffer Type | Direction |
|---|---|---|---|
| AD20 | D[54]# | Source Synch | Input/Output |
| AD21 | D[59]# | Source Synch | Input/Output |
| AD22 | VSS | Power/Other | |
| AD23 | DSTBN[3]# | Source Synch | Input/Output |
| AD24 | D[57]# | Source Synch | Input/Output |
| AD25 | VSS | Power/Other | |
| AD26 | GTLREF | Power/Other | Input |
| AE1 | VSS | Power/Other | |
| AE2 | VID[6] | CMOS | Output |
| AE3 | VID[4] | CMOS | Output |
| AE4 | VSS | Power/Other | |
| AE5 | VID[2] | CMOS | Output |
| AE6 | PSI# | CMOS | Output |
| AE7 | VSS_SENSE | Power/Other | Output |
| AE8 | VSS | Power/Other | |
| AE9 | VCC | Power/Other | |
| AE10 | VCC | Power/Other | |
| AE11 | VSS | Power/Other | |
| AE12 | VCC | Power/Other | |
| AE13 | VCC | Power/Other | |
| AE14 | VSS | Power/Other | |
| AE15 | VCC | Power/Other | |
| AE16 | VSS | Power/Other | |
| AE17 | VCC | Power/Other | |
| AE18 | VCC | Power/Other | |
| AE19 | VSS | Power/Other | |
| AE20 | VCC | Power/Other | |
| AE21 | D[58]# | Source Synch | Input/Output |
| AE22 | D[55]# | Source Synch | Input/Output |
| AE23 | VSS | Power/Other | |
| AE24 | DSTBP[3]# | Source Synch | Input/Output |
| AE25 | D[60]# | Source Synch | Input/Output |
| AE26 | VSS | Power/Other | |
| AF1 | TEST3 | Test | |
| AF2 | VID[5] | CMOS | Output |
| AF3 | VSS | Power/Other | |
| AF4 | VID[3] | CMOS | Output |
| AF5 | VID[1] | CMOS | Output |
| AF6 | VSS | Power/Other | |
| AF7 | VCC_SENSE | Power/Other | |
| AF8 | VSS | Power/Other | |
| AF9 | VCC | Power/Other | |

**Table 18. Pin Listing by Pin Number (Sheet 12 of**

| Pin # | Pin Name | Signal Buffer Type | Direction |
|---|---|---|---|
| AF10 | VCC | Power/Other | |
| AF11 | VSS | Power/Other | |
| AF12 | VCC | Power/Other | |
| AF13 | VSS | Power/Other | |
| AF14 | VCC | Power/Other | |
| AF15 | VCC | Power/Other | |
| AF16 | VSS | Power/Other | |
| AF17 | VCC | Power/Other | |
| AF18 | VCC | Power/Other | |
| AF19 | VSS | Power/Other | |
| AF20 | VCC | Power/Other | |
| AF21 | VSS | Power/Other | |
| AF22 | D[62]# | Source Synch | Input/Output |
| AF23 | D[56]# | Source Synch | Input/Output |
| AF24 | VSS | Power/Other | |
| AF25 | D[61]# | Source Synch | Input/Output |
| AF26 | D[63]# | Source Synch | Input/Output |

## 4.3 Alphabetical Signals Reference

**Table 19. Signal Description (Sheet 1 of 8)**

| Name | Type | Description |
|---|---|---|
| A[35:3]# | Input/ Output | A[35:3]# (Address) define a $2^{36}$-byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of both agents on the Celeron FSB. A[35:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. Address signals are used as straps which are sampled before RESET# is de-asserted.<br>**NOTE: When paired with a chipset limited to 32-bit addressing, A[35:32] should remain unconnected** |
| A20M# | Input | If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode.<br>A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/ Output Write bus transaction. |
| ADS# | Input/ Output | ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[35:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction. |
| ADSTB[1:0]# | Input/ Output | Address strobes are used to latch A[35:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below.<br>**Signals** — **Associated Strobe**<br>REQ[4:0]#, A[16:3]# — ADSTB[0]#<br>A[35:17]# — ADSTB[1]# |
| BCLK[1:0] | Input | The differential pair BCLK (Bus Clock) determines the FSB frequency. All FSB agents must receive these signals to drive their outputs and latch their inputs.<br>All external timing parameters are specified with respect to the rising edge of BCLK0 crossing $V_{CROSS}$. |
| BNR# | Input/ Output | BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions. |

## Table 19. Signal Description (Sheet 2 of 8)

| Name | Type | Description |
|---|---|---|
| BPM[2:1]#<br><br>BPM[3,0]# | Output<br><br>Input/ Output | BPM[3:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[3:0]# should connect the appropriate pins of all Celeron FSB agents.This includes debug or performance monitoring tools. |
| BPRI# | Input | BPRI# (Bus Priority Request) is used to arbitrate for ownership of the FSB. It must connect the appropriate pins of both FSB agents. Observing BPRI# active (as asserted by the priority agent) causes the other agent to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by de-asserting BPRI#. |
| BR0# | Input/ Output | BR0# is used by the processor to request the bus. The arbitration is done between Celeron (Symmetric Agent) and northbridge (High Priority Agent).<br>This signal does not have on-die termination and must be terminated. |
| BSEL[2:0] | Output | BSEL[2:0] (Bus Select) are used to select the processor input clock frequency. Table 15 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset and clock synthesizer. All agents must operate at the same frequency. The Celeron processor 200 sequence operates at a 533-MHz system bus frequency (133-MHz BCLK[1:0] frequency). |
| COMP[3:0] | Analog | COMP[3:0] must be terminated on the system board using precision (1% tolerance) resistors. |
| D[63:0]# | Input/ Output | D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the FSB agents, and must connect the appropriate pins on both agents. The data driver asserts DRDY# to indicate a valid data transfer.<br>D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DINV#.<br>**Quad-Pumped Signal Groups**<br>**Data Group** / **DSTBN# / DSTBP#** / **DINV#**<br>D[15:0]# — 0 — 0<br>D[31:16]# — 1 — 1<br>D[47:32]# — 2 — 2<br>D[63:48]# — 3 — 3<br>Furthermore, the DINV# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DINV# signal. When the DINV# signal is active, the corresponding data group is inverted and therefore sampled active high. |

**Table 19. Signal Description (Sheet 3 of 8)**

| Name | Type | Description |
|---|---|---|
| DBR# | Output | DBR# (Data Bus Reset) is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect in the system. DBR# is not a processor signal. |
| DBSY# | Input/ Output | DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the FSB to indicate that the data bus is in use. The data bus is released after DBSY# is de-asserted. This signal must connect the appropriate pins on both FSB agents. |
| DEFER# | Input | DEFER# is asserted by an agent to indicate that a transaction cannot be ensured in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of both FSB agents. |
| DINV[3:0]# | Input/ Output | DINV[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DINV[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle.<br>**DINV[3:0]# Assignment to Data Bus**<br>**Bus Signal** / **Data Bus Signals**<br>DINV[3]# — D[63:48]#<br>DINV[2]# — D[47:32]#<br>DINV[1]# — D[31:16]#<br>DINV[0]# — D[15:0]# |
| DPRSTP# | Input | DPRSTP# is not used by the Celeron processor. |
| DPWR# | Input | DPWR# is a control signal used by the chipset to reduce power on the processor data bus input buffers. This is not used by the processor. |
| DRDY# | Input/ Output | DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be de-asserted to insert idle clocks. This signal must connect the appropriate pins of both FSB agents. |
| DSTBN[3:0]# | Input/ Output | Data strobe used to latch in D[63:0]#.<br>**Signals** / **Associated Strobe**<br>D[15:0]#, DINV[0]# — DSTBN[0]#<br>D[31:16]#, DINV[1]# — DSTBN[1]#<br>D[47:32]#, DINV[2]# — DSTBN[2]#<br>D[63:48]#, DINV[3]# — DSTBN[3]# |

## Table 19. Signal Description (Sheet 4 of 8)

| Name | Type | Description |
|---|---|---|
| DSTBP[3:0]# | Input/ Output | Data strobe used to latch in D[63:0]#.<br><br>**Signals** — **Associated Strobe**<br>D[15:0]#, DINV[0]# — DSTBP[0]#<br>D[31:16]#, DINV[1]# — DSTBP[1]#<br>D[47:32]#, DINV[2]# — DSTBP[2]#<br>D[63:48]#, DINV[3]# — DSTBP[3]# |
| FERR#/PBE# | Output | FERR# (Floating-point Error)/PBE#(Pending Break Event) is a multiplexed signal and its meaning is qualified with STPCLK#. When STPCLK# is not asserted, FERR#/PBE# assertion indicates that an unmasked floating point error has been detected. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. In both cases, assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/ PBE# is asserted, indicating a break event, it will remain asserted until STPCLK# is de-asserted. Assertion of PREQ# when STPCLK# is active will also cause an FERR# break event.<br>For additional information on the pending break event functionality, including identification of support of the feature and enable/disable information, refer to Volume 3 of the *Intel® Architecture Software Developer's Manual* and the *Intel® Processor Identification and CPUID Instruction* application note. |
| GTLREF | Input | GTLREF determines the signal reference level for GTL+ input pins. GTLREF should be set at 2/3 $V_{CCP}$. GTLREF is used by the GTL+ receivers to determine if a signal is a logical 0 or logical 1. |
| HIT#<br><br>HITM# | Input/ Output<br><br>Input/ Output | HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Either FSB agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by re-asserting HIT# and HITM# together. |
| IERR# | Output | IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the FSB. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#. |
| IGNNE# | Input | IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is de-asserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set.<br>IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/ Output Write bus transaction. |

**Table 19. Signal Description (Sheet 5 of 8)**

| Name | Type | Description |
|---|---|---|
| INIT# | Input | INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output Write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction. INIT# must connect the appropriate pins of both FSB agents.<br>If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST). |
| LINT[1:0] | Input | LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous.<br>Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/ INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration. |
| LOCK# | Input/ Output | LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of both FSB agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction.<br>When the priority agent asserts BPRI# to arbitrate for ownership of the FSB, it will wait until it observes LOCK# de-asserted. This enables symmetric agents to retain ownership of the FSB throughout the bus locked operation and ensure the atomicity of lock. |
| PRDY# | Output | Probe Ready signal used by debug tools to determine processor debug readiness. |
| PREQ# | Input | Probe Request signal used by debug tools to request debug operation of the processor. |
| PROCHOT# | Input/ Output | As an output, PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. As an input, assertion of PROCHOT# by the system will activate the TCC, if enabled. The TCC will remain active until the system de-asserts PROCHOT#.<br>This signal may require voltage translation on the motherboard. |

## Table 19. Signal Description (Sheet 6 of 8)

| Name | Type | Description |
|---|---|---|
| PWRGOOD | Input | PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. “Clean” implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD.<br>The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation. |
| REQ[4:0]# | Input/ Output | REQ[4:0]# (Request Command) must connect the appropriate pins of both FSB agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB[0]#. |
| RESET# | Input | Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least two milliseconds after $V_{CC}$ and BCLK have reached their proper specifications. On observing active RESET#, both FSB agents will de-assert their outputs within two clocks. All processor straps must be valid within the specified setup time before RESET# is de-asserted.<br>There is a 55-Ω (nominal) on die pull-up resistor on this signal. |
| RS[2:0]# | Input | RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of both FSB agents. |
| RSVD | Reserved /No Connect | These pins are RESERVED and must be left unconnected on the board. However, it is recommended that routing channels to these pins on the board be kept open for possible future use. |
| SLP# | Input | SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, de-assertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is de-asserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If DPSLP# is asserted while in the Sleep state, the processor will exit the Sleep state and transition to the Deep Sleep state. |
| SMI# | Input | SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.<br>If SMI# is asserted during the de-assertion of RESET# the processor will tristate its outputs. |

**Table 19. Signal Description (Sheet 7 of 8)**

| Name | Type | Description |
|---|---|---|
| STPCLK# | Input | STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the FSB and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is de-asserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input. |
| TCK | Input | TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port). |
| TDI | Input | TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support. |
| TDO | Output | TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support. |
| TEST1, TEST2, TEST3, TEST4 | Input | TEST1 and TEST2 must have a stuffing option of separate pull down resistors to $V_{SS}$.<br>For testing purposes it is recommended, but not required, to route the TEST3 and TEST4 pins through a ground referenced 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection. |
| THERMTRIP# | Output | The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 125°C. This is signalled to the system by the THERMTRIP# (Thermal Trip) pin. |
| TMS | Input | TMS (Test Mode Select) is a JTAG specification support signal used by debug tools. |
| TRDY# | Input | TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of both FSB agents. |
| TRST# | Input | TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. |
| $V_{CC}$ | Input | Processor core power supply. |
| VCCA | Input | VCCA provides isolated power for the internal processor core PLLs. |
| $V_{CCP}$ | Input | Processor I/O Power Supply. |

**Table 19. Signal Description (Sheet 8 of 8)**

| Name | Type | Description |
|---|---|---|
| VCC_SENSE | Output | VCC_SENSE together with VSS_SENSE are voltage feedback signals to IMVP 6 that control the 2.1-mΩ loadline at the processor die. It should be used to sense or measure power near the silicon with little noise. |
| VID[6:0] | Output | VID[6:0] (Voltage ID) pins are used to support automatic selection of power supply voltages ($V_{CC}$). Unlike some previous generations of processors, these are CMOS signals that are driven by the Celeron processor. The voltage supply for these pins must be valid before the VR can supply $V_{CC}$ to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations. See Table 2 for definitions of these pins. The VR must supply the voltage that is requested by the pins, or disable itself. |
| VSS_SENSE | Output | VSS_SENSE together with VCC_SENSE are voltage feedback signals to Intel MVP 6 that control the 2.1mohm loadline at the processor die. It should be used to sense or measure ground near the silicon with little noise. |

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# 5 Thermal Specifications

A complete thermal solution includes both component and system level thermal management features. The Celeron processor requires a thermal solution to maintain temperatures within operating limits.

***Caution:*** Any attempt to operate the processor outside operating limits may result in permanent damage to the processor and potentially other components in the system.

The system/processor thermal solution should remain within the minimum and maximum junction temperature (Tj) specifications at the corresponding thermal design power (TDP) value listed in Table 20.

For more information on designing a component level thermal solution, refer to the *Intel® Celeron® Processor 200 Sequence Thermal and Mechanical Design Guidelines*.

## 5.1 Thermal Specifications

To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed such that the processor remains within the minimum and maximum junction temperature ($T_J$) specifications when operating at or below the Thermal Design Power (TDP) value listed per frequency in Table 20. Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system. For more details on thermal solution design, refer to the *Intel® Celeron® Processor 200 Sequence Thermal and Mechanical Design Guidelines*.

The junction temperature is defined at the geometric top center of the processor. Analysis indicates that real applications are unlikely to cause the processor to consume maximum power dissipation for sustained time periods. Intel recommends that complete thermal solution designs target the Thermal Design Power (TDP) indicated in Table 20 instead of the maximum processor power consumption. The Thermal Monitor feature is designed to protect the processor in the unlikely event that an application exceeds the TDP recommendation for a sustained periods of time. For more details on the usage of this feature, refer to Section 5.3. In all cases the Thermal Monitor feature must be enabled for the processor to remain within specification.

**Table 20. Processor Thermal Specifications**

| Symbol | Processor Number | Core Frequency | Cache | Thermal Design Power | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| TDP | 220 | 1.20 GHz | 512 KB | 19 | | | W | 1,4,5 |
| **Symbol** | **Parameter** | | | **Min** | **Typ** | **Max** | **Unit** | |
| $T_J$ | Junction Temperature | | | 0 | | 100 | °C | 3,4 |

**NOTES:**
1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum $T_J$ has been reached.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
5. At Tj of 100 °C.



## 5.2 Processor Thermal Features

### 5.2.1 Thermal Monitor

The Thermal Monitor feature helps control the processor temperature by activating the thermal control circuit (TCC) when the processor silicon reaches its maximum operating temperature. The TCC reduces processor power consumption by modulating (starting and stopping) the internal processor core clocks. **The Thermal Monitor feature must be enabled for the processor to be operating within specifications.** The temperature at which Thermal Monitor activates the thermal control circuit is not user configurable and is not software visible. Bus traffic is snooped in the normal manner, and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

When the Thermal Monitor feature is enabled, and a high temperature situation exists (i.e., TCC is active), the clocks will be modulated by alternately turning the clocks off and on at a duty cycle specific to the processor (typically 30–50%). Clocks often will not be off for more than 3.0 microseconds when the TCC is active. Cycle times are processor speed dependent and will decrease as processor core frequencies increase. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the TCC goes inactive and clock modulation ceases.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would be immeasurable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss, and in some cases may result in a $T_J$ that exceeds the specified maximum temperature and may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under-designed may not be capable of cooling the processor even when the TCC is active continuously. Refer to the *Intel® Celeron® Processor 200 Sequence Thermal and Mechanical Design Guidelines* for information on designing a thermal solution.

The duty cycle for the TCC, when activated by the Thermal Monitor, is factory configured and cannot be modified. The Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines.

### 5.2.2 On-Demand Mode

The processor provides an auxiliary mechanism that allows system software to force the processor to reduce its power consumption. This mechanism is referred to as “On-Demand” mode and is distinct from the Thermal Monitor feature. On-Demand mode is intended as a means to reduce system level power consumption. Systems using the processor must not rely on software usage of this mechanism to limit the processor temperature.

If bit 4 of the ACPI P_CNT Control Register (located in the processor IA32_THERM_CONTROL MSR) is written to a '1', the processor will immediately reduce its power consumption via modulation (starting and stopping) of the internal core clock, independent of the processor temperature. When using On-Demand mode, the duty cycle of the clock modulation is programmable via bits 3:1 of the same ACPI P_CNT Control Register. In On-Demand mode, the duty cycle can be programmed from 12.5% on/87.5% off, to 87.5% on/12.5% off in 12.5% increments. On-Demand mode may be

used in conjunction with the Thermal Monitor. If the system tries to enable On-Demand mode at the same time the TCC is engaged, the factory configured duty cycle of the TCC will override the duty cycle selected by the On-Demand mode.

### 5.2.3 PROCHOT# Signal

An external signal, PROCHOT# (processor hot), is asserted when the processor core temperature has reached its maximum operating temperature. If the Thermal Monitor is enabled (note that the Thermal Monitor must be enabled for the processor to be operating within specification), the TCC will be active when PROCHOT# is asserted. The processor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT#.

As an output, PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the core has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. As an input, assertion of PROCHOT# by the system will activate the TCC, if enabled. The TCC will remain active until the system de-asserts PROCHOT#.

PROCHOT# allows for some protection of various components from over-temperature situations. The PROCHOT# signal is bi-directional in that it can either signal when the processor has reached its maximum operating temperature or be driven from an external source to activate the TCC. The ability to activate the TCC via PROCHOT# can provide a means for thermal protection of system components.

PROCHOT# can allow VR thermal designs to target maximum sustained current instead of maximum current. Systems should still provide proper cooling for the VR, and rely on PROCHOT# only as a backup in case of system cooling failure. The system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its Thermal Design Power. With a properly designed and characterized thermal solution, it is anticipated that PROCHOT# would only be asserted for very short periods of time when running the most power intensive applications. An under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may cause a noticeable performance loss. Refer to the *Voltage Regulator-Down (VRD) 11 Design Guide For Desktop and Transportable LGA775 Socket* for details on implementing the bi-directional PROCHOT# feature.

### 5.2.4 THERMTRIP# Signal

Regardless of whether or not Thermal Monitor is enabled, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached an elevated temperature (refer to the THERMTRIP# definition in Table 19). At this point, the FSB signal THERMTRIP# will go active and stay active as described in Table 19. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. If THERMTRIP# is asserted, processor core voltage ($V_{CC}$) must be removed within the timeframe defined in Table 11.

## 5.3 Processor Thermal Features

The Celeron processor incorporates three methods of monitoring die temperature:

- Intel® Thermal Monitor
- Digital Thermal Sensor

The Intel Thermal Monitor (detailed in Section 5.4) must be used to determine when the maximum specified processor junction temperature has been reached.

## 5.4 Intel® Thermal Monitor

The Intel Thermal Monitor helps control the processor temperature by activating the TCC (Thermal Control Circuit) when the processor silicon reaches its maximum operating temperature. The temperature at which the Intel Thermal Monitor activates the TCC is not user configurable. Bus traffic is snooped in the normal manner and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be minor and hence not detectable.

***Caution:*** An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss and may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under designed may not be capable of cooling the processor even when the TCC is active continuously.

The Intel Thermal Monitor controls the processor temperature by modulating (starting and stopping) the processor core clocks when the processor silicon reaches its maximum operating temperature. The Intel Thermal Monitor uses two modes to activate the TCC: Automatic mode and on-demand mode. If both modes are activated, automatic mode takes precedence.

***Note:*** The Intel Thermal Monitor automatic mode must be enabled through BIOS for the processor to be operating within specifications.

The processor supports an automatic mode called Intel Thermal Monitor 1 (TM1). This mode is enabled by writing values to the MSRs of the processor. After automatic mode is enabled, the TCC will activate only when the internal die temperature reaches the maximum allowed value for operation.

During high temperature situations, TM1 will modulate the clocks by alternately turning the clocks off and on at a 50% duty cycle. Cycle times are processor speed dependent and will decrease linearly as processor core frequencies increase. Once the temperature has returned to a non-critical level, modulation ceases and TCC goes inactive. A small amount of hysteresis has been included to prevent rapid active/ inactive transitions of the TCC when the processor temperature is near the trip point. The duty cycle is factory configured and cannot be modified. Also, automatic mode does not require any additional hardware, software drivers, or interrupt handling routines. Processor performance will be decreased by the same amount as the duty cycle when the TCC is active.

The TCC may also be activated via on-demand mode. If bit 4 of the ACPI Intel Thermal Monitor control register is written to a 1, the TCC will be activated immediately independent of the processor temperature. When using on-demand mode to activate the TCC, the duty cycle of the clock modulation is programmable via bits 3:1 of the same ACPI Intel Thermal Monitor control register. In automatic mode, the duty cycle is fixed at 50% on, 50% off, however in on-demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off, to 87.5% on/12.5% off in 12.5% increments. On-demand mode may be used at the same time automatic mode is enabled, however, if the system tries to enable the TCC via on-demand mode at the same time automatic mode is enabled and a high temperature condition exists, automatic mode will take precedence.

An external signal, PROCHOT# (processor hot) is asserted when the processor detects that its temperature is above the thermal trip point. Bus snooping and interrupt latching are also active while the TCC is active.

Besides the thermal sensor and thermal control circuit, the Intel Thermal Monitor also includes one ACPI register, one performance counter register, three MSR, and one I/O pin (PROCHOT#). All are available to monitor and control the state of the Intel Thermal Monitor feature. The Intel Thermal Monitor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT#.

***Note:*** PROCHOT# will not be asserted when the processor is in the Stop Grant, Sleep, and Deep Sleep low power states (internal clocks stopped.). As a result, the thermal diode reading must be used as a safeguard to maintain the processor junction temperature within maximum specification. If the platform thermal solution is not able to maintain the processor junction temperature within the maximum specification, the system must initiate an orderly shutdown to prevent damage. If the processor enters one of the above low power states with PROCHOT# already asserted, PROCHOT# will remain asserted until the processor exits the low power state and the processor junction temperature drops below the thermal trip point.

If Intel Thermal Monitor automatic mode is disabled, the processor will be operating out of specification. Regardless of enabling the automatic or on-demand modes, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached a temperature of approximately 125 °C. At this point the THERMTRIP# signal will go active. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. When THERMTRIP# is asserted, the processor core voltage must be shut down within the time specified in Chapter 3.

## 5.5 Digital Thermal Sensor

The Celeron processor also contains an on die Digital Thermal Sensor (DTS) that can be read via a MSR (no I/O interface). The DTS is the preferred method of reading the processor die temperature since it can be located much closer to the hottest portions of the die and can thus more accurately track the die temperature and potential activation of processor core clock modulation via the Intel Thermal Monitor. The DTS is only valid while the processor is in the normal operating state (C0 state).

Unlike traditional thermal devices, the DTS will output a temperature relative to the maximum supported operating temperature of the processor ($T_{J,max}$). It is the responsibility of software to convert the relative temperature to an absolute temperature. The temperature returned by the digital thermal sensor will always be at or below $T_{J,max}$. Over temperature conditions are detectable via an Out Of Spec status bit. This bit is also part of the DTS MSR. When this bit is set, the processor is operating out of specification and immediate shutdown of the system should occur. The processor operation and code execution is not ensured once the activation of the Out of Spec status bit is set. Note that there is a temperature offset and a time delay reading the die temperature using the DTS via MSR. The method to calculate $T_j$ should be DTS + 3 °C.

The DTS relative temperature readout corresponds to an Intel Thermal Monitor (TM1) trigger point. When the DTS indicates maximum processor core temperature has been reached the TM1 hardware thermal control mechanism will activate. The DTS and TM1 temperature may not correspond to the thermal diode reading since the thermal diode is located in a separate portion of the die. Additionally, the thermal gradient from DTS to thermal diode can vary substantially due to changes in processor power, mechanical and thermal attach and software application. The system designer is required to use the DTS to ensure proper operation of the processor within its temperature operating specifications.

Changes to the temperature can be detected via two programmable thresholds located in the processor MSRs. These thresholds have the capability of generating interrupts via the core's APIC. Refer to the *Intel® Architecture Software Developer's Manual* for specific register and programming details.

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