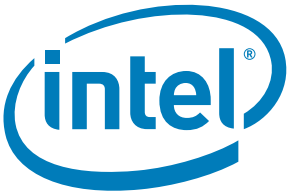

Intel® Platform Controller Hub MP30

Datasheet

May 2011

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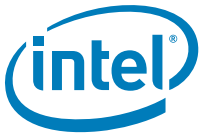

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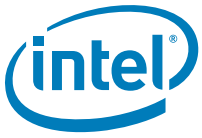
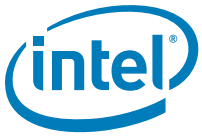


Figures

Tables



Revision History

Document Number	Revision Number	Description	Revision Date
325565	001	Initial release	May 2011

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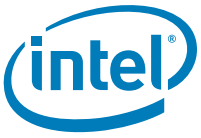

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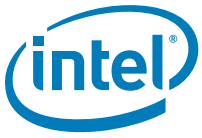

1 Read Me First

1.1 Abstract

The *Intel® Platform Controller Hub MP30 Datasheet* describes the architecture, features, buffers, signal descriptions, power management, pin states, operating parameters, electrical, mechanical, and thermal specifications for the Intel® Platform Controller Hub MP30.

1.2 About the Intel® Platform Controller Hub MP30 Datasheet

The *Intel® Platform Controller Hub MP30 Datasheet* is intended for use by hardware developers that are designing and manufacturing products using the Intel® Platform Controller Hub MP30.

1.3 Organization of the Intel® Platform Controller Hub MP30 Datasheet

The *Intel® Platform Controller Hub MP30 Datasheet* is composed of seven chapters and is organized as follows:

- Chapter 1—"Read Me First"
- Chapter 2—"Introduction"
- Chapter 3—"Signal Descriptions"
- Chapter 4—"Electrical Specifications"
- Chapter 5—"Absolute Maximums and Operating Conditions"
- Chapter 6—"Intel® Platform Controller Hub MP30 Pin States"
- Chapter 7—"Mechanical and Package Specifications"

Each chapter begins with a chapter contents description. This is high level information about the subject matter contained within chapter.

Some chapters contain a list of important acronyms and a description of the acronyms used in the chapter.

1.4 Reference Documents

Table 1-1. Intel® Platform Controller Hub MP30 Reference Documents (Sheet 1 of 2)

Document	Document Number/Location
Universal Host Controller Interface, Revision 1.1 (UHCI)	http://download.intel.com/technology/usb/UHCI11D.pdf
Enhanced Host Controller Interface Specification for Universal Serial Bus, Revision 1.0 (EHCI)	http://developer.intel.com/technology/usb/ehcispec.htm
Universal Serial Bus Specification (USB), Revision 2.0	http://www.usb.org/developers/docs

Table 1-1. Intel® Platform Controller Hub MP30 Reference Documents (Sheet 2 of 2)

Document	Document Number/Location
On-The-Go Supplement to the USB 2.0 Specification Rev 1.3	http://www.usb.org/developers/onthego/
SDIO Specification	http://www.sdcard.org/developers/tech/sdio/sdio_spec/
SD Host Controller Specification	http://www.sdcard.org/developers/tech/host_controller/simple_spec/
MIPI CSI-2 Specification	http://www.mipi.org/
I^2C Bus Specification	http://www.nxp.com/acrobat_download2/various/I2CBUS.pdf
I^2S Bus Specification	http://en-origin.nxp.com/acrobat_download2/various/I2SBUS.pdf
Intel® Atom™ Processor Z6xx Series Datasheet	325567-001[1,2]

NOTES:
1. Contact your Intel representative for the latest revision and document number for this document.
2. The Intel® Atom™ processor Z6xx series is also known as Lincroft.

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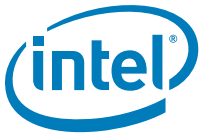


2 Introduction

2.1 Chapter Contents

This chapter contains information about:

- "Intel® Platform Controller Hub MP30 Acronyms and Terminology"
- "Architectural Overview"
- "Intel® Platform Controller Hub MP30 Feature Set"

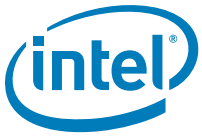
2.2 Intel® Platform Controller Hub MP30 Acronyms and Terminology

Table 2-1. Acronyms and Terminology (Sheet 1 of 2)

Acronym	Description
AMBA	Advanced Microcontroller Bus Architecture
AOAC	Always On, Always Connected
BGA	Ball Grid Array
Bluetooth*, BT	Bluetooth* is a local connectivity wireless protocol. Bluetooth* supports the transport of unencoded voice signals (that is, wireless headsets). Bluetooth* basebands typically have a PCM audio interface for the unencoded voice data and a UART or USB for control, data, and compressed audio (using sub-band coding).
BT.601/BT.656	ITU-R Recommendation BT.601/BT.656
cDMI	CMOS Direct Media Interface
cDVO	CMOS Display Video Output
CI/CSI	Camera Interface/Camera Sideband Interface
CSB	Camera Side Band signals
eMMC*	Embedded MultiMediaCard
ESSP	Enhanced Synchronous Serial Port
FIPS	Federal Information Processing Standards
GPIO	General Purpose Input Output
GPS	Global Positioning Satellite
HDMI	High Definition Multimedia Interface
Host	This term is used synonymously with the processor.
I^2S	The Inter-IC Sound (I^2S) bus is a variant of a general PCM interface in which the SYNC signal is asserted/deasserted for an entire data word. The signal toggles high and low to distinguish between left and right signals. I^2S is an industry standard for supporting stereo DACs and comes in many flavors (differences in clock/data alignment, receive data signal, and so on).
JTAG	Joint Test Action Group
LAN	Local Area Network
TRM	Intel® Platform Controller Hub MP30 Technical Reference Manual
LCD	Liquid Crystal Display
MIPI	Mobile Industry Processor Interface

Table 2-1. Acronyms and Terminology (Sheet 2 of 2)

Acronym	Description
MIPI CSI-2	Mobile Industry Processor Interface organizations Camera Serial Interface 2 specification
MLC	Multiple Layer Cell
MMC	MultiMediaCard
MSI	Message Signaled Interrupt—MSI is a transaction initiated outside the host, conveying interrupt information to the receiving agent through the same path that normally carries read and write commands.
Multi-drop	Indicates that a line goes to several devices on a board. Multi-drop buses make use of multi-drop lines to provide a data transport between multiple devices. Output drivers of devices on a multi-drop line often tri-state to avoid bus contention.
OCP	Open Core Protocol
OCP-IP	Open Core Protocol-International Partnership
OTG	On-The-Go
PCH	Platform Controller Hub
PCM Interface	Basic serial interface providing connectivity processors and audio sources/ sinks. Data format commonly used is PCM though compounded variants are also used. The simplest PCM interface has lines for CLK, SYNC, TxDATA, and RxDATA though 6-wire PCM interfaces with rate-independent transmit and receive subsections are also used. Many variations in PCM interfaces exist (rising-edge clock versus falling-edge clock, positive polarity SYNC versus negative polarity SYNC, bit-length SYNC versus word-length SYNC.
PMIC SPI	Power Management Integrated Controller Serial Peripheral Interface
Pulse Code Modulation (PCM)	Standard technique of representing an audio stream using x-bits sampled uniformly y times a second. Each sample captures the amplitude of the signal at that point in time. PCM samples are sent over serial buses between processors and audio codecs.
RO	Reset Out
SCU	System Controller Unit
SD	Secure Digital Memory Device
SDIO	Secure Digital I/O
SLC	Single Layer Cell
SMK	Scan Matrix Keypad
SoC	System on Chip
SPI	Serial Peripheral Interface
SSP	Synchronous Serial Port
Tri-state	An output is tri-stated when it is not actively driven either high or low. Output drivers on a serial bus are often tri-stated to allow other devices to communicate on the same line. The electrical state of such line is determined by either the output of another driver on the same line (if being actively driven), by a pull-up/pull-down resistor, or by a weak Keeper.
USB	Universal Serial Bus
UTMI	USB Transceiver Macrocell Interface
Voice codec	A voice codec typically contains one (or more ADCs) and one DAC tailored for voice-band operation (8 KHz, 16 KHz, and 26 KHz). The voice codec is a key device during a voice call.
WLAN	Wireless Local Area Network



2.3 Architectural Overview

The Next-Generation Intel® Atom™ processor-based platform consists of 3 chips:

- Intel® Atom™ processor Z6xx series with Integrated Graphics and Memory Controller
- Intel® Platform Controller Hub MP30
- Power Management Integrated Circuit (PMIC)
  - The PMIC has power delivery and audio codec features incorporated into its integrated circuit.

Figure 2-1 is a block diagram that describes the Next-Generation Intel® Atom™ processor-based platform architecture.

The Intel® Platform Controller Hub MP30 is built around the AMBA protocol, an OCP industry standard for interfaces and interconnects. The Intel® Platform Controller Hub MP30 is designed to leverage proven functional blocks from the System-on-Chip (SoC) ecosystem; thus, improving software stability and reducing Time-To-Market (TTM).

To protect personal data and play protected multimedia content, the Intel® Platform Controller Hub MP30 integrates a cryptographic engine. This engine performs high speed decryption of protected content and provides storage and management of cryptographic secret keys. The cryptographic engine also validates software—enabling secure boot in run-time environments through signed firmware and software modules.

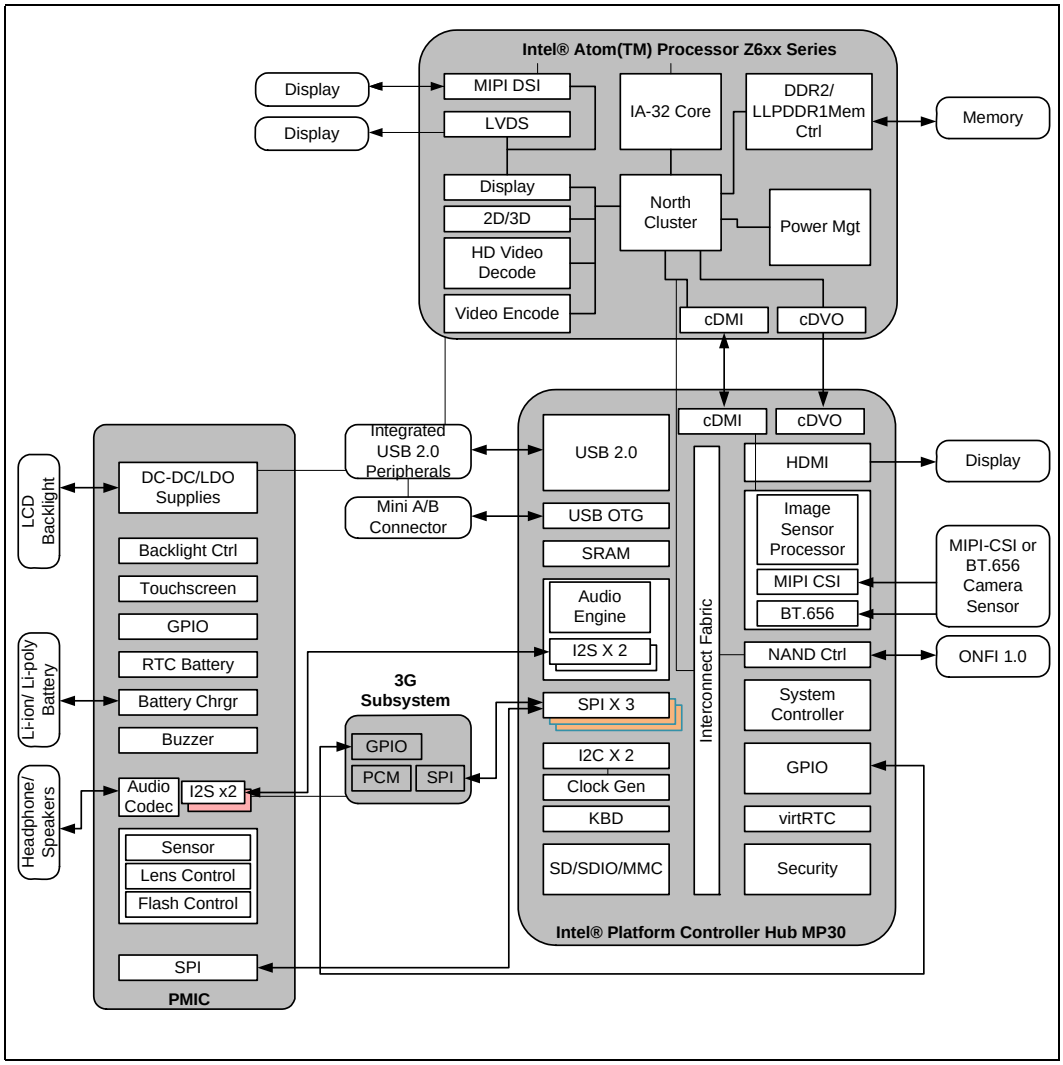
To provide low-cost camera functionality, the Intel® Platform Controller Hub MP30 integrates an image processing array. This array interfaces uses low-cost imaging sensors to perform image enhancement, color correction, color space, and image size conversion.

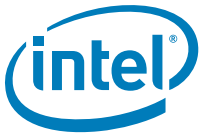
The Intel® Platform Controller Hub MP30 introduces several USB power saving features. For USB devices inside the box, it supports the USB L1 link state and deferring. These power saving features provide a low power link state that quiets the link and the host controller when there are no activities on the USB bus. The Intel® Platform Controller Hub MP30 also allows the end device to reactivate the link when it needs attention. This significantly reduces platform power by eliminating USB polling in an otherwise idle system.

Along with the integrated System Controller Unit (SCU), the Intel® Platform Controller Hub MP30 introduces the new power state, “Always On, Always Connected” (AOAC). This new, very low power standby state, uses the System Controller Unit to quickly awaken the system to respond to system or user events. This provides the perception to the user that the device is never off and never loses network connectivity—even while most of the system is in the standby state. This feature allows Next-Generation Intel® Atom™ processor-based Tablets and Smartphones to have battery standby times of several days while instantly responding to user requests.

To reduce component count and board space the Intel® Platform Controller Hub MP30 integrates the system clock generation functions for the platform. The Intel® Platform Controller Hub MP30 also provides voltage control by means of the PMIC to optimize battery life.

Figure 2-1. Next-Generation Intel® Atom™ Processor-Based Platform Block Diagram





2.4 Intel® Platform Controller Hub MP30 Feature Set

The major features of the Intel® Platform Controller Hub MP30 are:

- CMOS Direct Media Interface (cDMI)—Primary link between the Intel® Atom™ Processor Z6xx Series and the Intel® Platform Controller Hub MP30
- CMOS Display Video Output (cDVO)—Secondary video link from the Intel® Atom™ Processor Z6xx Series to the Intel® Platform Controller Hub MP30
- High Definition Multimedia Interface (HDMI)—Primary display/multimedia output
- Discrete NAND Controller—Primary boot device and storage
- Universal Serial Bus (USB) High Speed (HS)—USB HS device interface
- USB On-The-Go (USB-OTG) 2.0—USB host and peripheral file transfer and synchronization
- Secure Digital Memory Device (SD) and Embedded MultiMediaCard (eMMC*)—secondary storage
- Secure Digital I/O (SDIO)—Supports wireless communication solutions
- Intel® Smart Sound Technology (Intel® SST)
- Mobile Industry Processor Interface (MIPI) CSI-2 and BT.601/BT.656—Still camera and video interface
- Serial Interface and General Purpose I/O (GPIO)
  - GPIO—Flexible I/O voltage (1.8V, 2.5V, and 3.3V)
  - Integrated key pad interface—Supports matrix key pad and Direct Key/ thumbwheel
  - I^2C—Camera control and sensor interface
  - Serial Peripheral Interface (SPI)—Wireless communication and PMIC interface
  - Pulse Code Modulation (PCM)—Transfer encoded voice from PMIC to Intel® Platform Controller Hub MP30 and communication components
  - I^2S/PCM—Support for audio playback and voice communication
- Integrated Clock Generator—To enhance power management control and reduce BOM
- Intel® Smart & Secure Technology (Intel® S&ST)—To improve wireless networking, personal data and platform security
- System Controller Unit (SCU)—Provides platform power management by use of PMIC and management system standby states
- Comprehensive power management
- SRAM—A 256KB block of SRAM used for system boot code and other functions when system DRAM (connected to the Intel® Atom™ Processor Z6xx Series) is unavailable.
  - This allows the processor to extend standby time and enhances battery life.
- Integrated Clocking
  - BCLK—100 MHz differential
  - MIPI CSI-2 Side band clock: 25 MHz
- DFx—Design for Test/Debug
  - Boundary Scan
  - JTAG access to System Controller Unit (SCU) to support power management and boot debug

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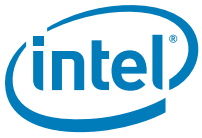


3 Signal Descriptions

3.1 Chapter Contents

This chapter contains detailed information about:

- "Buffer Types and Descriptions"
- "Intel® Platform Controller Hub MP30 Signal and Pin Descriptions"
- "Intel® Platform Controller Hub MP30 Discrete NAND Controller Multiplexing"
- "Intel® Platform Controller Hub MP30 SPI Slave Pin Exchange"
- "Power Rails"
- "Serial I/O and GPIO"

3.2 Buffer Types and Descriptions

Table 3-1 describes various buffers used on the Intel® Platform Controller Hub MP30. CMOS18, CMOS25, and CMOS33 buffers are based on the same CMOSXX buffer. The COMSXX buffer is able to support 1.8V, 2.5V, and 3.3V operation. CMOS18, CMOS25, and CMOS33 represent the default configuration of the buffer set by the SCU Firmware.

Table 3-1. Intel® Platform Controller Hub MP30 I/O Buffer Characteristics

Type	Description
CMOS105	1.05V CMOS buffers
CMOS18	CMOS buffers configured for 1.8V operation
CMOS25	CMOS buffers configured for 2.5V operation
CMOS33	CMOS buffers configured for 3.3V operation
CMOSXX	CMOS buffers that can be configured for 3.3V, 2.5V, or 1.8V operation
HDMI	Buffer compatible with differential High Definition Multimedia Interface
MIPI	Buffer compatible with differential Mobile Industry Processor Interface
USB-OTG	USB-On The Go buffer type
USB-HS	USB Hi-speed buffer type
A	Analog reference or output—May be used as a threshold voltage or for buffer compensation.

3.3 Intel® Platform Controller Hub MP30 Signal and Pin Descriptions

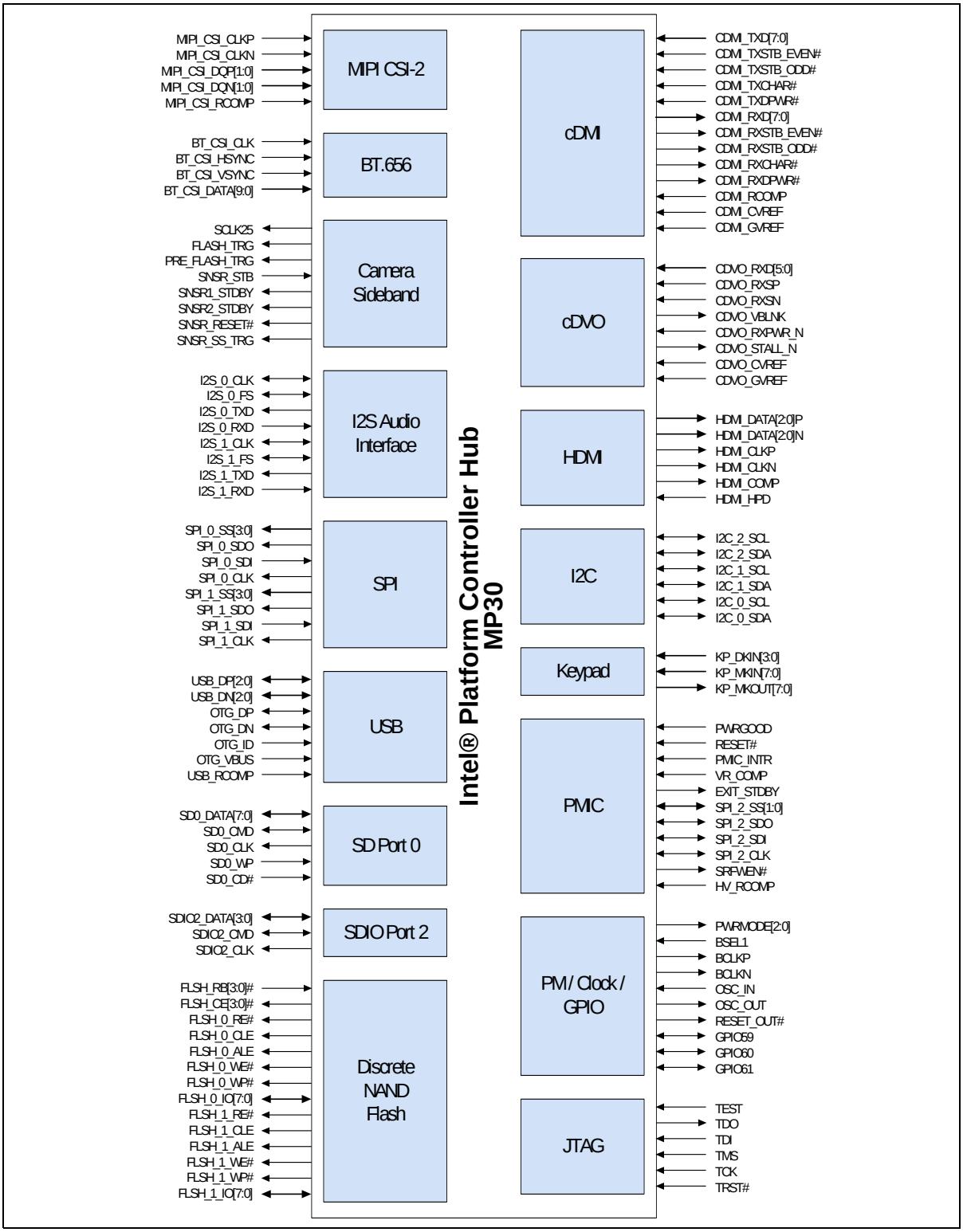
The Intel® Platform Controller Hub MP30 signal and pin descriptions are arranged in functional groups according to their associated interface as shown in Table 3-2.

Each signal description table has the following headings:

- **Signal/Pin:** The name of the signal/pin that supports the interface.
- **Dir., Type:** The buffer direction and type. Buffer direction can be either Input (I), Output (O), or I/O (bi-directional). See Table 3-1 for additional definitions of the different buffer types.
- **Power Rail:** The power plane used to supply power to that signal. See Table 3-26.
- **Reset State:** The state of the pin upon exiting Reset.
- **Description:** A brief explanation of the signal function.

The signals are arranged in functional groups according to their associated interface (see Figure 3-1).

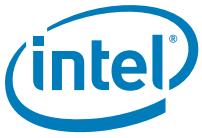
Figure 3-1. Intel® Platform Controller Hub MP30 Signal Diagram



3.3.1 cDMI Interface

Table 3-2. cDMI Interface Signals

Signal/Pin	Dir., Type	Power Rail	Description
CDMI_TXD[7:0]	I CMOS105	PWR_DMIDVO	**CMOS DMI Receive Data** in from the North Complex
CDMI_TXSTB_EVEN#	I CMOS105	PWR_DMIDVO	**CMOS DMI Receive Data Strobe Positive** in from the North Complex
CDMI_TXSTB_ODD#	I CMOS105	PWR_DMIDVO	**CMOS DMI Receive Data Strobe Negative** in from the North Complex
CDMI_TXCHAR#	I CMOS105	PWR_DMIDVO	**CMOS DMI Receive Control** for command or data
CDMI_TXDPWR#	I CMOS105	PWR_DMIDVO	**CMOS DMI Receive Power Management**
CDMI_RCOMP	I A	PWR_DMIDVO	**CMOS Resistor Compensation**: Connect a precision ±1% resistor to PWR_DMIDVO input source. Refer to the *Next-Generation Intel® Atom™ Processor-based Board Design Guide* for specific recommendation.
CDMI_CVREF	I A	PWR_DMIDVO	**VREF for CDMI Receivers**: Connect to 1/2*PWR_DMIDVO resistor divider when CDMI I/O mode is fused to CMOS mode.
CDMI_GVREF	I A	PWR_DMIDVO	**VREF for CDMI strobe signals:** Connect to 1/2*PWR_DMIDVO resistor divider when CDMI I/O mode is fused to CMOS mode.
CDMI_RXD[7:0]	O CMOS105	PWR_DMIDVO	**CMOS DMI Transmit Data** out to North Complex
CDMI_RXSTB_EVEN#	O CMOS105	PWR_DMIDVO	**CMOS DMI Transmit Data Strobe EVEN for CDMI_RXD[7:0]**
CDMI_RXSTB_ODD#	O CMOS105	PWR_DMIDVO	**CMOS DMI Transmit Data Strobe ODD for CDMI_RXD[7:0]**
CDMI_RXCHAR#	O CMOS105	PWR_DMIDVO	**CMOS DMI Control** to indicate either command or data transmits on CDMI_RXD[7:0]
CDMI_RXDPWR#	O CMOS105	PWR_DMIDVO	**CMOS DMI Receive Buffer Power Management control**



3.3.2 cDVO Interface

Table 3-3. cDVO Interface Signals

Signal / Pin	Dir., Type	Power Rail	Description
CDVO_RXD[5:0]	I CMOS105	PWR_DMIDVO	**CMOS Display Link Receive Data**
CDVO_RXSP	I CMOS105	PWR_DMIDVO	**CMOS Display Link Data Strobe, Positive**
CDVO_RXSN	I CMOS105	PWR_DMIDVO	**CMOS Display Link Data Strobe, Negative**
CDVO_VBLNK	O CMOS105	PWR_DMIDVO	**CMOS Display Link Vertical Blank**
CDVO_RXPWR_N	I CMOS105	PWR_DMIDVO	**CMOS Display Link Receive Power Management:** This active low signal is used to gate-off Intel® Platform Controller Hub MP30 input sense amps to save power when asserted.
CDVO_STALL_N	O CMOS105	PWR_DMIDVO	**External Display Pipe Stall:** Indicates the South Complex can no longer receive display data from the North Complex.
CDVO_CVREF	A	PWR_DMIDVO	VREF for cDVO Receivers
CDVO_GVREF	A	PWR_DMIDVO	VREF for cDVO strobe signals

3.3.3 Host Power Management and Clock Interface

Table 3-4. Host Power Management and Clock Interface Signals

Signal / Pin	Dir., Type	Power Rail	Description
PWRMODE[2:0]	O CMOS105	PWR_CPU	**CPU PM:** Grey-code output to allow processor to transition properly on power-up.
BSEL1	I CMOS105	PWR_CPU	**CPU Clock Select:** Host clock frequency select. 0 = 100 MHz 1 = Reserved
BCLKP	O CMOS105	VCC_HCLK	**Positive Host Ref Clock:** Based on value of BSEL1 -0.5% SSC at spread modulation of 32 KHz
BCLKN	O CMOS105	VCC_HCLK	**Negative Host Ref Clock:** Based on value of BSEL1 -0.5% SSC at spread modulation of 32 KHz

3.3.4 HDMI Interface

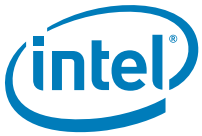
Table 3-5. HDMI Interface Signals

Signal/Pin	Dir., Type	Power Rail	Description
HDMI_DATA[2:0]P	O HDMI	HDMIVCC33	**Positive TMDS Data:** Differential signals for HDMI
HDMI_DATA[2:0]N	O HDMI	HDMIVCC33	**Negative TMDS Data:** Differential signals for HDMI
HDMI_CLKP	O HDMI	HDMIVCC33	**Positive TMDS Clock:** Differential clock output
HDMI_CLKN	O HDMI	HDMIVCC33	**Negative TMDS Clock:** Differential clock output
HDMI_COMP	I A		**HDMI_RCOMP:** Tied to external resistor for output buffer compensation.
HDMI_HPD	I CMOSXX		**HDMI Hot Plug Detect:** 5V-tolerant hot plug detect.

3.3.5 I²C Interface

Table 3-6. I²C Interface Signals

Signal/Pin	Dir., Type	Power Rail	Description
I2C_0_SCL	I/O CMOSXX	PWR_KBDMISC	**I²C Clock:** I²C Serial Clock
I2C_0_SDA	I/O CMOSXX	PWR_KBDMISC	**I²C Data:** I²C Serial Data
I2C_1_SCL	I/O CMOSXX	PWR_CSB	**I2C 1 SDATA:** This signal defaults to a GPIO. It can be programmed to be an I²C port to support imaging/video sensors.
I2C_1_SDA	I/O CMOSXX	PWR_CSB	**I2C 1 SCLK:** This signal defaults to a GPIO. It can be programmed to be an I²C port to support imaging/video sensors.
I2C_2_SCL	I/O CMOSXX	PWR_KBDMISC	**I²C Clock:** I²C Serial Clock Dedicated for use with the HDMI Interface
I2C_2_SDA	I/O CMOSXX	PWR_KBDMISC	**I²C Data:** I²C Serial Data Dedicated for use with the HDMI Interface



3.3.6 MIPI CSI-2 Interface

Table 3-7. MIPI CSI-2 Interface Signals

Signal/Pin	Dir., Type	Power Rail	Description
MIPI_CSI_CLKP	I MIPI	VCC12	**MIPI Clock:** Common to Lanes 0 and 1
MIPI_CSI_CLKN	I MIPI	VCC12	**MIPI Clock:** Common to Lanes 0 and 1
MIPI_CSI_DQP [1:0]	I MIPI	VCC12	**MIPI Positive Data for Lanes 0 and 1**
MIPI_CSI_DQN [1:0]	I MIPI	VCC12	**MIPI Negative Data for Lanes 0 and 1**
MIPI_CSI_RCOMP	I A	VCC12	**MIPI Compensation:** Compensation analog pin for MIPI interface; tie on board to a precision ±1% resistor to V_{CC12}. Refer to the *Next-Generation Intel® Atom™ Processor-based Platform Board Design Guide* for specific recommendations.

3.3.7 BT.601/BT.656 Interface

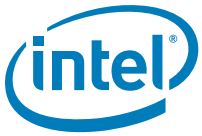
Table 3-8. BT.601/BT.656 Interface Signals

Signal/Pin	Dir., Type	System Rail Name	Description
BT_CSI_CLK	I CMOSXX	PWR_BT	**Camera I/F BT.656 Clock Input**
BT_CSI_HSYNC	I CMOSXX	PWR_BT	**Camera BT.656 Horizontal Synchronization**
BT_CSI_VSYNC	I CMOSXX	PWR_BT	**Camera BT.656 Vertical Synchronization**
BT_CSI_DATA[9:0]	I CMOSXX	PWR_BT	**Camera 10b Data Input**

3.3.8 Camera Sideband Interface

Table 3-9. Camera Side Band Signals

Signal	Dir., Type	Power Rail	Description
SCLK25	O CMOSXX	PWR_CSB	**SCLK25** is a 25 MHz clock supply to camera Sensor 1 and Sensor 2. The same clock signal can be shared between the two sensors. The PLL on the camera sensor uses the SCK25 to generate the target pixel clock.
FLASH_TRG	O CMOSXX	PWR_CSB	**Flash Trigger:** This signal is asserted by the Camera Interface in the Intel® Platform Controller Hub MP30 indicating that a full frame is about to be captured. The Flash fires when it detects an assertion of this signal. The signal deasserts to revert the flash into charge buildup mode. This signal can be used to control White LEDs. The assertion of the signal causes the LEDs to light up, and deassertion of this signal turns the LEDs off. The Camera Interface will adjust the pulse width and timing depending on whether the signal is driving a Flash or an LED. For details, refer to the ISP_FLASH register in the camera chapter of the *Intel® Platform Controller Hub MP30 Technical Reference Manual*.
PRE_FLASH_TRG	O CMOSXX	PWR_CSB	**Pre Flash Trigger:** The Camera Interface asserts this signal to light up a pilot lamp prior to firing the flash to support prevent red-eye reduction.
SNSR_STB	I CMOSXX	PWR_CSB	**Sensor Strobe:** The Sensor asserts this signal to indicate the start of a full frame, when it is configured in the single shot mode, or to indicate a flash exposed frame for flash synchronization. Some sensors may not support this signal, this signal can be a N/C. Single shot mode might be supported by the sensor, but CI will have to synchronize to BT_CSI_Vsync.
SNSR1_STDBY	O CMOSXX	PWR_CSB	**Sensor Standby 1:** This signal is used to control Sensor 1 Standby power states.
SNSR2_STDBY	O CMOSXX	PWR_CSB	**Sensor Standby 2:** This signal is used to control Sensor 2 Standby power states.
SNSR_RESET#	O CMOSXX	PWR_CSB	**Sensor Reset:** This signal is active low and shared by both sensors.
SNSR_SS_TRG	O CMOSXX	PWR_CSB	**Sensor Single Shot Trigger:** This signal is used to request of the sensor, when configured in single shot mode, that the next frame (or a programmable delay later, if provided) be captured as a full frame.



3.3.9 USB Interface

Table 3-10. USB Interface Signals

Signal/Pin	Dir., Type	Power Rail	Description
USB_DP[2:0]	I/O USB-HS	VCCA_USB33 VCCA_USB25	**USB 2.0 Data Positive Data (D+):** In USB 2.0 mode this is the positive differential data signal.
USB_DN[2:0]	I/O USB-HS	VCCA_USB33 VCCA_USB25	**USB 2.0 Data Negative (D-):** In USB 2.0 mode, this is the negative differential data signal.
OTG_DP	I/O USB-OTG	VCCA_USB33 VCCA_USB25	**OTG Data Positive (D+):** OTG port Data Positive.
OTG_DN	I/O USB-OTG	VCCA_USB33 VCCA_USB25	**OTG Data Negative (D-):** OTG port Data Negative.
OTG_ID	I CMOSXX	VCCA_USB33	**ID:** Determine the initial port status (master or slave) to determine the port that owns the initialization.
OTG_VBUS	I A	n/a	**VBUS:** Connect to GND.
USB_RCOMP	I A	n/a	**Resistor Compensation:** Connect to a precision ±1% resistor to GND. Refer to the Next-Generation *Intel® Atom™ Platform-based Board Design Guide* for specific recommendation.

3.3.10 SDIO Port 2 Interface

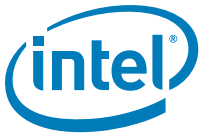
Table 3-11. SDIO Port 2 Interface Signals

Signal/Pin	Dir., Type	Power Rail	Description
SDIO2_DATA[3:0]	I/O CMOSXX	PWR_SDIO2	**SDIO Data:** Four bi-directional data signals.
SDIO2_CMD	I/O CMOSXX	PWR_SDIO2	**SDIO CMD:** Bi-directional command response signal.
SDIO2_CLK	O CMOSXX	PWR_SDIO2	**SDIO CLK:** Active high clock that is CMOS level and interfaces to internal communication ports.

3.3.11 SD/eMMC* Port 0 Interface

Table 3-12. SD/eMMC* Port 0 Interface Signals

Signal/Pin	Dir., Type	Power Rail	Description
SD0_DATA[7:0]	I/O CMOSXX	PWR_SD0	**SD Port Data:** By default, after power-up, only SDIO_DATA[0] is used for data transfer. A wider data bus can be configured for data transfer. **MMC Port Data:** These signals operate in push-pull mode. The MMC card includes internal pull-ups for all data lines. By default, after power-up, only MMC_DATA[0] is used for data transfer. A wider data bus can be configured for data transfer.
SD0_CMD	I/O CMOSXX	PWR_SD0	**SD Port Command:** This signal is used for card initialization and transfer of commands. **MMC Port Command:** This signal is used for card initialization and transfer of commands. It has two modes—open-drain for initialization and push-pull for fast command transfer.
SD0_CLK	O CMOSXX	PWR_SD0	**SD Port Clock:** With each cycle of this signal a one-bit transfer on the command and each data line occurs. It is generated by the Intel® Platform Controller Hub MP30, at a maximum frequency of 25 MHz. **MMC Port Clock:** With each cycle of this signal a one-bit transfer on the command and each data line occurs. It is generated by the Intel® Platform Controller Hub MP30, at a maximum frequency of 52 MHz.
SD0_WP	I CMOSXX	PWR_SD0	**SD Port Write Protect:** Active high when a card does not want to accept writes. **MMC Port Write Protect:** Active high when a card is not accepting writes.
SD0_CD#	I CMOSXX	PWR_SD0	**SD Port Card Detect:** Active low when a card is present. Floating (pulled high) when a card is not present. This signal is attached to the SDIO connector. **MMC Port Card Detect:** Active low when a card is present. Floating (pulled high) when a card is not present. This signal is attached to the MMC connector.



3.3.12 SD Port 1 Interface

SD Port 1 is multiplexed with discrete NAND controller port 1. See section Section 3.4.

3.3.13 Discrete NAND Flash Interface

Table 3-13. Discrete NAND Flash Interface Signals

Signal/Pin	Dir., Type	Power Rail	Description
FLSH_RB[3:0]#	I CMOSXX	PWR_FLASH0	**NAND FLASH Port Run/Busy#:** The Ready/ Busy signal indicates the target status. When low, the signal indicates that one or more LUN operations are in progress.
FLSH_[1:0]_RE#	O CMOSXX	PWR_FLASH1 PWR_FLASH0	**NAND FLASH Port Read Enable:** Valid for Standard Flash ONFI interface. Active low read enable signal.
FLSH_[3:0]_CE#	O CMOSXX	PWR_FLASH0	**NAND FLASH Port Chip Enable:** Active low chip enable signal used to select a target.
FLSH_[1:0]_CLE	O CMOSXX	PWR_FLASH1 PWR_FLASH0	**NAND FLASH Port Command Latch Enable:** When asserted, the command on FLSH_IO is latched on the rising edge of FLSH_WE#.
FLSH_[1:0]_ALE	O CMOSXX	PWR_FLASH1 PWR_FLASH0	**NAND FLASH Port Address Latch Enable:** Address Latch Enable is used to load address into target. When asserted, the address is loaded on the rising edge of FLSH_WE#.
FLSH_[1:0]_WE#	O CMOSXX	PWR_FLASH1 PWR_FLASH0	**NAND FLASH Port Write Enable:** Valid only for Standard Flash ONFI interface. These are active low write enable signals.
FLSH_[1:0]_WP#	O CMOSXX	PWR_FLASH1 PWR_FLASH0	**NAND FLASH Port Write Protect:** Write Protect disables the Flash array program and erase operations.
FLSH_1_IO[7:0]	I/O CMOSXX	PWR_FLASH1	**NAND FLASH Port Address/Data:** Eight (8)-bit wide bi-directional bus for transferring address, command, and data to and from the device. These signals transfer the upper byte when instantiated in a two x8 configuration at the platform level.
FLSH_0_IO[7:0]	I/O CMOSXX	PWR_FLASH0	**NAND FLASH Port Address/Data:** Eight (8)-bit wide bi-directional bus for transferring address, command, and data to and from the device. These signals transfer the lower byte when instantiated in a two x8 configuration at the platform level.

3.3.14 I²S Interface

The I2S0 is dedicated for voice call interface and the I2S1 is dedicated for audio/music playback.

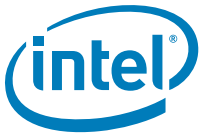
Table 3-14. I²S Interface Signals

Signal/Pin	Dir., Type	Power Rail	Description
I2S_0_CLK	I/O CMOSXX	PWR_I2S	**I²S 0 Clock:** This signal can be configured either as an input or an output. It is configured as an input to support voice PCM payload.
I2S_0_FS	I/O CMOSXX	PWR_I2S	**I²S 0 Frame Sync:** This signal can be configured either as an input or an output.
I2S_0_TXD	O CMOSXX	PWR_I2S	**I²S 0 Transmit Data:** Output data line is actively driven or tri-state.
I2S_0_RXD	I CMOSXX	PWR_I2S	**I²S 0 Receive Data:** Input data line
I2S_1_CLK	I/O CMOS18	PWR_PMIC	**I²S 1 Clock:** This signal can be configured either as an input or an output. it is configured as an input to support audio PCM payload.
I2S_1_FS	I/O CMOS18	PWR_PMIC	**I²S 1 Frame Sync:** This signal can be configured either as an input or an output.
I2S_1_TXD	O CMOS18	PWR_PMIC	**I²S 1 Transmit Data:** Output data line is actively driven or tri-stated.
I2S_1_RXD	I CMOS18	PWR_PMIC	**I²S 1 Receive Data:** Input data line

3.3.15 Analog Clock Interface

Table 3-15. Analog Clock Interface Signals

Signal/Pin	Dir., Type	Power Rail	Description
OSC_IN	I CMOS105	VCCAHPLL	**Oscillator Input:** This signal provides input to Pierce oscillator from 25-MHz crystal.
OSC_OUT	O CMOS105	VCCAHPLL	**Oscillator Output:** This is the output of Pierce oscillator and should be connected to the crystal.



3.3.16 JTAG Interface

Table 3-16. JTAG Interface Signals

Signal	Dir., Type	Power Rail	Description
TEST	I CMOS105	PWR_CPU	**TEST:** When asserted, the component is put into TEST modes in specific combinations. Keeping an active high termination is not required.
TDO	O CMOS105	PWR_CPU	**JTAG Test Data Output:** This serial output is for test instruction and data from the test logic.
TDI	I CMOS105	PWR_CPU	**JTAG Test Data Input:** This signal receives serial test instruction and data of test logic.
TMS	I CMOS105	PWR_CPU	**JTAG Test Mode Select:** This signal is decoded by the TAP controller to control test operations.
TCK	I CMOS105	PWR_CPU	**JTAG Test Clock:** Clock for the test logic.
TRST#	I CMOS105	PWR_CPU	**JTAG Test Reset:** Asynchronous initialization of the TAP controller.

3.3.17 Reset Out Interface

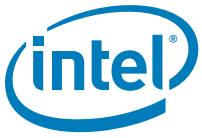
Table 3-17. Reset Out Interface Signals

Signal/Pin	Dir., Type	Power Rail	Description
RESET_OUT#	O CMOS18	PWR_PMIC	**RESET_OUT:** A programmable delayed reset for platform components.

3.3.18 PMIC Interface

Table 3-18. PMIC Interface Signals

Signal/Pin	Dir., Type	Power Rail	Description
PWRGOOD	I CMOS18	PWR_PMIC	**POWER GOOD:** PMIC asserts this signal to indicate that all initial power rails to the Intel® Platform Controller Hub MP30 are valid. Assertion of PWRGOOD also means that VCCA_OSC has been valid for at least 30 µs. The Intel® Platform Controller Hub MP30 will remain off until this signal is asserted.
RESET#	I CMOS18	PWR_PMIC	**Active Low Hard Reset for Intel® Platform Controller Hub MP30:** This signal is driven by the PMIC.
PMIC_INTR	I CMOS18	PWR_PMIC	**PMIC Interrupt:** Active high—Attach this to PMIC IRQ9.
VR_COMP	I CMOS18	PWR_PMIC	V**oltage Regulator Complete:** Active high indication from the PMIC that the requested voltage regulation request over SPI has been completed.
EXIT_STDBY	O CMOS18	PWR_PMIC	**EXIT Standby:** When asserted, the PMIC should exit the AOAC Standby settings for regulating the platform supplies.
SPI_2_SS[1:0]	I/O CMOS18	PWR_PMIC	**SPI 2 Slave Select(s):** The second slave select is reserved for additional PMIC load.
SPI_2_SDO	I/O CMOS18	PWR_PMIC	**SPI Port 2 Serial Data Out:** Defaults to output
SPI_2_SDI	I/O CMOS18	PWR_PMIC	**SPI Port 2 Serial Data In:** Defaults to input
SPI_2_CLK	I/O CMOS18	PWR_PMIC	**SPI Port 2 Clock:** Defaults to output
SRFWEN#	O CMOS18	PWR_PMIC	**Memory Self-Refresh:** The Intel® Platform Controller Hub MP30 asserts this SRFWEN# after the Intel® Atom™ processor Z6xx series sends the ACK_S0i3 to force DDR into self-refresh.
HV_RCOMP	I A	n/a	**HVIO Buffer RCOMP:** Tie to a precision ±1% resistor to ground—Please refer to the *Next-Generation Intel® Atom™ Processor-based Board Design Guide* for specific recommendations.



3.3.19 SPI Port 0 Interface

Table 3-19. SPI Port 0 Interface Signals

Signal	Dir., Type	Power Rail	Description
SPI_0_SS[3:0]	O CMOSXX	PWR_SPI	**SPI 0 Slave Select(s):** active low; output from master A total of 4 slaves are supported on this SPI port.
SPI_0_SDO	O CMOSXX	PWR_SPI	**SPI Port 0 Serial Data Out:** Connects to MOSI
SPI_0_SDI	I CMOSXX	PWR_SPI	**SPI Port 0 Serial Data In:** Connects to MISO
SPI_0_CLK	O CMOSXX	PWR_SPI	**SPI Port 0 Clock:** Serial Clock (output from master)

3.3.20 SPI Port 1 Interface

Table 3-20. SPI Port 1 Interface Signals

Signal	Dir., Type	Power Rail	Description
SPI_1_SS[3:0]	O CMOSXX	PWR_SPI	**SPI_1_Slave Select(s):** active low; output from master A total of 4 slaves are supported by this SPI port.
SPI_1_SDO	O CMOSXX	PWR_SPI	**SPI Port 1 Serial Data Out:** Connects to MOSI
SPI_1_SDI	I CMOSXX	PWR_SPI	**SPI Port 1 Serial Data In:** Connects to MISO
SPI_1_CLK	O CMOSXX	PWR_SPI	**SPI Port 1 Clock:** Serial Clock (output from master)

Note: The SDI/SDO convention requires that the master SDO be connected to the slave SDI, and the slave SDO be connected to the master SDI.

3.3.21 Scan Matrix Keypad Interface

Table 3-21. Scan Matrix Keypad Interface Signals

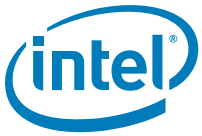
Signal	Dir., Type	Power Rail	Description
KP_DKIN[3:0]	I CMOSXX	PWR_KBDMISC	**Direct Key Inputs:**
KP_MKIN[7:0]	I CMOSXX	PWR_KBDMISC	**Matrix Key Returns:**
KP_MKOUT[7:0]	O CMOSXX	PWR_KBDMISC	**Matrix Key Output:**

NOTE: Some of these pins may also serve as straps for Intel® Reference Board ID. Use with caution when leveraging Intel designs.

3.3.22 Miscellaneous GPIO Interface

Table 3-22. Miscellaneous GPIO Interface Signals

Signal	Dir., Type	Power Rail	Description
GPIO59	I/O CMOSXX	PWR_KBDMISC	**Spare GPIOs:** Defaults to GPIO. This pin shares the power plane with I2C_0.
GPIO60 / SPI_IRQ#	I/O CMOSXX	PWR_KBDMISC	**GPIOs:** This GPIO is used as SPI_IRQ# for the communication devices. This pin shares the power plane with I2C_0.
GPIO61	I/O CMOSXX	PWR_KBDMISC	**Spare GPIOs:** Defaults to GPIO. This pin shares the power plane with I2C_0.



3.4 Intel® Platform Controller Hub MP30 Discrete NAND Controller Multiplexing

3.4.1 SD Port 1 and Flash Channel 1 Pin Multiplexing

Table 3-23. SD Port 1 and Flash Channel 1 Pin Multiplexing

SDIO Signal	NAND Flash Signal	Power Well	Pin Count
SD_1_DATA[7:0]	FLSH_1_IO[7:0]	PWR_FLSH1	8
SD_1_CMD	FLSH_1_ALE	PWR_FLSH1	1
SD_1_CLK	FLSH_1_CLE	PWR_FLSH1	1
SD_1_WP	FLSH_1_WP#	PWR_FLSH1	1
SD_1_CD#	FLSH_1_WE#	PWR_FLSH1	1

3.5 Intel® Platform Controller Hub MP30 SPI Slave Pin Exchange

3.5.1 I2S0 Pin Exchange for SPI Slave Functionality

Table 3-24. I2S0 Pin Exchange for SPI Slave Functionality

I2S0 Signal	SPI Slave Signal	Power Well	Pin Count
I2S_0_CLK	SPI_3_CLK	PWR_I2S	1
I2S_0_SYNC	SPI_3_SS	PWR_I2S	1
I2S_0_TXD	SPI_3_SDI (MISO)	PWR_I2S	1
I2S_0_RXD	SPI_3_SDO (MOSI)	PWR_I2S	1

3.6 Power Rails

3.6.1 Power Rail Type

This section defines the power state and power level options.

Table 3-25. Power Rail Types

Rail Type	Description
F	**Fixed:** Voltage level is fixed—based on I/O family.
AON	**Always ON**: The voltage level must always be on for the component to operate safely and reliably.
S	**Selectable**: Voltage can be selected at the platform level, that is, low-speed I/O support for 1.8-, 2.5-, and 3.3-Volt levels.
V	**Variable:** Variable supplies are negotiable supply levels; that is, with SDIO the specification supports dynamic voltage management and the Intel® Platform Controller Hub MP30 will support negotiated from 3.3V to 1.8V.
SbF	**Selectable but Fixed:** I/O family or segment supports multi-termination levels; however, the current POR platform will only use one "fixed" level. This reduces electrical validation required at component and platform level.
VbF	**Variable but Fixed:** I/O family or segment supports variable, multi-term level; however, the current POR platform will only use one "fixed" level. This reduces the logic and electrical validation required at component and platform level.

3.6.2 Power Rail Descriptions

3.6.2.1 Core and I/O Power

This section describes the power signals and power states of each power signal.

Table 3-26. Core and I/O Power Signals (Sheet 1 of 2)

Signal	Type	Signal Group	Description
VCC12	F, AON	Core/MIPI	**1.2V Core and MIPI Supply:** Always on, required for the Intel® Platform Controller Hub MP30 power-on.
PWR_CPU	F	Host PM/ JTAG	**1.05V Supply for Host PM and JTAG Signals**
VCC_HCLK	F	Host BCLK	**Supply for Host Clock Driver.**
VCC_HCLK33	F	Host BCLK	**3.3V Supply for Host Clock PLL**
PWR_DMIDVO	F	CDMI	**1.05V Supply: For cDMI Output Drivers**
PWR_ADMIDVO	F, AON	CDMI, CDVO	**1.8V Supply:** For cDMI Receive buffer
VCCHDMI	F	HDMI	**1.2V HDMI Supply**
VCCHDMIBG	F	HDMI	**3.3V HDMI Display Bandgap Supply**
VCCA_USB33	F	USB OTG	**3.3V USB Supply**
VCCA_USB25	F	USB	**2.5V USB Supply**

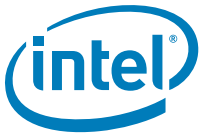


Table 3-26. Core and I/O Power Signals (Sheet 2 of 2)

Signal	Type	Signal Group	Description
PWR_SD0	V	SD/eMMC Port 0	**SDIO/MMC Port 0 Supply:** Dynamically negotiated from 3.3V to 1.8V based on the device.
PWR_SDIO2	VbF	SDIO_2	**SDIO Supply:** Typically 3.3V
PWR_FLSH0	S	NAND	**NAND Supply:** Typically 3.3V or 1.8V.
PWR_FLSH1	S	NAND, Storage Port1	**NAND and SDIO/MMC Port 1 Supply:** Typically 3.3V or 1.8V.
PWR_BT	SbF	BT.656	**BT.656 Camera Interface Supply:** Targeted for 2.5V, but 1.8V-operation possible.
PWR_PMIC	SbF	PMIC	**PMIC and SPI2 Interface Supply:** Powers SPI interface to PMIC. Required for the Intel® Platform Controller Hub MP30 power-on.
PWR_I2S	S	I2S_0	**I2S_0 (Voice) Interface Supply:** Typically 3.3V or 1.8V
PWR_CSB	S	CSB	**Camera Sideband Interface Supply:** Typically 1.8V.
PWR_SPI	S	SPI0, SPI1	**SPI Port 0 and Port 1 Supply**
PWR_KBDMISC	S	KBD, MISC	**Keypad and Miscellaneous GPIO Supply:** Typically 3.3V or 1.8V.

3.6.2.2 PLL/Bandgap Power and Ground

Table 3-27. PLL/Bandgap Power and Ground Signals

Signal	Type	Signal Group	Description
VCCAHPLL	F, AON	Host PM, Analog CLK	1.2V analog supply for oscillator and host PLL
VCCADPLL	F, AON	Display PLL	1.2V dedicated analog supply for display PLL

3.7 Serial I/O and GPIO

The Intel® Platform Controller Hub MP30 provides 62 highly-multiplexed General Purpose I/O (GPIO) pins for use in generating and capturing application-specific input and output signals. Each pin can be programmed as an output, an input, or as a bi-directional for certain alternate functions. Refer to Table 3-28 for the default GPIO usage.

Note: Refer to the *Intel® Platform Controller Hub Technical Reference Manual* for the GPIO pin multiplexing.

Table 3-28. GPIO Alternate Function Mapping (Sheet 1 of 2)

GPI Pin	Pin Name	Alternate Function 1 (In)	Alternate Function 1 (Out)
0	GPIO[0] PWRGOOD		
1	GPIO[1]/RESET#		
2	GPIO[2] PMIC_INTR		
3	GPIO[3] VR_COMP		
4	GPIO[4] EXIT_STANDBY		
5	GPIO[5]		SPI_2_SS[0]
6	GPIO[6]		SPI_2_SS[1]
7	GPIO[7]		SPI_2_SDO
8	GPIO[8]	SPI_2_SDI	
9	GPIO[9]		SPI_2_CLK
10	GPIO[10]		SPI_1_SS[0]
11	GPIO[11]		SPI_1_SS[1]
12	GPIO[12]		SPI_1_SS[2]
13	GPIO[13]		SPI_1_SS[3]
14	GPIO[14]		SPI_1_SDO
15	GPIO[15]	SPI_1_SDI	
16	GPIO[16]		SPI_1_CLK
17	GPIO[17]		SPI_0_SS[0]
18	GPIO[18]		SPI_0_SS[1]
19	GPIO[19]		SPI_0_SS[2]
20	GPIO[20]		SPI_0_SS[3]
21	GPIO[21]		SPI_0_SDO
22	GPIO[22]	SPI_0_SDI	
23	GPIO[23]		SPI_0_CLK
24	GPIO[24]	KP_MKIN[0]	
25	GPIO[25]	KP_MKIN[1]	
26	GPIO[26]	KP_MKIN[2]	
27	GPIO[27]	KP_MKIN[3]	
28	GPIO[28]	KP_MKIN[4]	
29	GPIO[29]	KP_MKIN[5]	
30	GPIO[30]	KP_MKIN[6]	
31	GPIO[31]	KP_MKIN[7]	
32	GPIO[32]		KP_MKOUT[0]
33	GPIO[33]		KP_MKOUT[1]
34	GPIO[34]		KP_MKOUT[2]

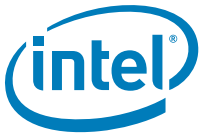


Table 3-28. GPIO Alternate Function Mapping (Sheet 2 of 2)

GPI Pin	Pin Name	Alternate Function 1 (In)	Alternate Function 1 (Out)
35	GPIO[35]		KP_MKOUT[3]
36	GPIO[36]		KP_MKOUT[4]
37	GPIO[37]		KP_MKOUT[5]
38	GPIO[38]		KP_MKOUT[6]
39	GPIO[39]		KP_MKOUT[7]
40	GPIO[40]	KP_DKIN[0]	
41	GPIO[41]	KP_DKIN[1]	
42	GPIO[42]	KP_DKIN[2]	
43	GPIO[43]	KP_DKIN[3]	
44	GPIO[44]		SCLK25
45	GPIO[45]		FLASH_TRG
46	GPIO[46]		PRE_LIGHT_TRG
47	GPIO[47]	SNSR_STB	
48	GPIO[48] SNSR_STDBY_1		
49	GPIO[49] SNSR_STDBY_2		
50	GPIO[50] SNSR_RESET#		
51	GPIO[51] SNSR_SS_TRG		
52	GPIO[52]	I2C_2_SDA	I2C_2_SDA
53	GPIO[53]	I2C_2_SCL	I2C_2_SCL
54	GPIO[54]	I2C_1_SDA	I2C_1_SDA
55	GPIO[55]	I2C_1_SCL	I2C_1_SCL
56	GPIO[56]	I2C_0_SDA	I2C_0_SDA
57	GPIO[57]	I2C_0_SCL	I2C_0_SCL
58	GPIO[58] SRFWEN#		
59	GPIO[59]		
60	GPIO[60]		
61	GPIO[61]		

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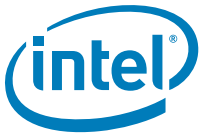


4 Electrical Specifications

4.1 Chapter Contents

This chapter contains information about:

- "Intel® Platform Controller Hub MP30 Power Net Characteristics"
- "Intel® Platform Controller Hub MP30 DC Characteristics"
- "Intel® Platform Controller Hub MP30 Power Sequencing Timing"

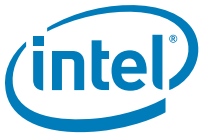
4.2 Intel® Platform Controller Hub MP30 Power Net Characteristics

Table 4-1. Power Net Characteristics (Sheet 1 of 2)

Power Rail	Parameters	Input (V)	Tolerance (%)	Peak Sustained Current (ma)	Idle Current (µA)	S0	S0i1	S0i3
VCC12	1.2V Core and MIPI Supply: Always on, required for Intel® Platform Controller Hub MP30 power-on.	1.2	+5/-5	210	—	ON	ON	ON
PWR_CPU	1.05V Supply for Host PM and JTAG Signals	1.05	+5/-5	1	0.01	ON	ON	OFF
VCC_HCLK	Supply for Host Clock Driver.	1.05	+5/-5	4.1	—	ON	ON	OFF
VCC_HCLK33	3.3V Supply for Host Clock PLL	3.3	+5/-5	1.2	—	ON	ON	ON
PWR_DMIDVO	1.05V Supply for cDMI Output Drivers	1.05	+5/-5	174	14.7	ON	ON	OFF
PWR_ADMIDVO	1.8V Supply for cDMI Receivers	1.8	+5/-5	5	0	ON	ON	ON
VCCHDMI	1.2V Supply DMI Supply	1.2	+5/-5	13.8	5	ON	ON	ON
HDMIVCC3	3.3V HDMI Supply	3.3	+5/-5	—	—	ON	ON	ON
VCCHDMIBG	3.3V HDMI Bandgap Supply	3.3	+5/-5	3.62	0	ON	ON	ON
VCCA_USB33	3.3V USB Supply	3.3	+5/-5	6	11	ON	ON	ON
VCCA_USB25	2.5V USB Supply	2.5	+5/-5	120	1.72	ON	ON	ON
PWR_SD0	SDIO/MMC Port 0 Supply: dynamically negotiated from 3.3V to 1.8V based on device type.	1.8	+5/-5	—	—	ON	ON	ON
		3.3	+5/-5	7.5	0.03	ON	ON	ON

Table 4-1. Power Net Characteristics (Sheet 2 of 2)

Power Rail	Parameters	Input (V)	Tolerance (%)	Peak Sustained Current (ma)	Idle Current (µA) (Contin	S0	S0i1	S0i3
PWR_SDIO2	SDIO Supply: Typically 3.3V	1.8	+5/-5	—	—	ON	ON	ON
		3.3	+5/-5	5	0.03	ON	ON	ON
PWR_FLSH0	NAND Supply: Typically 3.3V or 1.8V	1.8	+5/-5			ON	ON	ON
		3.3	+5/-5	40	0.08	ON	ON	ON
PWR_FLSH1	NAND and SDIO/MMC Port 1 Supply: Typically 3.3V or 1.8V	1.8	+5/-5	—	—	ON	ON	ON
		3.3	+5/-5	33	0.08	ON	ON	ON
PWR_BT	BT.656 Camera Interface Supply: Targeted for 2.5V, but 1.8V operation is possible	2.5	+5/-5	—	—	ON	ON	ON
PWR_PMIC	PMIC and SPI2 Interface Supply: Powers SPI interface to PMIC. Required for Intel® Platform Controller Hub MP30 power-on	1.8	+5/-5	1	0.01	ON	ON	ON
PWR_I2S	I2S_0 (Voice) Interface Supply	1.8	+5/-5	—	—	ON	ON	ON
		3.3	+5/-5	1	0.02	ON	ON	ON
PWR_CSB	Camera Sideband Interface Supply: Typically 1.8V	1.8	+5/-5	—	—	ON	ON	ON
		3.3	+5/-5	1	0.01	ON	ON	ON
PWR_SPI	SPI Port 0, Port 1 Supply	1.8	+5/-5	—	—	ON	ON	ON
		3.3	+5/-5	5	0.03	ON	ON	ON
PWR_KBDMISC	Keyboard and Miscellaneous GPIO Supply: Typically 3.3V or 1.8V.	1.8	+5/-5	—	—	ON	ON	ON
		3.3	+5/-5	1	10	ON	ON	ON
VCCAHPLL	Dedicated analog supply for oscillator and host PLL	1.2	+5/-5	10	0.01	ON	ON	ON
VCCADPLL	Dedicated analog supply for display PLL	1.2	+5/-5	20	0.01	ON	ON	ON



4.3 Intel® Platform Controller Hub MP30 DC Characteristics

This section documents the DC characteristics of the following Intel® Platform Controller Hub MP30 signal groups and interfaces.

4.3.1 cDMI/cDVO

Table 4-2. cDMI/cDVO DC Characteristics

Symbol	Parameter	Minimum	Nominal	Maximum	Unit
CMOS cDMI					
V_{OH}	Output High Voltage	0.9*PWR_DMIDVO	PWRDMIDVO	1.1*PWR_DMIDVO	V
V_{OL}	Output Low Voltage	0	0	0.1*PWR_DMIDVO	V
V_{IH}	Input High Voltage	1/2*PWR_DMIDVO+0.1	PWRDMIDVO	PWR_DMIDVO+0.1	V
V_{IL}	Input Low Voltage	-0.1	0	1/2*PWR_DMIDVO -0.1	V
I_{LEAK}	Input Leakage Current	—	—	10	µA
C_{IN}	Input Capacitance	—	1.5	—	pF

4.3.2 HDMI

Table 4-3. HDMI DC Characteristics

Symbol	Parameter	Minimum	Nominal	Maximum	Unit
A_{VCC}	Nominal High-level Signal Voltage	—	3.3	—	V
V_H	Single-ended High-level Output	A_{VCC} – 10mV	—	A_{VCC} + 10mV	V
V_L	Single-ended Low-level Output	A_{VCC} – 600mV	—	A_{VCC} – 400mV	V
V_{SWING}	Single-ended Output Swing Voltage	400	—	600	mV
V_{OFF}	Single-ended Standby (Off) Output Voltage	A_{VCC} – 1V	—	A_{VCC} + 10mV	

4.3.3 MMC / eMMC*

Table 4-4. MMC Power Supply—High Voltage MultiMediaCard

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{DD}	Supply voltage	2.7	3.6	V	
V_{SS}	Supply voltage	-0.5	0.5	V	

Table 4-5. MMC Power Supply—Dual Voltage MultiMediaCard

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{DDL}	Supply voltage (low voltage range)	1.7	1.95	V	1.95–2.7V is not supported
V_{DDH}	Supply voltage (high voltage range)	2.7	3.6	V	
V_{SS}	Supply voltage	-0.5	0.5	V	

Table 4-6. eMMC* Power Supply—High Voltage MultiMediaCard

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Supply voltage (NAND)	2.7	3.6	V	
		1.7	1.95	V	
V_{CCQ}	Supply voltage (I/O)	-0.5	0.5	V	
		1.7	1.95	V	

4.3.3.1 eMMC* Bus Signal Line Load

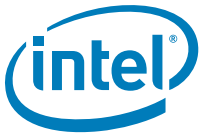
The total capacitance C_L of each line of the MultiMediaCard bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself, and the capacitance C_{CARD} of the card connected to this line,

$$C_L = C_{HOST}+C_{BUS}+C_{CARD}$$

and requiring the sum of the host and bus capacitances not to exceed 20 pF.

Table 4-7. eMMC* Capacitance

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
RCMD	Pull-up resistance for CMD	4.7	—	100	KΩ	to prevent bus floating
RDAT	Pull-up resistance for DAT	50	—	100	KΩ	to prevent bus floating
RINT	Internal pull-up resistance DAT1–DAT7	50	—	150	KΩ	to prevent unconnected lines floating
CL	Bus signal line capacitance	—	—	30	pF	Single card
CMICRO	Single card capacitance	1.7	—	1.95	pF	For MMCmicro
CMOBILE		—	—	30		For MMCmobile and MMCplus
CBGA		—	7	12		For BGA
	Maximum signal line capacitance	—	—	16	nH	fpp ≤ 52 MHz



4.3.3.2 eMMC* Bus Signal Levels

To meet the requirements of the JEDEC specification JESD8-1A, the card input and output voltages shall be within the following specified ranges for any V_{DD} of the allowed voltage range.

Table 4-8. eMMC* Push-Pull Mode Bus Signal Level—High Voltage MultiMediaCard

Symbol	Parameter	Minimum	Maximum	Units	Notes
V_{OH}	Output High Voltage	0.75*VDD	—	V	IOH=–100 µA VDD minimum
V_{OL}	Output Low Voltage	—	0.125*VDD	V	IOL = 100 µA VDD minimum
V_{IH}	Input High Voltage	0.625*VDD	VDD+0.3	V	
V_{IL}	Input Low Voltage	VSS–0.3	0.25*VDD	V	

The definition of the I/O signal levels for the Dual voltage MultiMediaCard changes as a function of VDD.

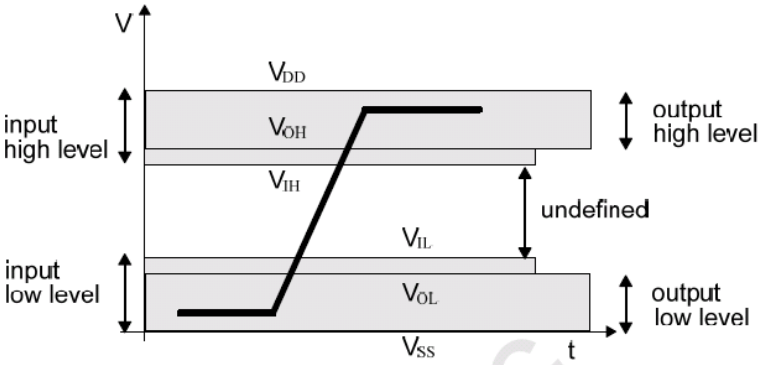
- 2.7–3.6V: Identical to the High Voltage MultiMediaCard
- 1.95–2.7V: Undefined. The card is not operating at this voltage range
- 1.70–1.95V: Compatible with EIA/JEDEC Standard "EIA/JESD8-7 Wide Range" as defined in Table 4-9.

Table 4-9. eMMC* Push-Pull Mode Bus Signal Level—Dual Voltage MultiMediaCard

Symbol	Parameter	Minimum	Maximum	Units	Notes
V_{OH}	Output High Voltage	VDD–0.2	—	V	IOH = –100 µA VDD minimum
V_{OL}	Output Low Voltage	—	0.2	V	IOL = 100 µA VDD minimum
V_{IH}	Input High Voltage	0.7*VDD	VDD+0.3	V	
V_{IL}	Input Low Voltage	VSS–0.3	0.3*VDD	V	

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

Figure 4-1. eMMC* Bus Signal Levels



4.3.4 SD/SDIO

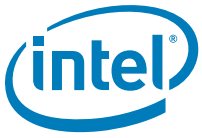
Table 4-10. SD/SDIO Threshold Level for High Voltage Range and General Parameters

Symbol	Parameter	Minimum	Maximum	Units	Notes
V_{DD}	Supply Voltage	—	—		
		2.7	3.6	V	3.3V input
V_{OH}	Output High Voltage	0.75*VDD	—	V	IOH=–100 µA VDD minimum
V_{OL}	Output Low Voltage	—	0.125*VDD	V	IOL=100 µA VDD minimum
V_{IH}	Input High Voltage	0.625*VDD	VDD+0.3	V	
V_{IL}	Input Low Voltage	VSS–0.3	0.25*VDD	V	
	Power Up Time	—	250	ms	From 0V to VDD minimum
	Peak voltage on all lines	-0.3	VDD + 0.3	V	
	Input Leakage Current	-10	10	uA	
	Output Leakage Current	-10	10	uA	

4.3.4.1 SD/SDIO/eMMC* Current Consumption

Current consumption is measured by averaging over one second.

- Before first command: Maximum current is 15 mA
- During initialization: Maximum current is 100 mA
- Operation in Default Mode: Maximum current is 100 mA
- Operation in High Speed Mode: Maximum current is 200 mA
- Operation with other functions: Maximum current is 500 mA.



4.3.4.2 SD/SDIO Bus Signal Line Load

The total capacitance of the SD Memory Card bus is the sum of the bus master capacitance CHOST, the bus capacitance CBUS, and the capacitance CCARD of each card connected to this line:

Total bus capacitance = CHOST + CBUS + N CCARD

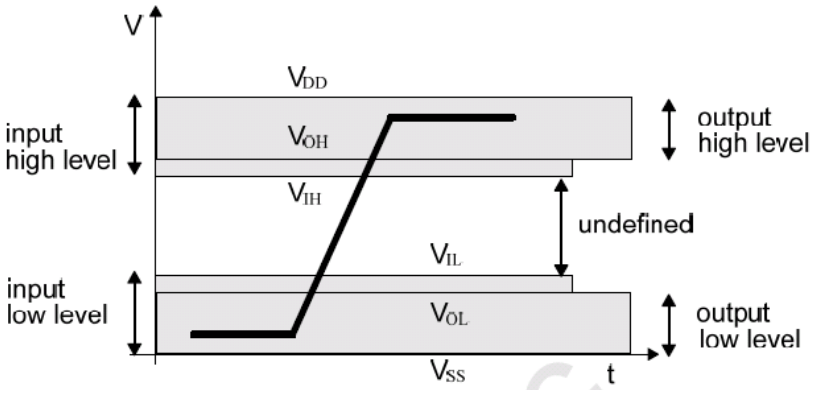
Note: Where N is the number of connected cards.

Table 4-11. SD/SDIO Bus Signal Line Load

Symbol	Parameter	Minimum	Maximum	Units	Notes	Figure
RCMD RDAT	Pull-up resistance	10	100	KΩ	To prevent bus floating	
CL	Total bus capacitance for each signal line	—	40	pF	One card CHOST+CBUS shall not exceed 30 pF	
CCARD	Capacitance of the card for each signal pin	—	10	pF		
	Maximum signal line inductance	—	16	nH	fPP ≤ 20 MHz	
RDAT3	Pull-up resistance inside card (pin1)	10	90	KΩ	May be used for card detection	

4.3.4.3 SD/SDIO Bus Signal Levels

Figure 4-2. Timing Diagram Data Input/Output Referenced to Clock (Default)



To meet the requirements of JEDEC specifications JESD8-1A and JESD8-7, the card input and output voltages must be within the specified ranges shown in Table 4-12 for any V_{DD} of the allowed voltage range.

4.3.5 BT.601 and BT.656

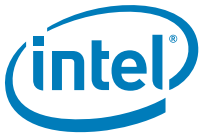
Table 4-12. BT.656 Minimum, Nominal, and Maximum Voltage Parameters

Symbol	Parameter	Minimum	Nominal	Maximum	Unit	Notes
V_{IH}	Input high voltage	1.26	—	—	V	
V_{IL}	Input low voltage	—	—	0.54	V	
V_{OH}	Output high voltage	1.62	—	—	V	
V_{OL}	Output low voltage	—	—	0.18	V	
C_{IN}	Input capacitance	—	—	10	pF	

4.3.6 I^2C

Table 4-13. I^2C—SDA and SCL I/O Stages for F/S-Mode Devices

Symbol	Parameter	Standard-Mode		Fast-Mode		Unit	Notes
		Min.	Max.	Min.	Max.		
V_{IL}	LOW level input voltage: VDD-related input levels	- 0.5	0.3 VDD	- 0.5	0.3* VDD	V	2
V_{IH}	HIGH level input voltage: VDD-related input levels	0.7 VDD	—	0.7 VDD	–	V	2, 3
V_{hys}	Hysteresis of Schmidt trigger inputs: VDD > 2V VDD < 2V	 n/a n/a	 n/a n/a	 0.05 VDD 0.1 VDD	 — —	 V V	
V_{OL} V_{OL3}	LOW level output voltage (open drain or open collector) at 3 mA sink current: VDD > 2V VDD < 2V	 0 n/a	 0.4 n/a	 0 0	 0.4 0.2VDD	 V V	2
t_{of}	Output fall time from VIHmin to VILmax with a bus capacitance from 10–400 pF	—	250	20 + 0.1Cb	250	ns	4, 5
t_{SP}	Pulse width of spikes which must be suppressed by the input filter	n/a	n/a	0	50	ns	
I_i	Input current each I/O pin with an input voltage between 0.1 VDD and 0.9 VDDmax	-10	10	-10	10	µA	6
C_i	Capacitance for each I/O pin	–	10	–	10	pF	



NOTES:
1. VDD refers both to PWR_CSB at 1.8V and to PWR_KBDMISC at either 1.8V or 3.3V.
2. Devices that use non-standard supply voltages which do not conform to the intended I^2C-bus system levels must relate their input levels to the VDD voltage to which the pull-up resistors Rp are connected.
3. Maximum VIH = VDDmax + 0.5V.
4. C_b = capacitance of one bus line in pF.
5. The maximum tf for the SDA and SCL bus lines quoted in Table 4-13 (300 ns) is longer than the specified maximum **t**of for the output stages (250 ns). This allows series protection resistors (Rs) to be connected between the SDA/SCL pins and the SDA/SCL bus lines as shown in Table 4-13 without exceeding the maximum specified tf.
6. I/O pins of fast-mode devices must not obstruct the SDA and SCL lines if VDD is switched off.

4.3.7 I^2S

4.3.7.1 I2S_0 (Voice Interface)

Table 4-14. I2S_0 Minimum, Nominal, and Maximum Voltage Parameters

Symbol	Parameter	Minimum	Nominal	Maximum	Unit	Notes
I2S_0						
V_{IL}	Input Low Voltage	–	–	0.3 * PWR_I2S	V	1, 4
V_{IH}	Input High Voltage	0.7*PWR_I2S	–	PWR_I2S	V	1, 4
V_{OL}	Output Low Voltage	–	–	0.1	V	2, 4
V_{OH}	Output High Voltage	PWR_I2S–0.1	–	–	V	3, 4

NOTES:
1. I2S_0 VIL can undershoot -1.0V for periods of <2 ns and I2S_0 V_{IH} can overshoot to a maximum of 2.8V for periods <2 ns.
2. I_{OL} = +100 µA
3. I_{OH} = -100 µA
4. PWR_I2S = 1.8V, 2.5V, or 3.3V

4.3.7.2 I2S_1 (Audio Interface)

Table 4-15. I2S_1 Minimum, Nominal, and Maximum Voltage Parameters

Symbol	Parameter	Minimum	Nominal	Maximum	Unit	Note
I2S_1						
V_{IL}	Input Low Voltage	–	1.8	0.3 * PWR_PMIC	V	1, 4
V_{IH}	Input High Voltage	0.7*PWR_PMIC	–	PWR_PMIC	V	1, 4
V_{OL}	Output Low Voltage	–	–	0.1	V	2, 4
V_{OH}	Output High Voltage	PWR_PMIC –0.1	–	–	V	3, 4

NOTES:
1. I2S_1 VIL can undershoot -1.0V for periods of <2 ns and I2S_1 V_{IH} can overshoot to a maximum of 2.8V for periods <2 ns.
2. I_{OL} = +100 µA
3. I_{OH} = -100 µA
4. PWR_PMIC = 1.8V

4.3.8 MIPI CSI-2

Table 4-16. MIPI HS-RX/MIPI LP-RX Minimum, Nominal, and Maximum Voltage Parameters

Symbol	Parameter	Min.	Nom.	Max.	Unit	Notes
MIPI HS-RX						
$V_{CMRX(DC)}$	Common-mode voltage HS receive mode	70	—	330	mV	
V_{IDTH}	Differential input high threshold	—	—	70	mV	
V_{IDTL}	Differential input low threshold	-70	–	—	mV	
V_{IHHS}	Single-ended input high voltage	—	—	460	mV	
V_{ILHS}	Single-ended input low voltage	-40	–	—	mV	
$V_{TERM-EN}$	Single-ended threshold for HS termination enable	—	—	450	mV	
Z_{ID}	Differential input impedance	80	100	125	ohm	
MIPI LP-RX						
V_{IH}	Logic 1 input voltage	880	–	–	mV	
V_{IL}	Logic 0 input voltage, not in ULP state	–	–	550	mV	
$V_{IL-ULPS}$	Logic 0 input voltage, ULP state	–	–	300	mV	
V_{HYST}	Input hysteresis	25	–	–	mV	

4.3.9 ONFI 1.0 NAND (Flash)

Table 4-17. Recommended Discrete NAND Operating Conditions

Symbol	Parameter	Minimum	Nominal	Maximum	Unit	Notes
V_{CC33}	Supply voltage for 3.3V devices	2.7	3.3	3.6	V	
V_{CC18}	Supply voltage for 1.8V devices	1.7	1.8	1.95	V	
V_{SS}	Supply voltage	0	0	0	V	

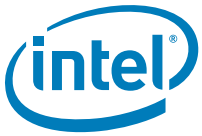


Table 4-18. Discrete NAND Interface CMOS DC Parameters

Symbol	Parameter	Minimum	Nominal	Maximum	Unit	Notes
Discrete NAND CMOS3.3[1]						
I_{CC1}	Operating current Read Page with serial access	—	—	50	mA	
I_{CC2}	Operating current Program	—	—	50	mA	
I_{CC3}	Operating current Erase	—	v	50	mA	
I_{SB1}	Standby current	—	—	1	mA	
I_{SB2}	Standby current	—	—	50	µA	
I_{LI}	Input Leakage Current	—	—	±10	µA	
I_{LO}	Output Leakage Current	—	—	±10	µA	
V_{IH}	Input High Voltage	VCC33*0.8	VCC33	VCC33+0.3	V	
V_{IL}	Input Low Voltage	-0.3	—	VCC33*0.2	V	
V_{OH}	Output High Voltage	VCC33*0.67	—		V	
V_{OL}	Output Low Voltage	—	—	0.1	V	
I_{OL} (R/B#)	Output Low Current (R/B#)	8	10	—	mA	
I_{ST}	Staggered power-up current	—	—	10 per LUN	mA	
Discrete NAND CMOS1.8[1]						
I_{CC1}	Operating current Read Page with serial access	—	—	50	mA	
I_{CC2}	Operating current Program	—	—	50	mA	
I_{CC3}	Operating current Erase	—	—	50	mA	
I_{SB1}	Standby current	—	—	1	mA	
I_{SB2}	Standby current	—	—	50	µA	
I_{LI}	Input Leakage Current	—	—	±10	µA	
I_{LO}	Output Leakage Current	—	—	±10	µA	
V_{IH}	Input High Voltage	VCC18*0.8	–	VCC18+0.3	V	
V_{IL}	Input Low Voltage	-0.3	–	VCC18*0.2	V	
V_{OH}	Output High Voltage	VCC18*0.67	—		V	
V_{OL}	Output Low Voltage	—	—	0.1	V	
I_{OL} (R/B#)	Output Low Current (R/B#)	3	4	—	mA	
I_{ST}	Staggered power-up current	—	—	10 per LUN	mA	

NOTE: [1]Flash port 0 operates at 3.3V. Flash port 1/SD port 1 can operate at 3.3V or 1.8V.

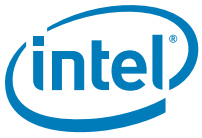
4.3.10 SPI

Table 4-19. SPI Master Minimum, Nominal, and Maximum Voltage Parameters

Symbol	Parameter	Minimum	Nominal	Maximum	Unit	Notes
SPI						
PWR_SPI	Supply Voltage	1.57	1.8	1.98	V	
		2.92	3.3	3.63		
V_{IL}	Input Low Voltage	—	—	PWR_SPI*0.30	V	
V_{IH}	Input High Voltage	PWR_SPI*0.70	—	—	V	
V_{OL}	Output Low Voltage	—	—	0.1	V	
V_{OH}	Output High Voltage	PWR_SPI-0.1	—		V	
I_{OL}	Output Low Current	—	—	3.5	mA	
I_{LEAK}	Input Leakage Current	—	—	1.4	µA	
C_{IN}	Input Capacitance	2.0	—	3.4	pF	

Table 4-20. SPI Slave Minimum, Nominal, and Maximum Voltage Parameters

Symbol	Parameter	Minimum	Nominal	Maximum	Unit	Notes
SPI						
V_{DD}	Supply Voltage	1.57	1.8	1.98	V	
V_{IL}	Input Low Voltage	—	—	0.54	V	
V_{IH}	Input High Voltage	1.26	—	—	V	
V_{OL}	Output Low Voltage	—	—	0.1	V	
V_{OH}	Output High Voltage	1.7	—	—	V	
I_{OL}	Output Low Current	—	—	3.5	mA	
I_{LEAK}	Input Leakage Current	—	—	1.4	µA	
C_{IN}	Input Capacitance	2.0	—	3.4	pF	



4.3.11 USB

Table 4-21. USB Low/Full Speed DC Input Characteristics

Symbol	Parameter	Min.	Max.	Unit	Notes
Input					
V_{DI}	Differential Input Sensitivity	0.2	—	V	1, 3, 4
V_{CM}	Differential Common Mode Range	0.8	2.5	V	2, 3, 4
V_{SE}	Single-Ended Receiver Threshold	0.8	2.0	V	3, 4
Output					
Vol	Low	0	0.3v	V	
V_{OH}	High (Driven)	2.8	3.6	V	
V_{OSE1}	SE1	0.8	—	V	
V_{CRS}	Output Signal Crossover Voltage	1.3	2.0	V	

NOTES:
1. $V_{DI} = |D+ - D-|$
2. Includes VDI range
3. Applies to Low-Speed/High-Speed USB
4. Applies OTG_D{P/N} signals that support High/Full/Low and Full Speed modes.

Table 4-22. USB High Speed DC Input Characteristics

Symbol	Parameter	Min.	Max.	Unit	Notes
Input					
V_{HSSQ}	HS Squelch Detection Threshold	100	150	mV	Note 1,2
V_{HSDSC}	HS Disconnect Detection Threshold	525	625	mV	Note 1,2
V_{HSCM}	HS Data Signaling Common Mode Voltage Range	–50	500	mV	Note 1,2
Output					
V_{HSOI}	High-speed idle level	-10	10	mV	
V_{HSOH}	High-speed data signaling high	260	440	mV	
V_{HSOL}	High-speed data signaling low	-10	10	mV	
V_{CHIRPJ}	Chirp J level (differential voltage)	700	1100	mV	
V_{CHIRPK}	Chirp K level (differential voltage)	-900	-500	mV	

NOTES:
1. Applies to USB_D{P/N}[2:0] that support USB High Speed only.
2. Applies OTG_D{P/N} signals that support High/Full/Low and Full Speed modes.

4.3.12 USB-OTG VBUS Characteristics

The VBus is driven by the PMIC. Refer to the respective PMIC specification for the VBus characteristics.

Refer to the *On-the-Go Supplement to the USB 2.0 Specification Revision 1.3* for details, refer to:
http://www.usb.org/developers/docs/USB_OTG_1-3.pdf

Table 4-23. USB Minimum, Nominal, and Maximum Voltage Parameters

Symbol	Parameter	Minimum	Nominal	Maximum	Unit	Notes
USB High Speed						
Refer to the *Universal Serial Bus (USB) Base Specification, Rev. 2.0*. Only High-speed signaling is supported on the USB 2.0 ports. Full-speed and low-speed signaling are not supported on USB 2.0 ports. High speed and full-speed signaling are supported on the USB-OTG ports.						
USB-OTG						
Refer to the *Universal Serial Bus (USB) On the Go Specification, Revision 1.3.* Only High-Speed and Full Speed signaling is supported on the USB-OTG port. Low-speed signaling is not supported on USB-OTG ports.						

4.4 Intel® Platform Controller Hub MP30 Power Sequencing Timing

Refer to the *Briertown Power Management Integrated Circuit (PMIC) Specification* for power-on sequencing timing.

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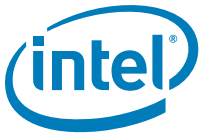


5 Absolute Maximums and Operating Conditions

5.1 Chapter Contents

This chapter contains information about:

- "Intel® Platform Controller Hub MP30 DC Absolute Maximum Operating Conditions"
- "Intel® Platform Controller Hub MP30 Absolute Maximum Temperature Conditions"
- "Thermal Management Acronyms"
- "Intel® Platform Controller Hub MP30 Thermal Characteristics"
- "Intel® Platform Controller Hub MP30 Power Specifications"

5.2 Intel® Platform Controller Hub MP30 DC Absolute Maximum Operating Conditions

The maximum DC ratings for the Intel® Platform Controller Hub MP30 are described in Table 5-1.

Table 5-1. Intel® Platform Controller Hub MP30 Absolute Maximum DC Ratings

Symbol	Absolute Minimum (V)	Absolute Maximum (V)
VCC12	-0.3	1.32
PWR_CPU	-0.3	1.15
VCC_HCLK	-0.3	1.15
VCC_HCLK33	-0.3	3.63
PWR_DMIDVO	-0.3	1.15
PWR_ADMIDVO	-0.3	1.98
VCCHDMI	-0.3	1.32
HDMIVCC3	-0.3	3.63
VCCHDMIBG	-0.3	3.63
VCCA_USB33	-0.3	3.63
VCCA_USB25	-0.3	2.75
VCCA_USB12	-0.3	1.32
PWR_SD0	-0.3	3.63
PWR_SDIO2	-0.3	3.63
PWR_FLSH0	-0.3	3.63
PWR_FLSH1	-0.3	3.63
PWR_BT	-0.3	3.63
PWR_PMIC	-0.3	1.98

Table 5-1. Intel® Platform Controller Hub MP30 Absolute Maximum DC Ratings

Symbol	Absolute Minimum (V)	Absolute Maximum (V)
PWR_I2S	-0.3	3.63
PWR_CSB	-0.3	3.63
PWR_SPI0	-0.3	3.63
PWR_SPI1	-0.3	3.63
PWR_KBDMISC	-0.3	3.63
VCCAHPLL	-0.3	1.32
VCCADPLL	-0.3	1.32

5.3 Thermal Management Acronyms

Table 5-2. Thermal Management Acronyms

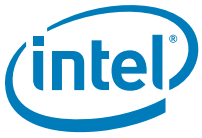
Acronym	Description
Ψ_{jt}	Characterization—Juntion-to-top
Θ_{ja}	Thermal Resistance—Junction-to-ambient
T_{die}	Die Junction Operating Temperature

5.4 Intel® Platform Controller Hub MP30 Absolute Maximum Temperature Conditions

Table 5-3 lists the Intel® Platform Controller Hub MP30 maximum environmental stress ratings. Functional operating parameters at the absolute maximum and minimum is neither implied nor ensured.

The voltage on a specific pin shall be denoted as “V” followed by the subscripted name of that pin.

Caution: At conditions outside functional operation limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits. If the component is exposed to conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time then, when returned to conditions within the functional operating condition limits, it will either not function, or its reliability will be severely degraded. Although the device contains protective circuitry to resist damage from electro-static discharge, precautions should always be taken to avoid high static voltages or electric fields.



5.5 Intel® Platform Controller Hub MP30 Thermal Characteristics

Table 5-3. Intel® Platform Controller Hub MP30 Absolute Maximum Temperature Storage Ratings

Parameter	Description / Signal Names	Minimum	Maximum	Unit
$T_{storage\ (mounted)}$ $T_{storage\ (un\text{-}mounted)}$	Storage Temperature Storage Temperature	-40 -25	85 85	ºC

The thermal resistance of the package is provided in Table 5-4. Package thermal resistance is the measure of the package heat dissipation capability from the die active surface (junction) to a specified reference point (for example; case, board, ambient, and so forth).

Table 5-4. Thermal Characteristics

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
Ψ_{jt}	Characterization Junction-to-top	—	3.0	—	ºC/ Watt	1
Θ_{ja}	Thermal Resistance Junction-to-ambient	—	32	—	ºC/ Watt	1
T_{die}	Die Junction Operating Temperature	-25	—	90	ºC	2, 3

NOTES:

1. Functionality is not ensured for parts that exceed T_{die} temperature above 90º C. T_{die} is measured at the top center of the package. Full performance may be affected if the on-die thermal sensor is enabled.
2. Possible damage to the system controller hub may occur if the Intel® Platform Controller Hub MP30 storage temperature exceeds $T_{storage}$ (mounted) or $T_{storage}$ (un-mounted). Intel does not ensure functionality for parts that have exceeded storage temperatures due to specification violation.
3. Storage temperature is applicable to storage conditions only. In this scenario, the device must not receive a clock, and no pins can be connected to a voltage bias. Storage within these limits will not effect the long-term reliability of the device. This rating applies to the silicon and does not include any tray or packaging.
4. In addition to this storage temperature specification, compliance to the latest IPC/JEDEC J-STD-033B.1 joint industry standard is required for all Surface Mount Devices (SMDs). This document governs handling, packing, shipping and use of moisture/reflow sensitive SMDs.

5.6 Intel® Platform Controller Hub MP30 Power Specifications

Table 5-5. Thermal Design Power

Symbol	Parameter	Value	Units	Notes
TDP	Thermal Design Power (under nominal voltages)	0.7	W	

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6 Intel® Platform Controller Hub MP30 Pin States

6.1 Chapter Contents

This chapter describes the default integrated pull-ups and pull-downs in the Intel® Platform Controller Hub MP30.

6.2 Integrated Pull-Ups and Pull-Downs

Table 6-1. Default Integrated Pull-Up and Pull-Down Signals (Sheet 1 of 2)

Signal/Pin	Resistor	Nominal	Tolerance
SDIO Port 2			
SDIO2_CMD	Pull-up	75 KΩ	±30%
SDIO2_DATA[3:0]	Pull-up	75 KΩ	±30%
SDIO2_CLK	disable	n/a	
SD Port 0			
SD0_CMD	Pull-up	75 KΩ	±30%
SD0_WP	Pull-up	75 KΩ	±30%
SD0_CD#	Pull-up	75 KΩ	±30%
SD0_DATA[7:0]	Pull-up	75 KΩ	±30%
SD0_CLK	disable	n/a	
Discrete NAND Flash Interface			
FLSH_RB[3:0]#	Pull-up	75 KΩ	±30%
FLSH_[1:0]_RE#	Pull-up	75 KΩ	±30%
FLSH_[3:0]_CE#	Pull-up	75 KΩ	±30%
FLSH_[1:0]_CLE	Pull-down	75 KΩ	±30%
FLSH_[1:0]_ALE	Pull-down	75 KΩ	±30%
FLSH_[1:0]_WE#	Pull-up	75 KΩ	±30%
FLSH_[1:0]_WP#	Pull-up	75 KΩ	±30%
FLSH_[1:0]_IO[7:0]	disable	n/a	
SPI1			
SPI_1_SS[3:0]	Pull-up	75 KΩ	±30%
SPI_1_SDO	Pull-down	75 KΩ	±30%
SPI_1_SDI	Pull-down	75 KΩ	±30%
SPI_1_CLK	Pull-down	75 KΩ	±30%
SPI0			
SPI_0_SS[3:0]	Pull-up	75 KΩ	±30%
SPI_0_SDO	Pull-down	75 KΩ	±30%
SPI_0_SDI	Pull-down	75 KΩ	±30%
SPI_0_CLK	Pull-down	75 KΩ	±30%

Table 6-1. Default Integrated Pull-Up and Pull-Down Signals (Sheet 2 of 2)

Signal / Pin	Resistor	Nominal	Tolerance
Keypad			
KP_MKIN[7:0]	Pull-down	2 KΩ	±30%
KP_MKOUT[7:0]	disable	n/a	
KP_DKIN[3:0]	disable	n/a	
Camera Sideband / I²C			
SCLK25	Pull-down	20 KΩ	±30%
FLASH_TRG	Pull-down	20 KΩ	±30%
PRE_FLASH_TRG	Pull-down	20 KΩ	±30%
SNSR_STB	disable	n/a	
SNSR1_STDBY	Pull-down	20 KΩ	±30%
SNSR2_STDBY	Pull-down	20 KΩ	±30%
SNSR_RESET#	Pull-up	20 KΩ	±30%
SNSR_SS_TRG	Pull-up	20 KΩ	±30%
I2C_2_SDA	Pull-up	20 KΩ	±30%
I2C_2_SCL	Pull-up	20 KΩ	±30%
I2C_1_SDA	Pull-up	20 KΩ	±30%
I2C_1_SCL	Pull-up	20 KΩ	±30%
I2C_0_SDA	Pull-up	20 KΩ	±30%
I2C_0_SCL	Pull-up	20 KΩ	±30%
Spare GPIOs			
GPIO[61:59]	Pull-up	20 KΩ	±30%
Parallel Camera Interface			
BT_CSI_CLK	disable	n/a	
BT_CSI_HSYNC	disable	n/a	
BT_CSI_VSYNC	disable	n/a	
BT_CSI_DATA_0	disable	n/a	
I²S			
I2S_1_TXD	Pull-down	75 KΩ	±30%
I2S_1_RXD	disable	n/a	
I2S_1_SYNC	disable	n/a	
I2S_1_CLK	disable	n/a	
I2S_0_TXD	Pull-down	75 KΩ	±30%
I2S_0_RXD	disable	n/a	
I2S_0_SYNC	disable	n/a	
I2S_0_CLK	disable	n/a	

Note: The default Intel® Plaform Controller Hub MP30 integrated pull-up and pull-down signals are based on Intel® Platform Controller Hub MP30 I/O configuration registers, as set by the SCU Firmware. For more information about these registers, refer to the *Intel® Platform Controller Hub MP30 Technical Reference Manual,* Chapter 5—General Purpose I/O.

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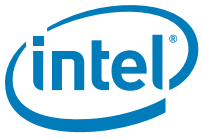


7 Mechanical and Package Specifications

7.1 Chapter Contents

This chapter contains information about:

- "Intel® Platform Controller Hub MP30 Mechanical and Package Acronyms"
- "Intel® Platform Controller Hub MP30 Ballout Pin Information"
- "Intel® Platform Controller Hub MP30 Package Specifications"
- "Intel® Platform Controller Hub MP30 Package Diagrams"
- "Intel® Platform Controller Hub MP30 Ballout Definition and Signal Locations"

7.2 Intel® Platform Controller Hub MP30 Mechanical and Package Acronyms

Table 7-1. Mechanical and Package Acronyms

Acronym	Description
BGA	Ball Grid Array
BO	Ball Out
DO	Die Outline
PL	Pin List

7.3 Intel® Platform Controller Hub MP30 Ballout Pin Information

Table 7-2 lists the Intel® Platform Controller Hub MP30 ballout information arranged alphabetically by signal name. Table 7-3 lists the ballout arranged numerically by pin number. Figure 7-4 through Figure 7-7 show the ballout map as viewed from the top of the package.

Table 7-2. Intel® Platform Controller Hub MP30 Ballout (Sort by Pin Name) (Sheet 1 of 14)

Pin Name	Pin #
BCLKN	E7
BCLKP	E6
BSEL1	E21
BT_CSI_CLK	AB19
BT_CSI_DATA 0	AA16
BT_CSI_DATA 1	Y16
BT_CSI_DATA 2	AB17
BT_CSI_DATA 3	AC17
BT_CSI_DATA 4	AC18
BT_CSI_DATA 5	AF19
BT_CSI_DATA 6	AC20
BT_CSI_DATA 7	AG20
BT_CSI_DATA 8	AE20
BT_CSI_DATA 9	AF22
BT_CSI_HSYNC	AB18
BT_CSI_VSYNC	AA18
CDMI_CVREF	G10
CDMI_GVREF	H12
CDMI_RCOMP	F10
CDMI_RXCHAR#	A16
CDMI_RXD0	D11
CDMI_RXD1	A12
CDMI_RXD2	F14
CDMI_RXD3	E12
CDMI_RXD4	B13
CDMI_RXD5	G14
CDMI_RXD6	A14
CDMI_RXD7	D13
CDMI_RXDPWR#	F16
CDMI_RXSTB_EVEN#	E14
CDMI_RXSTB_ODD#	B15
CDMI_TXCHAR#	H13
CDMI_TXD0	F12
CDMI_TXD1	B7
CDMI_TXD2	D9
CDMI_TXD3	A8
CDMI_TXD4	B9
CDMI_TXD5	G12

Table 7-2. Intel® Platform Controller Hub MP30 Ballout (Sort by Pin Name) (Sheet 2 of 14)

Pin Name	Pin #
CDMI_TXD6	E10
CDMI_TXD7	A10
CDMI_TXDPWR#	B11
CDMI_TXSTB_EVEN#	A6
CDMI_TXSTB_ODD#	E8
CDVO_CVEF	G18
CDVO_GVREF	H16
CDVO_TXD0	D17
CDVO_TXD1	G16
CDVO_TXD2	E18
CDVO_TXD3	B19
CDVO_TXD4	A18
CDVO_TXD5	F18
CDVO_TXSN	B17
CDVO_TXSP	E16
CDVO_TXPWR_N	D19
CDVO_STALL_N	H15
CDVO_VBLNK	D15
EXIT_STDBY	M1
FLASH_TRG	AD5
FLSH_0_ALE	M21
FLSH_0_CE#	H27
FLSH_0_CLE	K27
FLSH_0_IO0	M25
FLSH_0_IO1	L26
FLSH_0_IO2	M27
FLSH_0_IO3	N26
FLSH_0_IO4	P20
FLSH_0_IO5	P21
FLSH_0_IO6	P22
FLSH_0_IO7	R20
FLSH_0_RE#	H25
FLSH_0_WE#	M22
FLSH_0_WP#	M23
FLSH_1_ALE	D23
FLSH_1_CE#	K23
FLSH_1_CLE	D24
FLSH_1_IO0	C24

Table 7-2. Intel® Platform Controller Hub MP30 Ballout (Sort by Pin Name) (Sheet 3 of 14)

Pin Name	Pin #
FLSH_1_IO1	H20
FLSH_1_IO2	H21
FLSH_1_IO3	H22
FLSH_1_IO4	G22
FLSH_1_IO5	G23
FLSH_1_IO6	F24
FLSH_1_IO7	D25
FLSH_1_RE#	K22
FLSH_1_WE#	F23
FLSH_1_WP#	G20
FLSH_2_CE#	K25
FLSH_3_CE#	J26
FLSH_RB0#	E26
FLSH_RB1#	F25
FLSH_RB2#	F27
FLSH_RB3#	G26
GPIO59	T3
GPIO60	T1
GPIO61	P1
HDMI_CLK_DN	AG12
HDMI_CLK_DP	AE12
HDMI_HOTPLUG	AC16
HDMICOMP	AB12
HDMIDATA0_DN	AA12
HDMIDATA0_DP	Y12
HDMIDATA1_DN	AB14
HDMIDATA1_DP	AB13
HDMIDATA2_DN	AC14
HDMIDATA2_DP	AC13
HDMIVCC3	Y10
HDMIVCC3	AA10
HV_RCOMP	K3
I2C_0_SCL	T6
I2C_0_SDA	T5
I2C_1_SCL	AC5
I2C_1_SDA	AB5
I2C_2_SCL	P3
I2C_2_SDA	P5

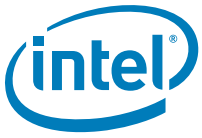


Table 7-2. Intel® Platform Controller Hub MP30 Ballout (Sort by Pin Name) (Sheet 4 of 14)

Pin Name	Pin #
I2S_0_CLK	Y21
I2S_0_RXD	AF23
I2S_0_SYNC	AB22
I2S_0_TXD	AA20
I2S_1_CLK	AC22
I2S_1_RXD	AG22
I2S_1_SYNC	AE22
I2S_1_TXD	AB20
KP_DKIN0	AB4
KP_DKIN1	AC4
KP_DKIN2	AC2
KP_DKIN3	Y7
KP_MKIN0	V8
KP_MKIN1	AB3
KP_MKIN2	AB1
KP_MKIN3	Y6
KP_MKIN4	AA2
KP_MKIN5	Y5
KP_MKIN6	Y3
KP_MKIN7	V7
KP_MKOUT0	V6
KP_MKOUT1	Y1
KP_MKOUT2	V3
KP_MKOUT3	V5
KP_MKOUT4	T8
KP_MKOUT5	V1
KP_MKOUT6	U2
KP_MKOUT7	T7
MIPI_CSI_CLKN	AE16
MIPI_CSI_CLKP	AG16
MIPI_CSI_DQN0	AG14
MIPI_CSI_DQN1	AG18
MIPI_CSI_DQP0	AE14
MIPI_CSI_DQP1	AE18
MIPI_CSI_RCOMP	AB16
OSC_IN	G8
OSC_OUT	F7
OTG_DN	AB27

Table 7-2. Intel® Platform Controller Hub MP30 Ballout (Sort by Pin Name) (Sheet 5 of 14)

Pin Name	Pin #
OTG_DP	AA26
OTG_ID	Y22
OTG_VBUS	Y25
PMIC_INTR	P8
PRE_FLASH_TRG	AA8
PWR_ADMIDVO	K10
PWR_BT	V17
PWR_CPU	K18
PWR_CSB	V10
PWR_DMIDVO	J11
PWR_DMIDVO	J2
PWR_DMIDVO	J4
PWR_DMIDVO	K12
PWR_DMIDVO	K15
PWR_DMIDVO	K16
PWR_FLSH0	M20
PWR_FLSH0	N17
PWR_FLSH0	N19
PWR_FLSH1	K20
PWR_FLSH1	K21
PWR_FLSH1	L17
PWR_FLSH1	L19
PWR_I2S	V20
PWR_KBDMISC	R10
PWR_KBDMISC	U10
PWR_PMIC	N9
PWR_SD0	R17
PWR_SD0	R18
PWR_SD0	T20
PWR_SD0	T21
PWR_SDIO2	P18
PWR_SPI0	L9
PWR_SPI1	L10
PWRGOOD	P6
PWRMODE0	E22
PWRMODE1	A22
PWRMODE2	B23
PWR_DMIDVO	J14

Table 7-2. Intel® Platform Controller Hub MP30 Ballout (Sort by Pin Name) (Sheet 6 of 14)

Pin Name	Pin #
RESERVED1	AG4
RESERVED10	AF9
RESERVED11	AG10
RESERVED12	AG8
RESERVED13	AF7
RESERVED14	AC10
RESERVED15	AG6
RESERVED16	AF5
RESERVED17	AE8
RESERVED18	AE10
RESERVED2	AG2
RESERVED3	D1
RESERVED32	AA14
RESERVED33	AB10
RESERVED34	AA10
RESERVED35	Y10
RESERVED4	B1
RESERVED5	B5
RESERVED6	D4
RESERVED7	AA23
RESERVED8_NCTF	A27
RESERVED9_NCTF	AG1
RESET_OUT#	L2
RESET#	P7
SCLK25	AC7
SD0_CD#	Y23
SD0_CLK	W24
SD0_CMD	W26
SD0_DATA0	T23
SD0_DATA1	T22
SD0_DATA2	V27
SD0_DATA3	U26
SD0_DATA4	V25
SD0_DATA5	V24
SD0_DATA6	Y27
SD0_DATA7	V23
SD0_WP	V22
SDIO2_CLK	T25

Table 7-2. Intel® Platform Controller Hub MP30 Ballout (Sort by Pin Name) (Sheet 7 of 14)

Pin Name	Pin #
SDIO2_CMD	R26
SDIO2_DAT0	P25
SDIO2_DAT1	P23
SDIO2_DAT2	P27
SDIO2_DAT3	T27
SNSR_RESET#	Y8
SNSR_SS_TRG	AD4
SNSR_STB	AE4
SNSR1_STDBY	AB6
SNSR2_STDBY	AC6
SPI_0_CLK	F1
SPI_0_SDI	K7
SPI_0_SDO	H5
SPI_0_SS0	H3
SPI_0_SS1	H1
SPI_0_SS2	K5
SPI_0_SS3	K6
SPI_1_CLK	F5
SPI_1_SDI	H7
SPI_1_SDO	F4
SPI_1_SS0	E2
SPI_1_SS1	H6
SPI_1_SS2	F2
SPI_1_SS3	K8
SPI_2_CLK	M7
SPI_2_SDI	M8
SPI_2_SDO	M6
SPI_2_SS0	M3
SPI_2_SS1	M5
SRFWEN#	K1
TCK	H18
TDI	D21
TDO	H19
TEST	B21
TMS	A20
TRST#	E20
USB_DN0	AB25
USB_DN1	AC24

Table 7-2. Intel® Platform Controller Hub MP30 Ballout (Sort by Pin Name) (Sheet 8 of 14)

Pin Name	Pin #
USB_DN2	AD24
USB_DP0	AC26
USB_DP1	AD25
USB_DP2	AE24
USB_RCOMP	AB24
VCC_HCLK	D3
VCC_HCLK33	D5
VCC12	P14
VCC12	R12
VCC12	R15
VCC12	V13
VCC12	V15
VCC12	Y18
VCC25	L12
VCCA_USB25	U18
VCCA_USB25	U20
VCCA_USB33	Y20
VCCADPLL	AE6
VCCAHPLL	H8
VCCHDMI	Y14
VCCHDMIBG	AB11
VR_COMP	N2
VSS	L11
VSS_NCTF	AG27
VSS_NCTF	A2
VSS_NCTF	A24
VSS_NCTF	A26
VSS_NCTF	A4
VSS	AA11
VSS	AA13
VSS	AA17
VSS	AA19
VSS	AA22
VSS	AA24
VSS	AA4
VSS	AA5
VSS	AA6
VSS	AA9

Table 7-2. Intel® Platform Controller Hub MP30 Ballout (Sort by Pin Name) (Sheet 9 of 14)

Pin Name	Pin #
VSS	AB21
VSS	AB7
VSS	AC19
VSS	AC21
VSS	AC23
VSS	AC9
VSS_NCTF	AD1
VSS	AD11
VSS	AD13
VSS	AD15
VSS	AD17
VSS	AD19
VSS	AD21
VSS	AD23
VSS_NCTF	AD27
VSS	AD3
VSS	AD7
VSS	AD9
VSS_NCTF	AF1
VSS_NCTF	AF2
VSS	L20
VSS	L21
VSS	L22
VSS	L23
VSS	L24
VSS	L4
VSS	L5
VSS	L6
VSS	L7
VSS	L8
VSS	N10
VSS	N11
VSS	N12
VSS	N13
VSS	N14
VSS	N15
VSS	N16
VSS	N18

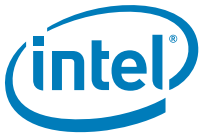


Table 7-2. Intel® Platform Controller Hub MP30 Ballout (Sort by Pin Name) (Sheet 10 of 14)

Pin Name	Pin #
VSS	N20
VSS	N21
VSS	N22
VSS	N24
VSS	N4
VSS	N5
VSS	N6
VSS	N7
VSS	N8
VSS	P11
VSS	P12
VSS	P16
VSS	R13
VSS	R2
VSS	R21
VSS	R22
VSS	R24
VSS_NCTF	AF26
VSS_NCTF	AF27
VSS_NCTF	AG25
VSS_NCTF	AG26
VSS_NCTF	B2
VSS_NCTF	B26
VSS_NCTF	B27
VSS	C10
VSS	C12
VSS	C14
VSS	C16
VSS	C18
VSS	C20
VSS	C22
VSS	C4
VSS	C6
VSS	C8
VSS_NCTF	D27
VSS	D7
VSS	E11
VSS	E13

Table 7-2. Intel® Platform Controller Hub MP30 Ballout (Sort by Pin Name) (Sheet 11 of 14)

Pin Name	Pin #
VSS	E15
VSS	E17
VSS	E19
VSS	E23
VSS	E24
VSS	E4
VSS	E5
VSS	E9
VSS	F11
VSS	F13
VSS	F15
VSS	F17
VSS	F19
VSS	F20
VSS	F21
VSS	R4
VSS	R5
VSS	R6
VSS	R7
VSS	R8
VSS	T11
VSS	T13
VSS	T15
VSS	T17
VSS	T19
VSS	U12
VSS	U14
VSS	U16
VSS	U21
VSS	U22
VSS	U23
VSS	U24
VSS	U25
VSS	U4
VSS	U5
VSS	U6
VSS	U7
VSS	U8

Table 7-2. Intel® Platform Controller Hub MP30 Ballout (Sort by Pin Name) (Sheet 12 of 14)

Pin Name	Pin #
VSS	V11
VSS	V12
VSS	V14
VSS	V16
VSS	V18
VSS	V19
VSS	V21
VSS	W2
VSS	W20
VSS	W21
VSS	W22
VSS	W23
VSS	W4
VSS	W5
VSS	W6
VSS	AA15
VSS	AB15
VSS	AC12
VSS	AC15
VSS	AC8
VSS	AF11
VSS	AF13
VSS	AF15
VSS	AF17
VSS	F22
VSS	F8
VSS	F9
VSS	G11
VSS	G13
VSS	G15
VSS	G17
VSS	G19
VSS	G2
VSS	G24
VSS	G4
VSS	G5
VSS	G6
VSS	G9

Table 7-2. Intel® Platform Controller Hub MP30 Ballout (Sort by Pin Name) (Sheet 13 of 14)

Pin Name	Pin #
VSS	H11
VSS	H14
VSS	H17
VSS	H23
VSS	H9
VSS	J12
VSS	J16
VSS	J17
VSS	J20
VSS	J21
VSS	J22
VSS	J23
VSS	J24
VSS	J5
VSS	J6
VSS	J7
VSS	J8
VSS	K13
VSS	L13
VSS	L14
VSS	L15
VSS	L16
VSS	L18
VSS	W7
VSS	W8
VSS	Y11
VSS	Y13
VSS	Y15
VSS	Y17
VSS	Y19
VSS	Y9
VSS	AB23
VSS	AB9
VSS	F6
VSS	N23
VSS	R23

Table 7-2. Intel® Platform Controller Hub MP30 Ballout (Sort by Pin Name) (Sheet 14 of 14)

Pin Name	Pin #
VSSHDMI	AC11
VSSADPLL	AB8
VSSAHPLL	H10

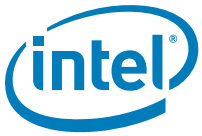


Table 7-3. Intel® Platform Controller Hub MP30 Ballout (Sort by Pin Number) (Sheet 1 of 13)

Pin #	Pin Name
A10	CDMI_TXD7
A12	CDMI_RXD1
A14	CDMI_RXD6
A16	CDMI_RXCHAR#
A18	CDVO_TXD4
A2	VSS_NCTF
A20	TMS
A22	PWRMODE1
A24	VSS_NCTF
A26	VSS_NCTF
A27	RESERVED8_NCTF
A4	VSS_NCTF
A6	CDMI_TXSTB_EVEN#
A8	CDMI_TXD3
AA10	HDMIVCC3
AA11	VSS
AA12	HDMIDATA0_DN
AA13	VSS
AA14	RESERVED32
AA15	VSS
AA16	BT_CSI_DATA 0
AA17	VSS
AA18	BT_CSI_VSYNC
AA19	VSS
AA2	KP_MKIN4
AA20	I2S_0_TXD
AA22	VSS
AA23	RESERVED7
AA24	VSS
AA26	OTG_DP
AA4	VSS
AA5	VSS
AA6	VSS
AA8	PRE_FLASH_TRG
AA9	VSS
AB1	KP_MKIN2
AB10	RESERVED33
AB11	VCCHDMIBG

Table 7-3. Intel® Platform Controller Hub MP30 Ballout (Sort by Pin Number) (Sheet 2 of 13)

Pin #	Pin Name
AB12	HDMICOMP
AB13	HDMIDATA1_DP
AB14	HDMIDATA1_DN
AB15	VSS
AB16	MIPI_CSI_RCOMP
AB17	BT_CSI_DATA 2
AB18	BT_CSI_HSYNC
AB19	BT_CSI_CLK
AB20	I2S_1_TXD
AB21	VSS
AB22	I2S_0_SYNC
AB23	VSS
AB24	USB_RCOMP
AB25	USB_DN0
AB27	OTG_DN
AB3	KP_MKIN1
AB4	KP_DKIN0
AB5	I2C_1_SDA
AB6	SNSR1_STDBY
AB7	VSS
AB8	VSSADPLL
AB9	VSS
AC10	RESERVED14
AC11	VSSHDMI
AC12	VSS
AC13	HDMIDATA2_DP
AC14	HDMIDATA2_DN
AC15	VSS
AC16	HDMI_HOTPLUG
AC17	BT_CSI_DATA 3
AC18	BT_CSI_DATA 4
AC19	VSS
AC2	KP_DKIN2
AC20	BT_CSI_DATA 6
AC21	VSS
AC22	I2S_1_CLK
AC23	VSS
AC24	USB_DN1

Table 7-3. Intel® Platform Controller Hub MP30 Ballout (Sort by Pin Number) (Sheet 3 of 13)

Pin #	Pin Name
AC26	USB_DP0
AC4	KP_DKIN1
AC5	I2C_1_SCL
AC6	SNSR2_STDBY
AC7	SCLK25
AC8	VSS
AC9	VSS
AD1	VSS_NCTF
AD11	VSS
AD13	VSS
AD15	VSS
AD17	VSS
AD19	VSS
AD21	VSS
AD23	VSS
AD24	USB_DN2
AD25	USB_DP1
AD27	VSS_NCTF
AD3	VSS
AD4	SNSR_SS_TRG
AD5	FLASH_TRG
AD7	VSS
AD9	VSS
AE10	RESERVED18
AE12	HDMI_CLK_DP
AE14	MIPI_CSI_DQP0
AE16	MIPI_CSI_CLKN
AE18	MIPI_CSI_DQP1
AE20	BT_CSI_DATA 8
AE22	I2S_1_SYNC
AE24	USB_DP2
AE4	SNSR_STB
AE6	VCCADPLL
AE8	RESERVED17
AF1	VSS_NCTF
AF11	VSS
AF13	VSS
AF15	VSS

Table 7-3. Intel® Platform Controller Hub MP30 Ballout (Sort by Pin Number) (Sheet 4 of 13)

Pin #	Pin Name
AF17	VSS
AF19	BT_CSI_DATA 5
AF2	VSS_NCTF
AF22	BT_CSI_DATA 9
AF23	I2S_0_RXD
AF26	VSS_NCTF
AF27	VSS_NCTF
AF5	RESERVED16
AF7	RESERVED13
AF9	RESERVED10
AG1	RESERVED9_NCTF
AG10	RESERVED11
AG12	HDMI_CLK_DN
AG14	MIPI_CSI_DQN0
AG16	MIPI_CSI_CLKP
AG18	MIPI_CSI_DQN1
AG2	RESERVED2
AG20	BT_CSI_DATA 7
AG22	I2S_1_RXD
AG25	VSS_NCTF
AG26	VSS_NCTF
AG27	VSS_NCTF
AG4	RESERVED1
AG6	RESERVED15
AG8	RESERVED12
B1	RESERVED4
B11	CDMI_TXDPWR#
B13	CDMI_RXD4
B15	CDMI_RXSTB_ODD#
B17	CDVO_TXSN
B19	CDVO_TXD3
B2	VSS_NCTF
B21	TEST
B23	PWRMODE2
B26	VSS_NCTF
B27	VSS_NCTF
B5	RESERVED5
B7	CDMI_TXD1

Table 7-3. Intel® Platform Controller Hub MP30 Ballout (Sort by Pin Number) (Sheet 5 of 13)

Pin #	Pin Name
B9	CDMI_TXD4
C10	VSS
C12	VSS
C14	VSS
C16	VSS
C18	VSS
C20	VSS
C22	VSS
C24	FLSH_1_IO0
C4	VSS
C6	VSS
C8	VSS
D1	RESERVED3
D11	CDMI_RXD0
D13	CDMI_RXD7
D15	CDVO_VBLNK
D17	CDVO_TXD0
D19	CDVO_TXPWR_N
D21	TDI
D23	FLSH_1_ALE
D24	FLSH_1_CLE
D25	FLSH_1_IO7
D27	VSS_NCTF
D3	VCC_HCLK
D4	RESERVED6
D5	VCC_HCLK33
D7	VSS
D9	CDMI_TXD2
E10	CDMI_TXD6
E11	VSS
E12	CDMI_RXD3
E13	VSS
E14	CDMI_RXSTB_EVEN#
E15	VSS
E16	CDVO_TXSP
E17	VSS
E18	CDVO_TXD2
E19	VSS

Table 7-3. Intel® Platform Controller Hub MP30 Ballout (Sort by Pin Number) (Sheet 6 of 13)

Pin #	Pin Name
E2	SPI_1_SS0
E20	TRST#
E21	BSEL1
E22	PWRMODE0
E23	VSS
E24	VSS
E26	FLSH_RB0#
E4	VSS
E5	VSS
E6	BCLKP
E7	BCLKN
E8	CDMI_TXSTB_ODD#
E9	VSS
F1	SPI_0_CLK
F10	CDMI_RCOMP
F11	VSS
F12	CDMI_TXD0
F13	VSS
F14	CDMI_RXD2
F15	VSS
F16	CDMI_RXDPWR#
F17	VSS
F18	CDVO_TXD5
F19	VSS
F2	SPI_1_SS2
F20	VSS
F21	VSS
F22	VSS
F23	FLSH_1_WE#
F24	FLSH_1_IO6
F25	FLSH_RB1#
F27	FLSH_RB2#
F4	SPI_1_SDO
F5	SPI_1_CLK
F6	VSS
F7	OSC_OUT
F8	VSS
F9	VSS

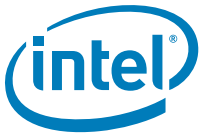


Table 7-3. Intel® Platform Controller Hub MP30 Ballout (Sort by Pin Number) (Sheet 7 of 13)

Pin #	Pin Name
G10	CDMI_CVREF
G11	VSS
G12	CDMI_TXD5
G13	VSS
G14	CDMI_RXD5
G15	VSS
G16	CDVO_TXD1
G17	VSS
G18	CDVO_CVREF
G19	VSS
G2	VSS
G20	FLSH_1_WP#
G22	FLSH_1_IO4
G23	FLSH_1_IO5
G24	VSS
G26	FLSH_RB3#
G4	VSS
G5	VSS
G6	VSS
G8	OSC_IN
G9	VSS
H1	SPI_0_SS1
H10	VSSAHPLL
H11	VSS
H12	CDMI_GVREF
H13	CDMI_TXCHAR#
H14	VSS
H15	CDVO_STALL_N
H16	CDVO_GVREF
H17	VSS
H18	TCK
H19	TDO
H20	FLSH_1_IO1
H21	FLSH_1_IO2
H22	FLSH_1_IO3
H23	VSS
H25	FLSH_0_RE#
H27	FLSH_0_CE#

Table 7-3. Intel® Platform Controller Hub MP30 Ballout (Sort by Pin Number) (Sheet 8 of 13)

Pin #	Pin Name
H3	SPI_0_SS0
H5	SPI_0_SDO
H6	SPI_1_SS1
H7	SPI_1_SDI
H8	VCCAHPLL
H9	VSS
J11	PWR_DMIDVO
J12	VSS
J14	PWR_DMIDVO
J16	VSS
J17	VSS
J2	PWR_DMIDVO
J20	VSS
J21	VSS
J22	VSS
J23	VSS
J24	VSS
J26	FLSH_3_CE#
J4	PWR_DMIDVO
J5	VSS
J6	VSS
J7	VSS
J8	VSS
K1	SRFWEN#
K10	PWR_ADMIDVO
K12	PWR_DMIDVO
K13	VSS
K15	PWR_DMIDVO
K16	PWR_DMIDVO
K18	PWR_CPU
K20	PWR_FLSH1
K21	PWR_FLSH1
K22	FLSH_1_RE#
K23	FLSH_1_CE#
K25	FLSH_2_CE#
K27	FLSH_0_CLE
K3	HV_RCOMP
K5	SPI_0_SS2

Table 7-3. Intel® Platform Controller Hub MP30 Ballout (Sort by Pin Number) (Sheet 9 of 13)

Pin #	Pin Name
K6	SPI_0_SS3
K7	SPI_0_SDI
K8	SPI_1_SS3
L10	PWR_SPI1
L11	VSS
L12	VCC25
L13	VSS
L14	VSS
L15	VSS
L16	VSS
L17	PWR_FLSH1
L18	VSS
L19	PWR_FLSH1
L2	RESET_OUT#
L20	VSS
L21	VSS
L22	VSS
L23	VSS
L24	VSS
L26	FLSH_0_IO1
L4	VSS
L5	VSS
L6	VSS
L7	VSS
L8	VSS
L9	PWR_SPI0
M1	EXIT_STDBY
M20	PWR_FLSH0
M21	FLSH_0_ALE
M22	FLSH_0_WE#
M23	FLSH_0_WP#
M25	FLSH_0_IO0
M27	FLSH_0_IO2
M3	SPI_2_SS0
M5	SPI_2_SS1
M6	SPI_2_SDO
M7	SPI_2_CLK
M8	SPI_2_SDI

Table 7-3. Intel® Platform Controller Hub MP30 Ballout (Sort by Pin Number) (Sheet 10 of 13)

Pin #	Pin Name
N10	VSS
N11	VSS
N12	VSS
N13	VSS
N14	VSS
N15	VSS
N16	VSS
N17	PWR_FLSH0
N18	VSS
N19	PWR_FLSH0
N2	VR_COMP
N20	VSS
N21	VSS
N22	VSS
N23	VSS
N24	VSS
N26	FLSH_0_IO3
N4	VSS
N5	VSS
N6	VSS
N7	VSS
N8	VSS
N9	PWR_PMIC
P1	GPIO61
P11	VSS
P12	VSS
P14	VCC12
P16	VSS
P18	PWR_SDIO2
P20	FLSH_0_IO4
P21	FLSH_0_IO5
P22	FLSH_0_IO6
P23	SDIO2_DAT1
P25	SDIO2_DAT0
P27	SDIO2_DAT2
P3	I2C_2_SCL
P5	I2C_2_SDA
P6	PWRGOOD

Table 7-3. Intel® Platform Controller Hub MP30 Ballout (Sort by Pin Number) (Sheet 11 of 13)

Pin #	Pin Name
P7	RESET#
P8	PMIC_INTR
R10	PWR_KBDMISC
R12	VCC12
R13	VSS
R15	VCC12
R17	PWR_SD0
R18	PWR_SD0
R2	VSS
R20	FLSH_0_IO7
R21	VSS
R22	VSS
R23	VSS
R24	VSS
R26	SDIO2_CMD
R4	VSS
R5	VSS
R6	VSS
R7	VSS
R8	VSS
T1	GPIO60
T11	VSS
T13	VSS
T15	VSS
T17	VSS
T19	VSS
T20	PWR_SD0
T21	PWR_SD0
T22	SD0_DATA1
T23	SD0_DATA0
T25	SDIO2_CLK
T27	SDIO2_DAT3
T3	GPIO59
T5	I2C_0_SDA
T6	I2C_0_SCL
T7	KP_MKOUT7
T8	KP_MKOUT4
U10	PWR_KBDMISC

Table 7-3. Intel® Platform Controller Hub MP30 Ballout (Sort by Pin Number) (Sheet 12 of 13)

Pin #	Pin Name
U12	VSS
U14	VSS
U16	VSS
U18	VCCA_USB25
U2	KP_MKOUT6
U20	VCCA_USB25
U21	VSS
U22	VSS
U23	VSS
U24	VSS
U25	VSS
U26	SD0_DATA3
U4	VSS
U5	VSS
U6	VSS
U7	VSS
U8	VSS
V1	KP_MKOUT5
V10	PWR_CSB
V11	VSS
V12	VSS
V13	VCC12
V14	VSS
V15	VCC12
V16	VSS
V17	PWR_BT
V18	VSS
V19	VSS
V20	PWR_I2S
V21	VSS
V22	SD0_WP
V23	SD0_DATA7
V24	SD0_DATA5
V25	SD0_DATA4
V27	SD0_DATA2
V3	KP_MKOUT2
V5	KP_MKOUT3
V6	KP_MKOUT0

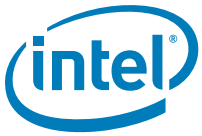


Table 7-3. Intel® Platform Controller Hub MP30 Ballout (Sort by Pin Number) (Sheet 13 of 13)

Pin #	Pin Name
V7	KP_MKIN7
V8	KP_MKIN0
W2	VSS
W20	VSS
W21	VSS
W22	VSS
W23	VSS
W24	SD0_CLK
W26	SD0_CMD
W4	VSS
W5	VSS
W6	VSS
W7	VSS
W8	VSS
Y1	KP_MKOUT1
Y10	HDMIVCC3
Y11	VSS
Y12	HDMIDATA0_DP
Y13	VSS
Y14	VCCHDMI
Y15	VSS
Y16	BT_CSI_DATA 1
Y17	VSS
Y18	VCC12
Y19	VSS
Y20	VCCA_USB33
Y21	I2S_0_CLK
Y22	OTG_ID
Y23	SD0_CD#
Y25	OTG_VBUS
Y27	SD0_DATA6
Y3	KP_MKIN6
Y5	KP_MKIN5
Y6	KP_MKIN3
Y7	KP_DKIN3
Y8	SNSR_RESET#
Y9	VSS

7.4 Intel® Platform Controller Hub MP30 Package Specifications

The Intel® Platform Controller Hub MP30 comes in a Flip-Chip Ball Grid Array (FCBGA) package and consists of a silicon die mounted face down on an organic substrate populated with 493 solder balls on the bottom side. Capacitors may be placed in the area surrounding the die. Because the die-side capacitors are electrically conductive, and only slightly shorter than the die height, care should be taken to avoid contacting the capacitors with electrically conductive materials. Doing so may short the capacitors and possibly damage the device or render it inactive.

The use of an insulating material between the capacitors and any thermal solution should be considered to prevent capacitor shorting. An exclusion, or keep out zone, surrounds the die and capacitors, and identifies the contact area for the package. Care should be taken to avoid contact with the package inside this area.

Unless otherwise specified, interpret the dimensions and tolerances in accordance with ASME Y14.5-1994. The dimensions are in millimeters. Key package attributes are listed below:

Dimensions:

- Package parameters: 14 mm x 14 mm
- Height 1.3 mm (maximum)
- Ball Count: 493
- Land metal diameter: See following Diagrams
- Solder resist opening: See following Diagrams

7.5 Intel® Platform Controller Hub MP30 Package Diagrams

Figure 7-1. Intel® Platform Controller Hub MP30 (Top View)

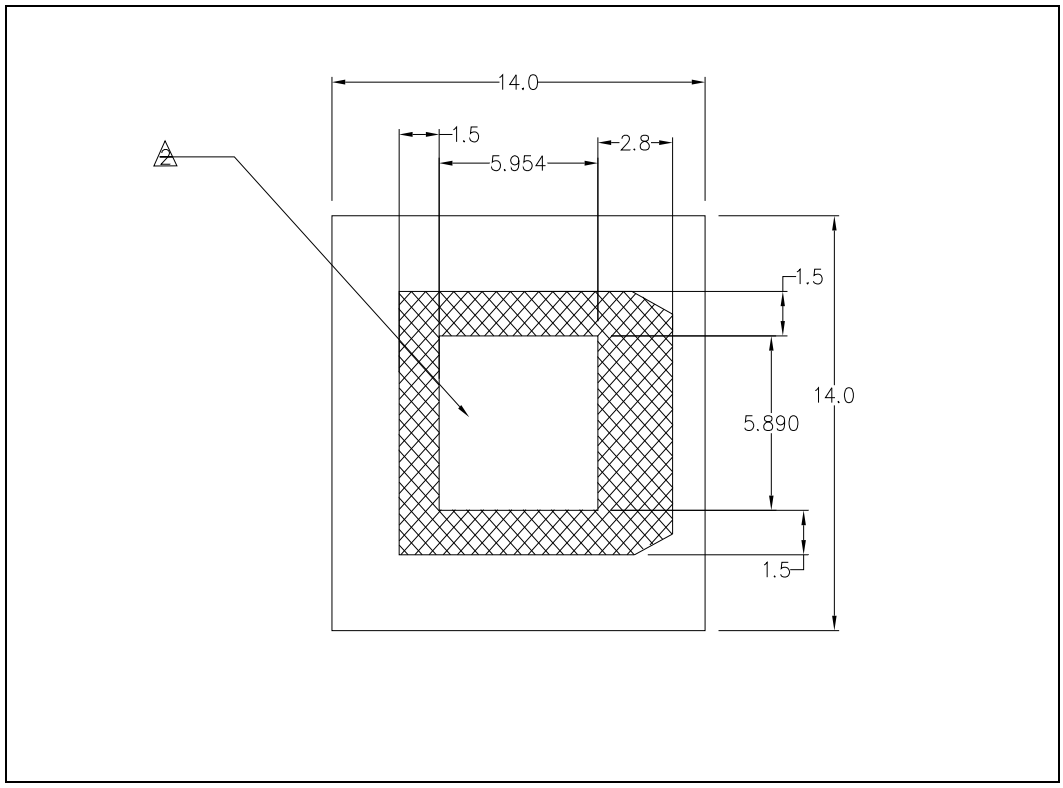


Figure 7-2. Intel® Platform Controller Hub MP30 (Bottom View)

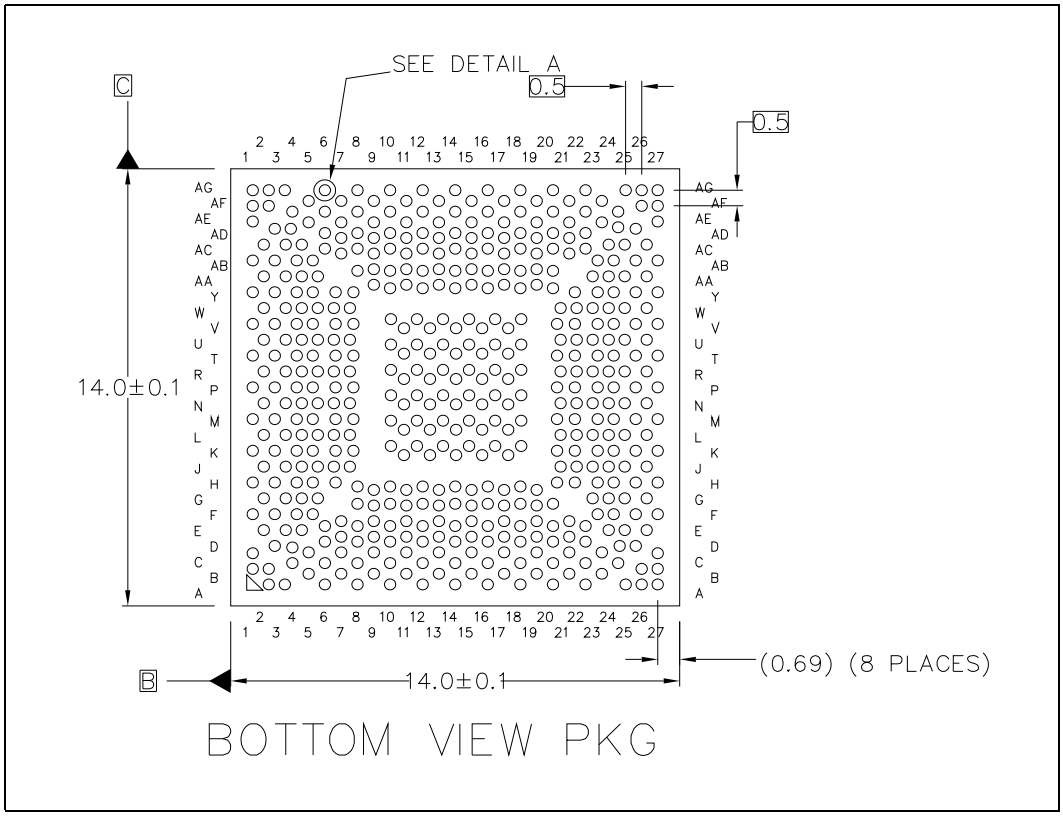
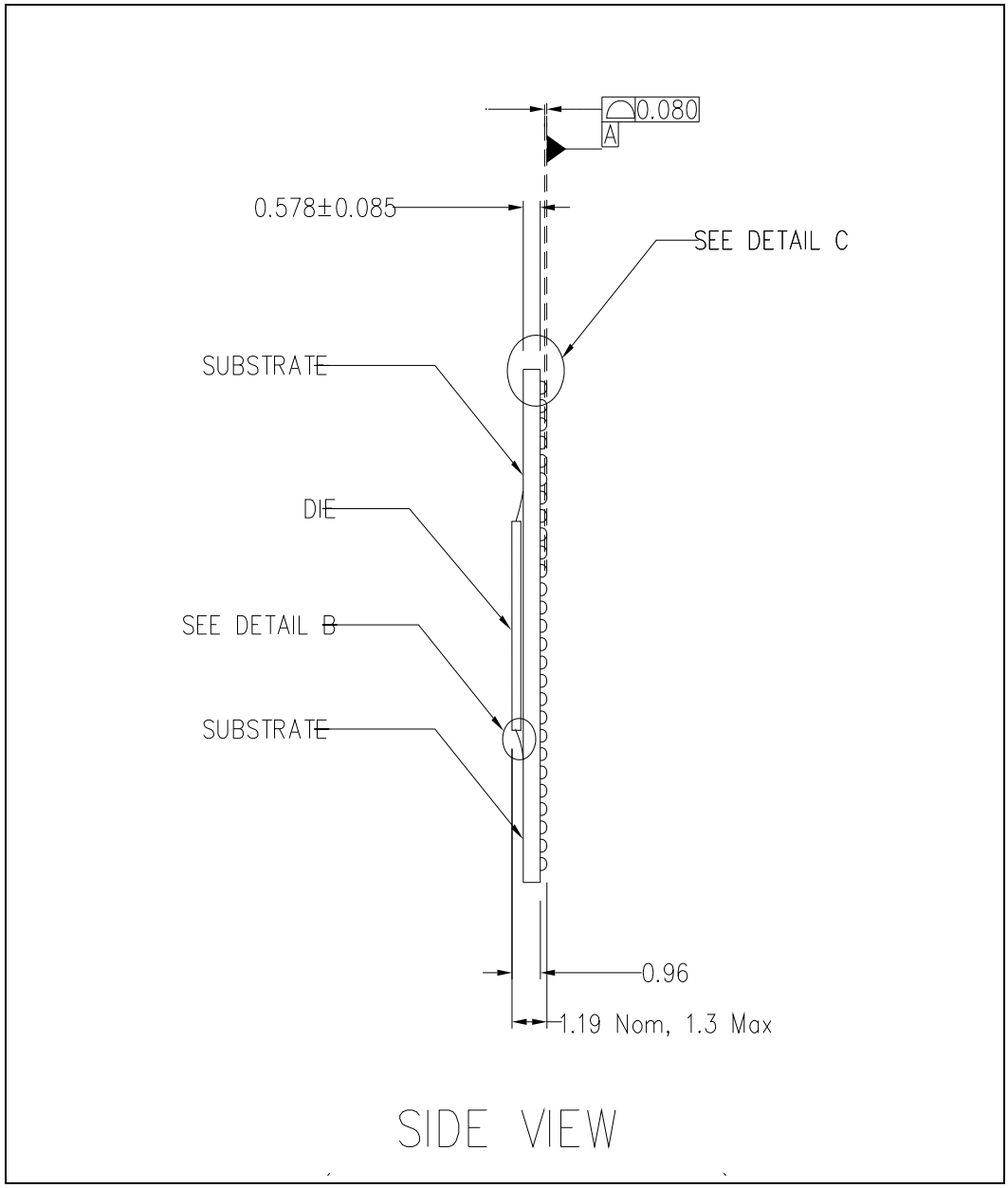


Figure 7-3. Intel® Platform Controller Hub MP30 (Side View, Unmounted)



NOTE: The maximum outgoing package coplanarity cannot exceed 8 mils.

Figure 7-4. Intel® Platform Controller Hub MP30 Package (Solder Ball Detail)

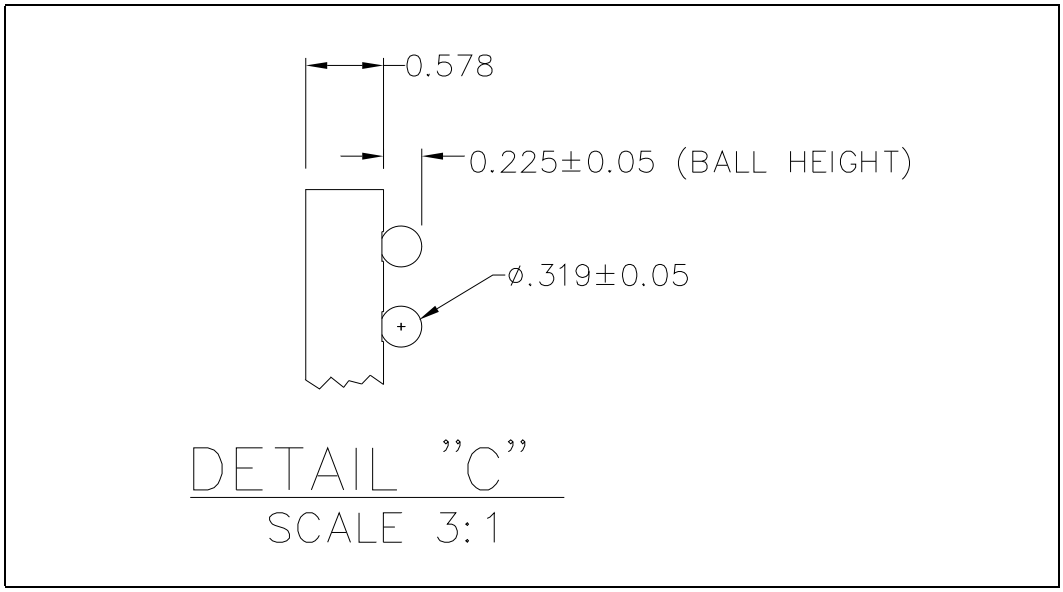


Figure 7-5. Intel® Platform Controller Hub MP30 Package (Underfill Detail)

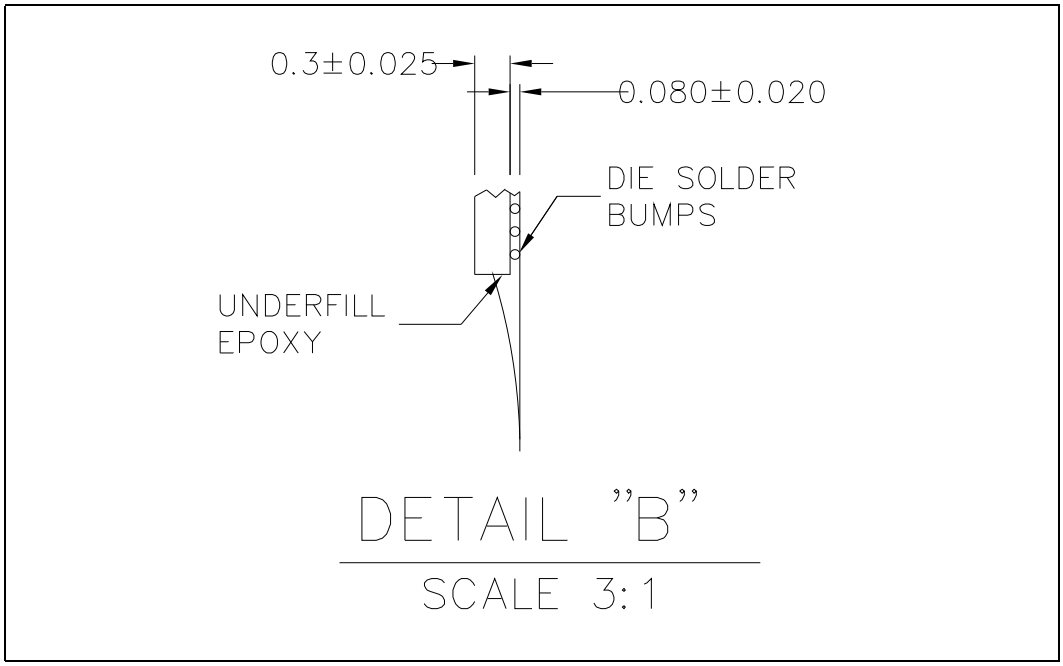
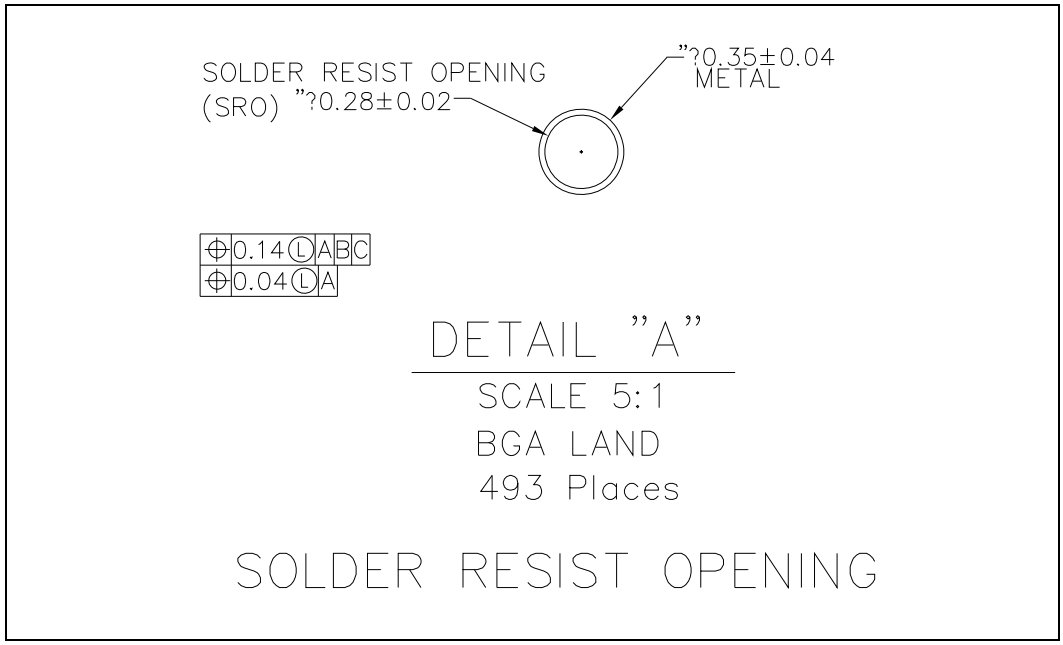


Figure 7-6. Intel® Platform Controller Hub MP30 Package (Solder Resist Opening)



7.6 Intel® Platform Controller Hub MP30 Ballout Definition and Signal Locations

Table 7-4. Intel® Platform Controller Hub MP30 Ball Map—Signal Locations (1–6)

	6	5	4	3	2	1	
AG	RESERVED15		RESERVED1		RESERVED2	RESERVED9_NCTF	**AG**
AF		RESERVED16			VSS_NCTF	VSS_NCTF	**AF**
AE	VCCADPLL		SNSR_STB				**AE**
AD		FLASH_TRG	SNSR_SS_TRG	VSS		VSS_NCTF	**AD**
AC	SNSR2_STDBY	I2C_1_SCL	KP_DKIN1		KP_DKIN2		**AC**
AB	SNSR1_STDBY	I2C_1_SDA	KP_DKIN0	KP_MKIN1		KP_MKIN2	**AB**
AA	VSS	VSS	VSS		KP_MKIN4		**AA**
Y	KP_MKIN3	KP_MKIN5		KP_MKIN6		KP_MKOUT1	**Y**
W	VSS	VSS	VSS		VSS		**W**
V	KP_MKOUT0	KP_MKOUT3		KP_MKOUT2		KP_MKOUT5	**V**
U	VSS	VSS	VSS		KP_MKOUT6		**U**
T	I2C_0_SCL	I2C_0_SDA		GPIO59		GPIO60	**T**
R	VSS	VSS	VSS		VSS		**R**
P	PWRGOOD	I2C_2_SDA		I2C_2_SCL		GPIO61	**P**
N	VSS	VSS	VSS		VR_COMP		**N**
M	SPI_2_SDO	SPI_2_SS1		SPI_2_SS0		EXIT_STDBY	**M**
L	VSS	VSS	VSS		RESET_OUT#		**L**
K	SPI_0_SS3	SPI_0_SS2		HV_RCOMP		SRFWEN#	**K**
J	VSS	VSS	PWR_DMIDVO		PWR_DMIDVO		**J**
H	SPI_1_SS1	SPI_0_SDO		SPI_0_SS0		SPI_0_SS1	**H**
G	VSS	VSS	VSS		VSS		**G**
F	VSS	SPI_1_CLK	SPI_1_SDO		SPI_1_SS2	SPI_0_CLK	**F**
E	BCLKP	VSS	VSS		SPI_1_SS0		**E**
D		VCC_HCLK33	RESERVED6	VCC_HCLK		RESERVED3	**D**
C	VSS		VSS				**C**
B		RESERVED5			VSS_NCTF	RESERVED4	**B**
A	CDMI_TXSTBP		VSS_NCTF		VSS_NCTF		**A**
	6	5	4	3	2	1	

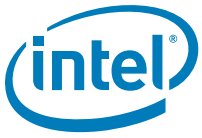


Table 7-5. Intel® Platform Controller Hub MP30 Ball Map—Signal Locations (7-13)

	13	12	11	10	9	8	7	
AG		HDMI_CLK_DN		RESERVED11		RESERVED12		**AG**
AF	VSS		VSS		RESERVED10		RESERVED13	**AF**
AE		HDMI_CLK_DP		RESERVED18		RESERVED17		**AE**
AD	VSS		VSS		VSS		VSS	**AD**
AC	HDMIDATA2_DP	VSS	HDMIVSS	RESERVED14	VSS	VSS	SCLK25	**AC**
AB	HDMIDATA1_DP	HDMICOMP	VCCHDMIBG	RESERVED33	VSS	VSSADPLL	VSS	**AB**
AA	VSS	HDMIDATA0_DN	VSS	HDMIVCC3	VSS	PRE_FLASH_TRG		**AA**
Y	VSS	HDMIDATA0_DP	VSS	HDMIVCC3	VSS	SNSR_RESET#	KP_DKIN3	**Y**
W						VSS	VSS	**W**
V	VCC12	VSS	VSS	PWR_CSB		KP_MKIN0	KP_MKIN7	**V**
U		VSS		PWR_KBDMISC		VSS	VSS	**U**
T	VSS		VSS			KP_MKOUT4	KP_MKOUT7	**T**
R	VSS	VCC12		PWR_KBDMISC		VSS	VSS	**R**
P		VSS	VSS			PMIC_INTR	RESET#	**P**
N	VSS	VSS	VSS	VSS	PWR_PMIC	VSS	VSS	**N**
M						SPI_2_SDI	SPI_2_CLK	**M**
L	VSS	VCC25	VSS	PWR_SPI1	PWR_SPI0	VSS	VSS	**L**
K	VSS	PWR_DMIDVO		PWR_ADMIDVO		SPI_1_SS3	SPI_0_SDI	**K**
J		VSS	PWR_DMIDVO			VSS	VSS	**J**
H	CDMI_TXCHAR#	CDMI_GVREF	VSS	VSSAHPLL	VSS	VCCAHPLL	SPI_1_SDI	**H**
G	VSS	CDMI_TXD5	VSS	CDMI_CVREF	VSS	OSC_IN		**G**
F	VSS	CDMI_TXD0	VSS	CDMI_RCOMP	VSS	VSS	OSC_OUT	**F**
E	VSS	CDMI_RXD3	VSS	CDMI_TXD6	VSS	CDMI_TXSTBN	BCLKN	**E**
D	CDMI_RXD7		CDMI_RXD0		CDMI_TXD2		VSS	**D**
C		VSS		VSS		VSS		**C**
B	CDMI_RXD4		CDMI_TXDPWR#		CDMI_TXD4		CDMI_TXD1	**B**
A		CDMI_RXD1		CDMI_TXD7		CDMI_TXD3		**A**
	13	12	11	10	9	8	7	

Table 7-6. Intel® Platform Controller Hub MP30 Ball Map—Signal Locations (14–20)

	20	19	18	17	16	15	14	
AG	BT_CSI_DATA7		MIPI_CSI_DQN1		MIPI_CSI_CLKP		MIPI_CSI_DQN0	AG
AF		BT_CSI_DATA5		VSS		VSS		AF
AE	BT_CSI_DATA8		MIPI_CSI_DQP1		MIPI_CSI_CLKN		MIPI_CSI_DQP0	AE
AD		VSS		VSS		VSS		AD
AC	BT_CSI_DATA6	VSS	BT_CSI_DATA4	BT_CSI_DATA3	HDMI_HOTPLUG	VSS	HDMIDATA2_DN	AC
AB	I2S_1_TXD	BT_CSI_CLK	BT_CSI_HSYNC	BT_CSI_DATA2	MIPI_CSI_RCOMP	VSS	HDMIDATA1_DN	AB
AA	I2S_0_TXD	VSS	BT_CSI_VSYNC	VSS	BT_CSI_DATA0	VSS	RESERVED32	AA
Y	VCCA_USB33	VSS	VCC12	VSS	BT_CSI_DATA1	VSS	VCCHDMI	Y
W	VSS							W
V	PWR_I2S	VSS	VSS	PWR_BT	VSS	VCC12	VSS	V
U	VCCA_USB25		VCCA_USB25		VSS		VSS	U
T	PWR_SD0	VSS		VSS		VSS		T
R	FLSH_0_IO7		PWR_SD0	PWR_SD0		VCC12		R
P	FLSH_0_IO4		PWR_SDIO2		VSS		VCC12	P
N	VSS	PWR_FLSH0	VSS	PWR_FLSH0	VSS	VSS	VSS	N
M	PWR_FLSH0							M
L	VSS	PWR_FLSH1	VSS	PWR_FLSH1	VSS	VSS	VSS	L
K	PWR_FLSH1		PWR_CPU		PWR_DMIDVO	PWR_DMIDVO		K
J	VSS			VSS	VSS		PWR_DMIDVO	J
H	FLSH_1_IO1	TDO	TCK	VSS	CDVO_GVREF	CDVO_STALL_N	VSS	H
G	FLSH_1_WP#	VSS	CDVO_CVREF	VSS	CDVO_TXD1	VSS	CDMI_RXD5	G
F	VSS	VSS	CDVO_TXD5	VSS	CDMI_RXDPWR#	VSS	CDMI_RXD2	F
E	TRST#	VSS	CDVO_TXD2	VSS	CDVO_TXSP	VSS	CDMI_RXSTBP	E
D		CDVO_TXPWR_N		CDVO_TXD0		CDVO_VBLNK		D
C	VSS		VSS		VSS		VSS	C
B		CDVO_TXD3		CDVO_TXSN		CDMI_RXSTBN		B
A	TMS		CDVO_TXD4		CDMI_RXCHAR#		CDMI_RXD6	A
	20	19	18	17	16	15	14	

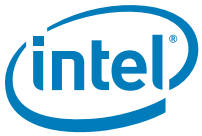


Table 7-7. Intel® Platform Controller Hub MP30 Ball Map—Signal Locations (21–27)

	27	26	25	24	23	22	21	
AG	VSS_NCTF	VSS_NCTF	VSS_NCTF			I2S_1_RXD		**AG**
AF	VSS_NCTF	VSS_NCTF			I2S_0_RXD	BT_CSI_DATA 9		**AF**
AE				USB_DP2		I2S_1_SYNC		**AE**
AD	VSS_NCTF		USB_DP1	USB_DN2	VSS		VSS	**AD**
AC		USB_DP0		USB_DN1	VSS	I2S_1_CLK	VSS	**AC**
AB	OTG_DN		USB_DN0	USB_RCOMP	VSS	I2S_0_SYN	VSS	**AB**
AA		OTG_DP		VSS	RESERVED7	VSS		**AA**
Y	SD0_DATA6		OTG_VBUS		SD0_CD#	OTG_ID	I2S_0_CLK	**Y**
W		SD0_CMD		SD0_CLK	VSS	VSS	VSS	**W**
V	SD0_DATA2		SD0_DATA4	SDO_DATA5	SD0_DATA7	SD0_WP	VSS	**V**
U		SD0_DATA3		VSS	VSS	VSS	VSS	**U**
T	SDIO2_DAT3		SDIO2_CLK		SD0_DATA0	SD0_DATA1	PWR_SD0	**T**
R		SDIO2_CMD		VSS	VSS	VSS	VSS	**R**
P	SDIO2_DAT2		SDIO2_DAT0		SDIO2_DAT1	FLSH_0_IO6	FLSH_0_IO5	**P**
N		FLSH_0_IO3		VSS	VSS	VSS	VSS	**N**
M	FLSH_0_IO2		FLSH_0_IO0		FLSH_0_WP#	FLSH_0_WE#	FLSH_0_ALE	**M**
L		FLSH_0_IO1		VSS	VSS	VSS	VSS	**L**
K	FLSH_0_CLE		FLSH_2_CE#		FLSH_1_CE#	FLSH_1_RE#	PWR_FLSH1	**K**
J		FLSH_3_CE#		VSS	VSS	VSS	VSS	**J**
H	FLSH_0_CE#		FLSH_0_RE#		VSS	FLSH_1_IO3	FLSH_1_IO2	**H**
G		FLSH_RB3#		VSS	FLSH_1_IO5	FLSH_1_IO4		**G**
F	FLSH_RB2#		FLSH_RB1#	FLSH_1_IO6	FLSH_1_WE#	VSS	VSS	**F**
E		FLSH_RB0#		VSS	VSS	PWRMODE0	BSEL1	**E**
D	VSS_NCTF		FLSH_1_IO7	FLSH_1_CLE	FLSH_1_ALE		TDI	**D**
C				FLSH_1_IO0		VSS		**C**
B	VSS_NCTF	VSS_NCTF			PWRMODE2		TEST	**B**
A	RESERVED8_ NCTF	VSS_NCTF		VSS_NCTF		PWRMODE1		**A**
	27	**26**	**25**	**24**	**23**	**22**	**21**	

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