CMOS –Inverters
Lecture 2

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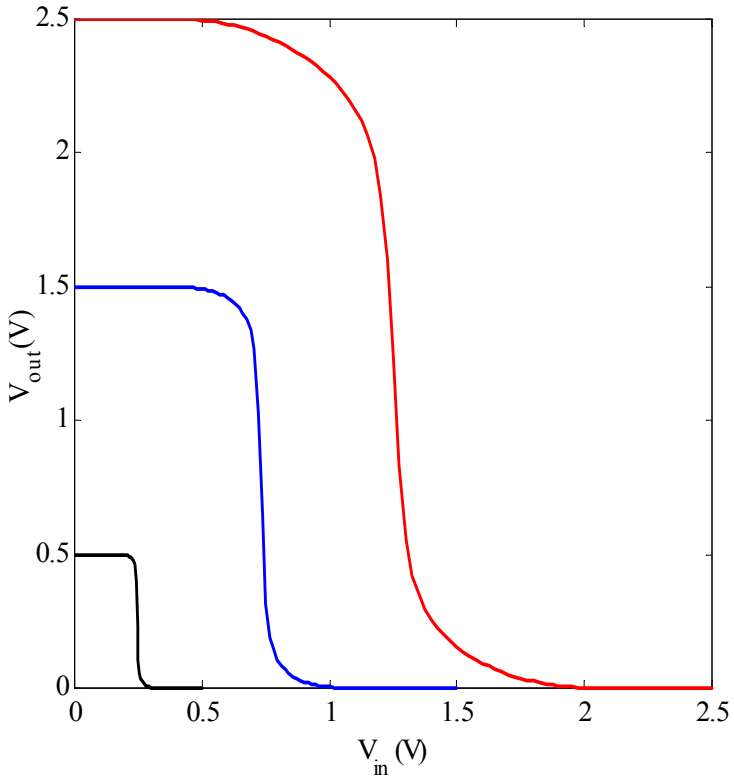
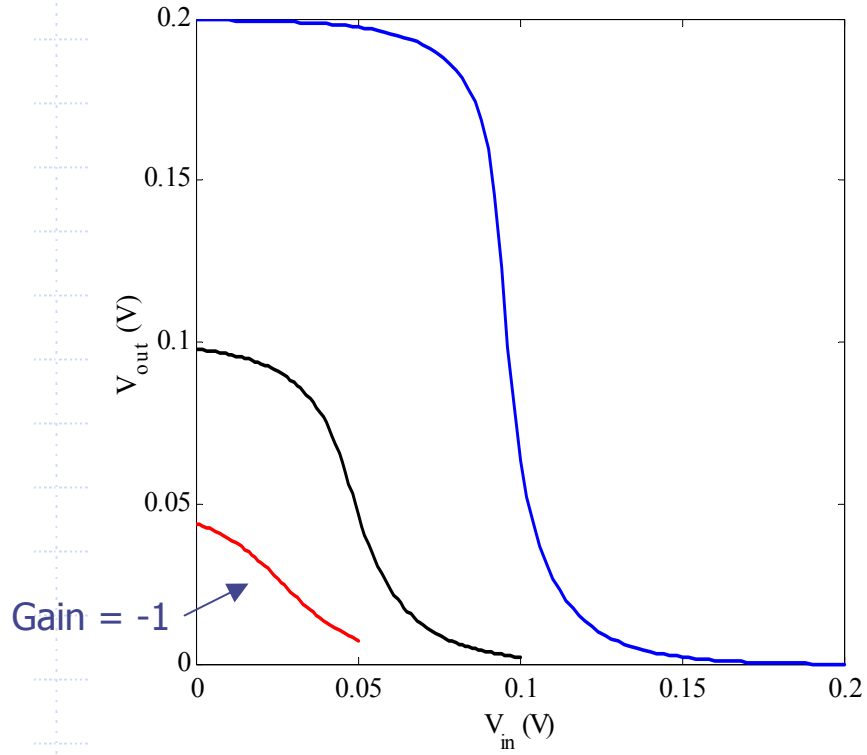
Supply Voltage Effects

Gain as a Function of V_{DD}





The gain can be improved by lowering the supply voltage, however, below a few tenths of a volt, the gain deteriorates.

Effects of Reducing the Supply Voltage

- Gain improves
- Energy dissipation is lowered
- Reduces internal noise (crosstalk)

- dc characteristics become sensitive to variations in device parameters
- Increases sensitivity to external noise
- **Increases the propagation delay times!**

Supply Voltage Effect on Propagation Delay

Average equivalent resistance during the load capacitance discharge.

$$R_{eq} = \frac{1}{V_{DD}/2}\int_{V_{DD}/2}^{V_{DD}} \frac{V}{I_{Dsat}(1+\lambda V)}dV \approx \frac{3V_{DD}}{4I_{Dsat}}\left(1-\frac{7\lambda V_{DD}}{9}\right)$$

$$I_{Dsat} = k'\frac{W}{L}\left[(V_{DD}-V_t)V_{DSsat} - \frac{V_{DSsat}^2}{2}\right]$$

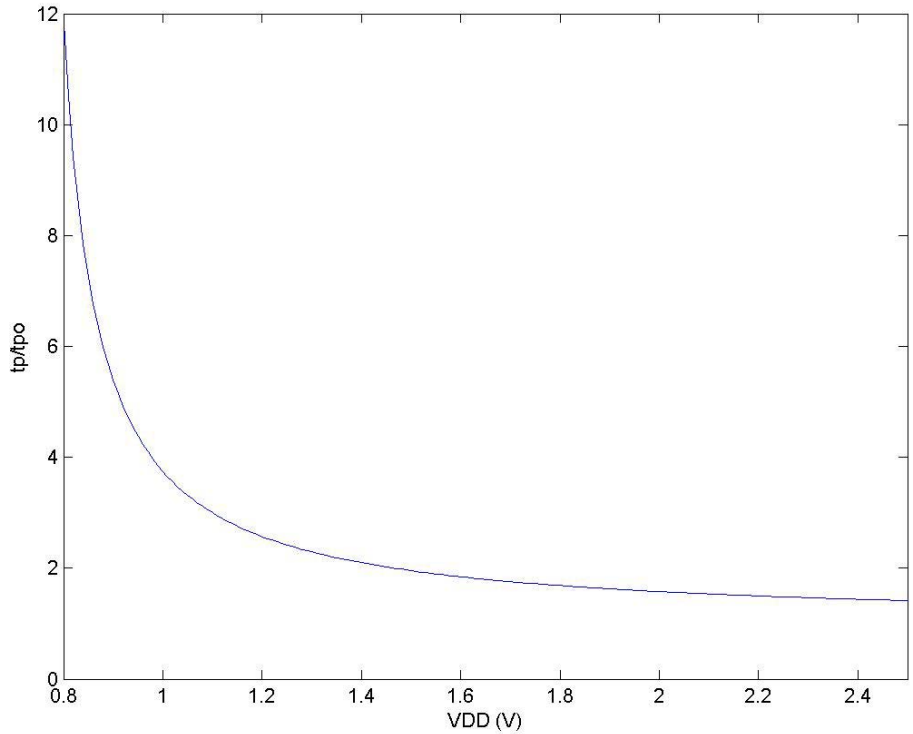
Ignoring channel-length modulation factor:

$$t_{pHL} = 0.69R_{eqn}C_{L-HL} = 0.69\frac{3C_LV_{DD}}{4I_{Dsatn}} = 0.52\frac{C_LV_{DD}}{(W_n/L_n)k_n'V_{Dsatn}(V_{DD}-V_{Tn}-V_{Dsatn}/2)}$$

$$t_{pHL} = t_{po}\times\frac{V_{DD}}{V_{DD}-V_{Tn}-V_{Dsatn}/2}$$

Supply Voltage Effect on Propagation Delay

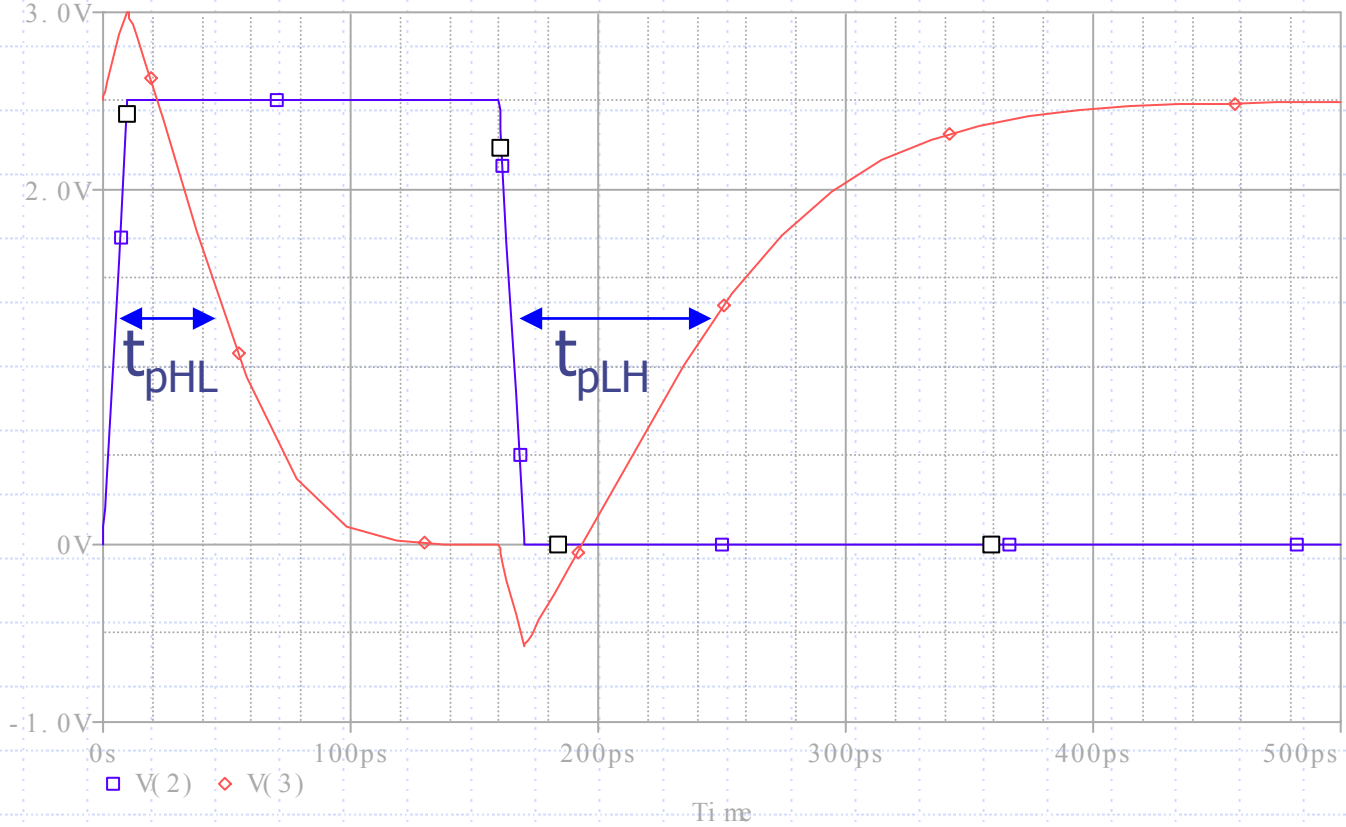
$$t_{pHL} = t_{po} \times \frac{V_{DD}}{V_{DD} - V_{Tn} - V_{Dsatn}/2} = t_{po} \times \frac{V_{DD}}{V_{DD} - 0.733}$$



Note that supply voltages below 1.1 V cause an enormous increase in the propagation delay.

Propagation Delay Effects from Sizing

Transient Response



```
A CMOS Inverter
*
.MODEL nch NMOS
+ LEVEL=3 PHI=0.70 TOX=1.0E-08 XJ=0.20U TPG=1
+ VTO=0.8 DELTA=2.5E-01 LD=4.0E-08 KP=1.88E-04
+ UO=545 THETA=2.5E-01 RSH=2.1E+01 GAMMA=0.62
+ NSUB=1.4E+17 NFS=7.1E+11 VMAX=1.9E+05 ETA=2.2E-02
+ KAPPA=9.7E-02 CGDO=3.7E-10 CGSO=3.7E-10 CGBO=4.0E-10
+ CJ=5.4E-04 MJ=0.6 CJSW=1.5E-10 MJSW=0.3 PB=0.99
*
.MODEL pch PMOS
+ LEVEL=3 PHI=0.70 TOX=1.0E-08 XJ=0.20U TPG=-1
+ VTO=-0.9 DELTA=2.5E-01 LD=6.7E-08 KP=4.45E-05
+ UO=130 THETA=1.8E-01 RSH=3.4E+00 GAMMA=0.52
+ NSUB=9.8E+16 NFS=6.5E+11 VMAX=3.1E+05 ETA=1.8E-02
+ KAPPA=6.3E+00 CGDO=3.7E-10 CGSO=3.7E-10 CGBO=4.3E-10
+ CJ=9.3E-04 MJ=0.5 CJSW=1.5E-10 MJSW=0.3 PB=0.95
*
M1 3 2 0 0 nch W=4u L=0.6u AS=7.2p PS=7.6u AD=7.2p PD=7.6u
M2 3 2 1 1 pch W=5.5u L=0.6u AS=9.9p PS=9.1u AD=9.9p PD=9.1u
CL 3 0 0.006pF
*
VDD 1 0 2.5V
VIN 2 0 PULSE(0 2.5 0 10p 10p 150p 1n)
*
.TRAN 0.005n 1n
*
.DC VIN 0V 2.5V 0.01V
*
.PROBE
*
.END
```

NMOS/PMOS Ratios

For equal resistance values, the width ratio, $\beta = W_p/W_n$, should be 3 to 3.5. If symmetry and reduced noise margins are not primary, then reducing the PMOS channel width can reduce the propagation delay.

Consider two identical cascaded inverters where the drain diffusion capacitances of the first inverter and the gate capacitances of the second inverter plus the interconnect capacitance between them are included :

$$C_L = (C_{dp1} + C_{dn1}) + (C_{gp2} + C_{gn2}) + C_W$$

NMOS/PMOS Ratios

When the PMOS are made β times larger than the NMOS, then all capacitances scale the same way.

$$C_L = (1+\beta)(C_{dn1} + C_{gn2}) + C_W$$

Propagation delay then becomes: (where R_{eqn} and R_{eqp} are resistances of identically sized transistors):

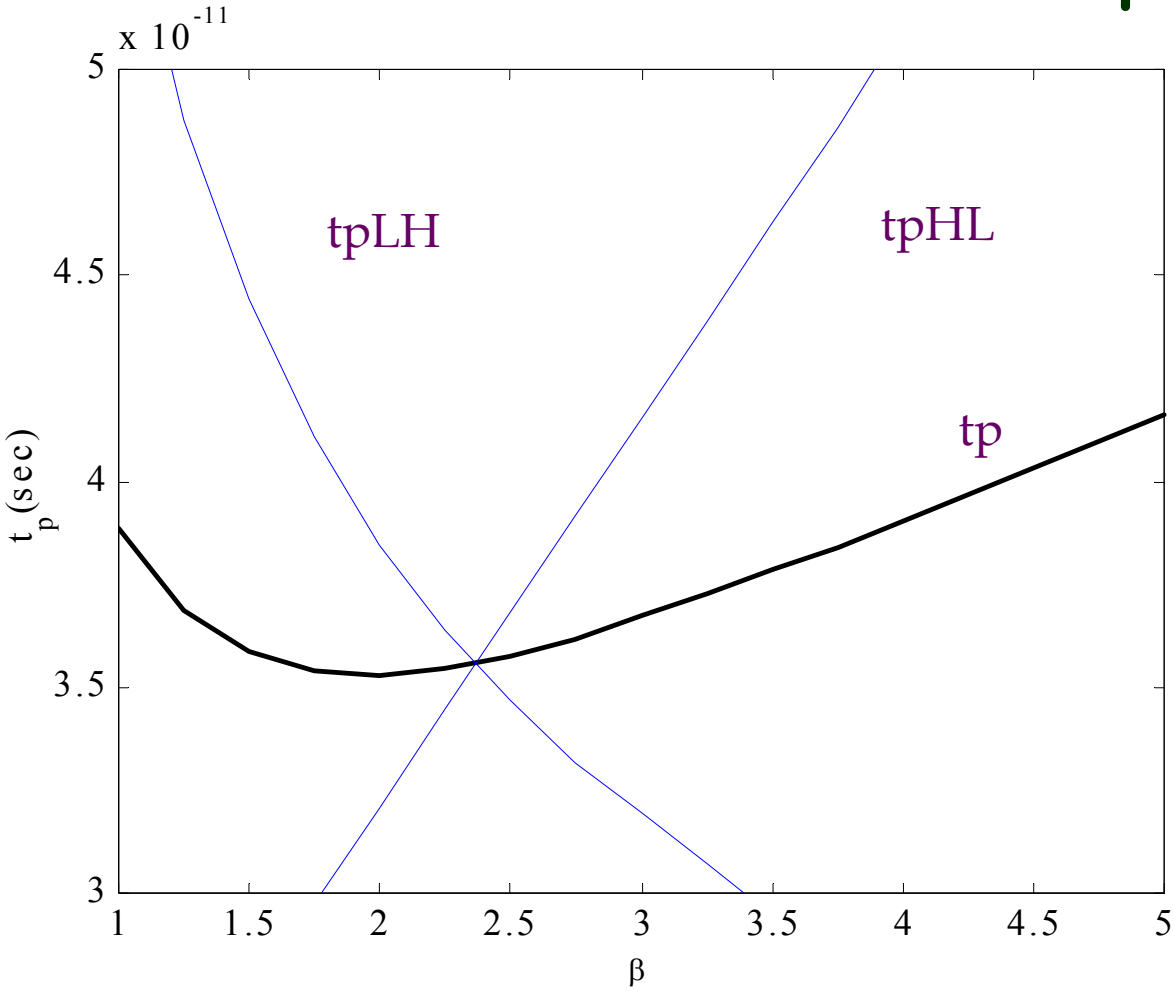
$$t_p = \frac{0.69}{2}[(1+\beta)(C_{dn1} + C_{gn2}) + C_W]\left(R_{eqn} + \frac{R_{eqp}}{\beta}\right)$$

Optimal β then becomes :

$$\beta_{opt} = \sqrt{\frac{R_{eqp}}{R_{eqn}}\left(1 + \frac{C_W}{C_{dn1} + C_{gn2}}\right)}$$

$$\frac{\partial t_p}{\partial \beta} = 0$$

NMOS/PMOS Ratio Effects on Propagation Delay



The smallest delay is for β=1.9. Equal propagation delays require β=2.4.

Inverter Sizing

- Assume a symmetrical inverter (PMOS and NMOS are sized to give identical rise and fall times).

- Load capacitance can be divided into intrinsic and extrinsic components: $C_L = C_{\text{int}} + C_{ext}$

- Intrinsic capacitance represents the intrinsic output capacitance of the inverter or the self-loading.
  - It is composed of the diffusion capacitances of transistors and gate-drain overlap (Miller) capacitances.
- Extrinsic capacitance is the extrinsic load capacitance made up of the input gate capacitances (fan-out) and wiring capacitance.

Inverter Sizing

- Let R_{eq} be the equivalent resistance of the gate. Then the propagation delay is:

$$t_p = 0.69R_{eq}(C_{\text{int}} + C_{ext}) = 0.69R_{eq}C_{\text{int}}(1 + C_{ext}/C_{\text{int}}) = t_{po}(1 + C_{ext}/C_{\text{int}})$$

t_{po} is the intrinsic or unloaded delay.

Sizing a Chain of Inverters

- Increasing an inverter's size decreases the delay, but it increases the input capacitance. The intrinsic output capacitance is proportional to the gate capacitance and both are proportional the transistor/inverter sizing.

$$C_{\text{int}} = \eta C_g$$

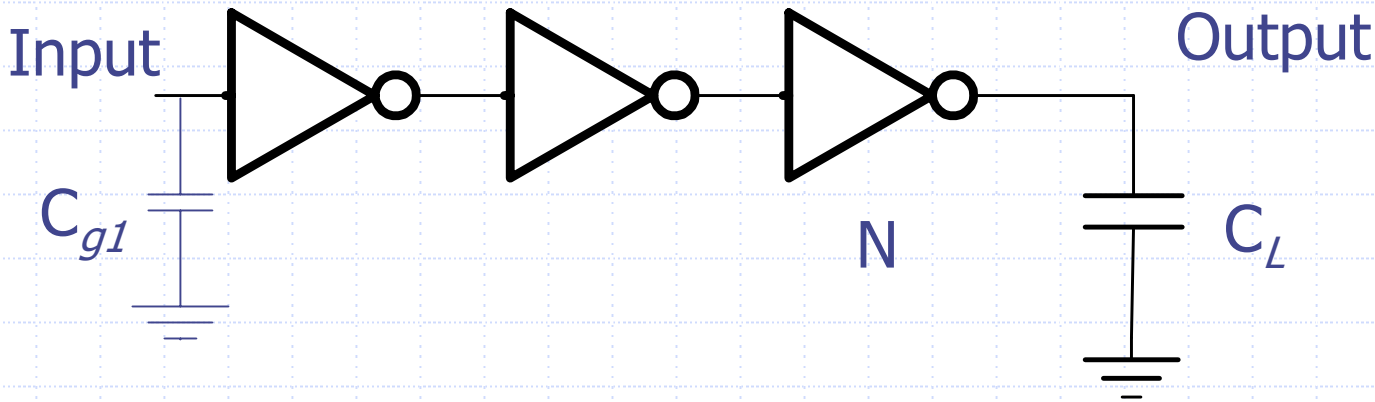
η is the proportionality factor and is near to unity in value.

Sizing of Inverter Chain

Therefore, the delay of an inverter is only a function of the ratio, *f*, between its external load capacitance and its input capacitance!!

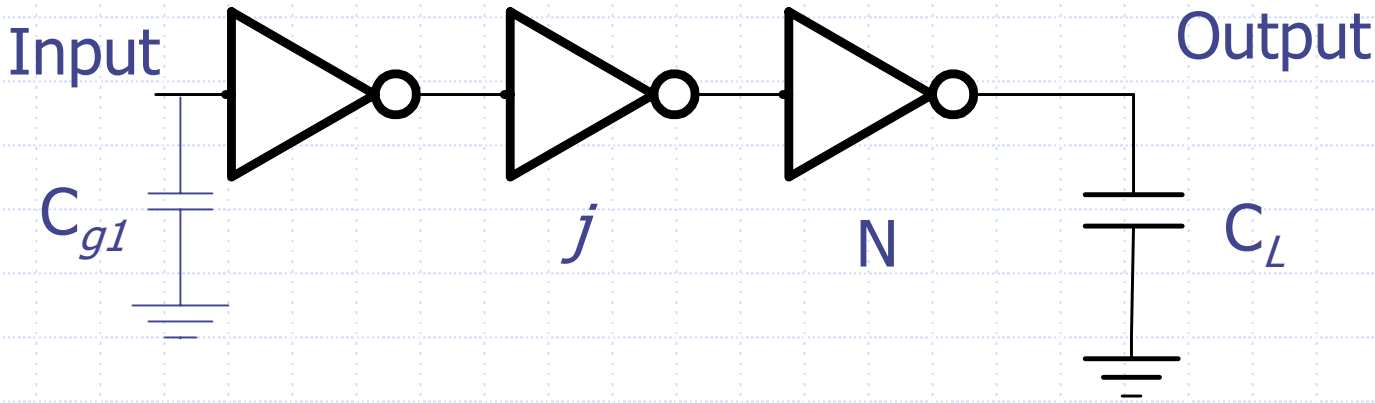
$$t_p = t_{po}(1 + C_{ext}/\eta C_g) = t_{po}(1 + f/\eta)$$

Inverter Chain Sizing



C_{g1} is the input capacitance of the 1st inverter.
C_L is the load capacitance at the end of the fixed chain.

Inverter Chain Sizing



Delay expression for the j^{th} stage is:

$$t_{p,j} = t_{po}(1 + C_{g,j+1}/\eta C_{g,j}) = t_{po}(1 + f_j/\eta)$$

Total delay for the chain is:

$$t_p = \sum_{j=1}^{N} t_{p,j} = t_{po} \sum_{j=1}^{N} (1 + C_{g,j+1}/\eta C_{g,j})$$

For $C_{g,N+1} = C_L$

Inverter Chain Sizing

$$t_p = \sum_{j=1}^{N} t_{p,j} = t_{po} \sum_{j=1}^{N} (1 + C_{g,j+1} / \eta C_{g,j})$$

There are N-1 unknowns, given C_{g1} and C_L. The minimum delay is found by taking N-1 partial derivatives and setting them each to 0:

$$\partial t_p / \partial C_{g,j} = 0$$

Result is:

$$C_{g,j+1} / C_{g,j} = C_{g,j} / C_{g,j-1}$$

Or:

$$C_{g,j} = \sqrt{C_{g,j-1} C_{g,j+1}}$$

Inverter Chain Sizing

$$C_{g,j} = \sqrt{C_{g,j-1} C_{g,j+1}}$$

This expression means that each inverter in the chain is sized up by the same factor, *f*, with respect to the preceding gate, has the same effective fan-out ($f_j = f$), and therefore the same delay.

Thus, given $C_{g,1}$ and C_L, the sizing factor for each stage to give the same delay through each stage, and the minimal total delay is:

$$f = \sqrt[N]{C_L / C_{g,1}} \equiv \sqrt[N]{F}$$

Inverter Chain Sizing

The minimal delay through the inverter chain is then:

$$t_p = N t_{po} (1 + \sqrt[N]{F} / \eta)$$

F represents the overall effective fan-out of the circuit and is equal to:

$$F = C_L / C_{g,1}$$

Inverter Chain Sizing: The Problem Posed One way

Usually $C_{g,1}$ is associated with a minimally-sized gate.

$$t_p = N t_{po} (1 + \sqrt[N]{F} / \eta)$$

For a given F (*e.g.* given a load capacitance to drive from a minimally-sized gate), what is the number of stages that obeys the minimal propagation delay expression derived above?

If N is too large then the first term dominates (intrinsic delay of the stages dominates). If N is too small then the effective fan-out of each stage becomes too large and the second term dominates.

Inverter Chain Sizing: The Solution

Differentiate the delay expression with respect to N and set to 0.

$$\partial t_p / \partial N = t_{po}(1 + \sqrt[N]{F}/\eta) + Nt_{po}(\ln F)\left(\frac{\sqrt[N]{F}}{\eta}\right)\left(\frac{-1}{N^2}\right) = 0$$

$$F = f^N = e^{N(1+\eta/f)}$$

$$\sqrt[N]{F} = f = e^{(1+\eta/f)}$$

Inverter Chain Sizing: The Solution

Given the first gate (usually minimally-sized), then we know its input capacitance, $C_{g,1}$ and its intrinsic output capacitance, C_{int}.

$$\eta = C_{\text{int}} / C_{g,1}$$

Knowing η, iteratively solve for f using the derived expression:

$$f = e^{(1+\eta/f)}$$

We know the load capacitance we are trying to drive, C_L, so we also know $F = C_L / C_{g,1}$.

Inverter Chain Sizing: The Solution

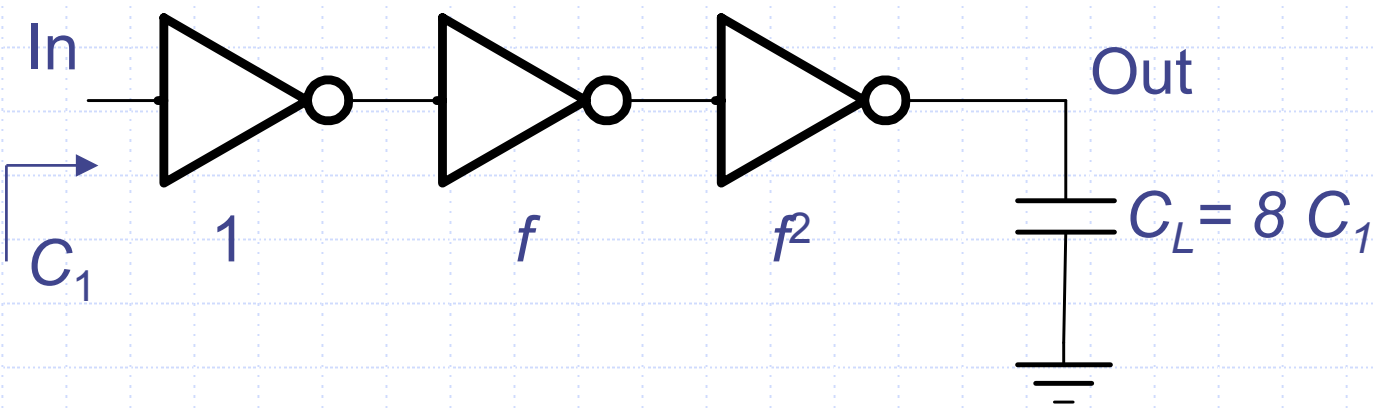
Finally, having values for *f* and *F*, we can find N; the number of stages needed to drive the load capacitance that gives a minimal propagation delay of the signal through the stages.

$$f = \sqrt[N]{F}$$

Also, we can compute the delay time using the expression previously derived:

$$t_p = N t_{po} (1 + \sqrt[N]{F} / \eta)$$

Example 1



C_L/C_1 has to be evenly distributed across $N = 3$ stages:

$$f = \sqrt[3]{C_L / C_1} = \sqrt[3]{8} = 2$$

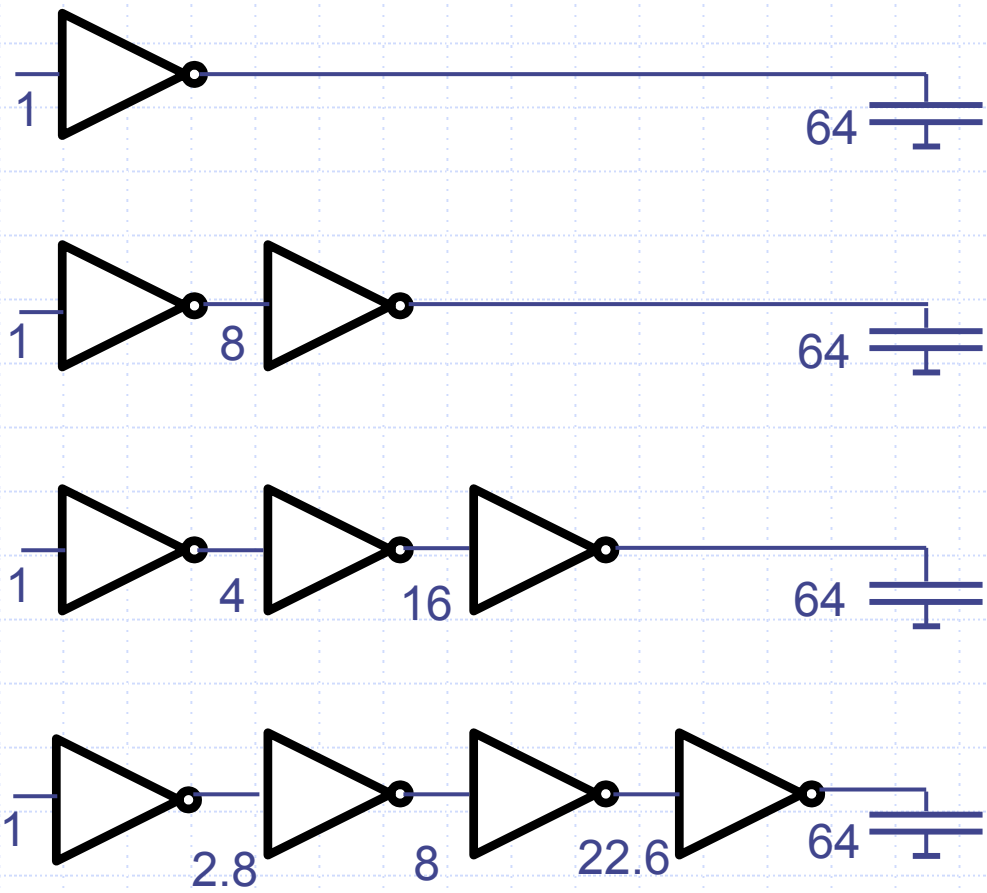
Example 2: Optimum Number of Stages

For a given load, C_L and given input capacitance C_{in}
Find optimal sizing f and minimal delay.

$$C_L = F \cdot C_{in} = f^N C_{in} \quad \text{with} \quad N = \frac{\ln F}{\ln f}$$

$$t_p = N t_{p0}\left(F^{1/N}/\eta + 1\right) = \frac{t_{p0} \ln F}{\eta}\left(\frac{f}{\ln f} + \frac{\eta}{\ln f}\right)$$

Number of Stages to Minimize t_p



N	f	t_p
1	64	65
2	$8=64^{1/2}$	18
3	$4=64^{1/3}$	15
4	$2.8=64^{1/4}$	15.3

Homework #1

- Using the Level-3 CMOS inverter model given above, determine the t_{pHL} and t_{pLH} for 6 to 10 different supply voltage values from 2.5 to 1.1 V.
- Do the simulations again using $L_n=L_p=0.25\ \mu m$, $W_n=2\ \mu m$, and $W_p=4\ \mu m$.
- You will need to modify the VIN values for the pulse and dc analysis as VDD is changed.

Homework #2

- Determine the sizes (f) of the inverters in the circuit below such that the delay time between input and output is minimized. (Hint: First find the ratios between the devices that minimize the delay. You should find that:

$$\frac{4C_{g,2}}{C_{g,1}} = \frac{4C_{g,3}}{C_{g,2}} = \frac{C_L}{C_{g,3}}$$

- Determine the sizes of the inverters if the extra fan-out at each stage is not taken into account.

Homework #2 - Circuit