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Patents

- Disc # 45991, A M&A FOR USING ASYMMETRIC LANES DYNAMICALLY IN PCI-EXPRESS TO SAVE POWER
- Disc # 44757, A M&A FOR COMPRESSION OF HEADERS IN PCI-EXPRESS FOR IMPROVED BANDWIDTH
- Disc# 41361, A M&A FOR MEETING COMPLIANCE FOR DEBUGGING AND TESTING A PCI-EXPRESS LINK AT MULTIPLE SPEEDS
- Disc # 40473, A M&A FOR NEGOTIATING AND CONFIGURING THE SPEED OF A LINK WHERE BOTH ENDS ARE CAPABLE OF SUPPORTING MULTIPLE SPEEDS
- 5,909,556, M&A for exchanging date, status and commands over an hierarchical serial bus assembly using communication packets
- 5,881,252, Method and apparatus for automatically configuring circuit cards in a computer system
- 5,768,542, Method and apparatus for automatically configuring circuit cards in a computer system
- 5,742,847, M&A for dynamically generating and maintaining frame based polling schedules for polling isochronous and asynchronous functions that guaranty latencies and bandwidths to the isochronous functions
- 5,708,849, Implementing scatter/gather operations in a direct memory access device on a personal computer
- 5,694,555, Method and apparatus for exchanging data, status, and commands over an hierarchical serial bus assembly using communication packets
- 5,655,127, Method and apparatus for control of power consumption in a computer system
- 5,623,610, System for assigning geographical addresses in a hierarchical serial bus by enabling upstream port and selectively enabling disabled ports at power on/reset
- 5,615,404, System having independently addressable bus interfaces coupled to serially connected multi-ported signal distributors generating and maintaining frame based polling schedule favoring isochronous peripherals