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Patents

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- 6706584, On-die de-coupling capacitor using bumps or bars and method of making same, 3/16/2004.
- 6703685, Super self-aligned collector device for mono and hetero bipolar junction transistors, 3/9/2004.
- 6686247, Self-aligned contacts to gates, 2/3/2004.
- 6671947, Method of making an interposer, 1/6/2004.
- 6653563, Alternate bump metallurgy bars for power and ground routing, 11/25/2003.
- 6624032, Structure and process flow for fabrication of dual gate floating body integrated MOS transistors, 9/23/2003.
- 6617681, Interposer and method of making same, 9/9/2003.
- 6579771, Self-aligned compact bipolar junction transistor layout, and method of making same, 6/17/2003.
- 6566737, Passivation structure for an integrated circuit, 5/20/2003.
- 6495897, Integrated circuit having etch-resistant layer substantially covering shallow trench regions, 12/17/2002.
- 6392271, Structure and process flow for fabrication of dual gate floating body integrated MOS transistors, 5/21/2002.
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- P. Bai, et al., "A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 um2 SRAM Cell," International Electron Devices Meeting, p. 657, (2004).
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- K. Yu, et al., "HMOS-CMOS — A Low-Power High-Performance Technology," Solid-State Circuits, vol. 16, no. 5, p. 454, (1981).

Professional Affiliations

- National Academy of Engineering member (2005)
- IEEE Fellow
- Senior sponsor for the University of Illinois campus for Intel's Academic Relations group.
- Executive Committee for the VLSI Symposia