Robert S. Chau
Intel Senior Fellow, Technology and Manufacturing Group
Director, Transistor Research and Nanotechnology
INTEL CORPORATION

Patents

- 7,005,366 Tri-gate devices and methods of fabrication
- 6,998,686 Metal-gate electrode for CMOS transistor applications
- 6,974,764 Method for making a semiconductor device having a metal gate electrode
- 6,974,738 Nonplanar device with stress incorporation layer and method of fabrication
- 6,974,733 Double-gate transistor with enhanced carrier mobility
- 6,972,228 Method of forming an element of a microelectronic circuit
- 6,970,373 Method and apparatus for improving stability of a 6T CMOS SRAM cell
- 6,952,040 Transistor structure and method of fabrication
- 6,939,815 Method for making a semiconductor device having a high-k gate dielectric
- 6,933,589 Method of making a semiconductor transistor
- 6,914,295 Tri-gate devices and methods of fabrication
- 6,909,151 Nonplanar device with stress incorporation layer and method of fabrication
- 6,900,481 Non-silicon semiconductor and high-k gate dielectric metal oxide semiconductor field effect transistors
- 6,897,134 Method for making a semiconductor device having a high-k gate dielectric
- 6,897,098 Method of fabricating an ultra-narrow channel semiconductor device
- 6,893,927 Method for making a semiconductor device with a metal gate electrode
- 6,890,807 Method for making a semiconductor device having a metal gate electrode
- 6,887,800 Method for making a semiconductor device with a high-k gate dielectric and metal layers that meet at a P/N junction
- 6,887,762 Method of fabricating a field effect transistor structure with abrupt source/drain junctions
- 6,887,395 Method of forming sub-micron-size structures over a substrate
- 6,885,084 Semiconductor transistor having a stressed channel
- 6,869,889 Etching metal carbide films
- 6,864,145 Method of fabricating a robust gate dielectric using a replacement gate flow

- 6,861,318 Semiconductor transistor having a stressed channel
- 6,858,478 Tri-gate devices and methods of fabrication
- RE38,674 Process for forming a thin oxide layer
- 6,825,506 Field effect transistor and method of fabrication
- 6,812,086 Method of making a semiconductor transistor
- 6,809,017 Interfacial layer for gate electrode and high-k dielectric layer and methods of fabrication
- 6,797,556 MOS transistor structure and method of fabrication
- 6,787,440 Method for making a semiconductor device having an ultra-thin high-k gate dielectric
- 6,777,759 Device structure and method for reducing silicide encroachment
- 6,765,273 Device structure and method for reducing silicide encroachment
- 6,713,358 Method for making a semiconductor device having a high-k gate dielectric
- 6,696,345 Metal-gate electrode for CMOS transistor applications
- 6,696,327 Method for making a semiconductor device having a high-k gate dielectric
- 6,667,251 Plasma nitridation for reduced leakage gate dielectric layers
- 6,667,232 Thin dielectric layers and non-thermal formation thereof
- 6,653,700 Transistor structure and method of fabrication
- 6,645,831 Thermally stable crystalline defect-free germanium bonded to silicon and silicon dioxide
- 6,621,131 Semiconductor transistor having a stressed channel
- 6,620,713 Interfacial layer for gate electrode and high-k dielectric layer and methods of fabrication
- 6,617,210 Method for making a semiconductor device having a high-k gate dielectric
- 6,617,209 Method for making a semiconductor device having a high-k gate dielectric
- 6,610,615 Plasma nitridation for reduced leakage gate dielectric layers
- 6,597,046 Integrated circuit with multiple gate dielectric structures
- 6,566,727 N2O nitrided-oxide trench sidewalls to prevent boron outdiffusion and decrease stress
- 6,541,343 Methods of making field effect transistor structure with partially isolated source/drain junctions
- 6,538,278 CMOS integrated circuit having PMOS and NMOS devices with different gate dielectric layers
- 6,518,155 Device structure and method for reducing silicide encroachment
- 6,514,879 Method and apparatus for dry/catalytic-wet steam oxidation of silicon
- 6,373,112 Polysilicon-germanium MOSFET gate electrodes
- 6,326,664 Transistor with ultra shallow tip and method of fabrication

- 6,261,925 N2O Nitrided-oxide trench sidewalls to prevent boron outdiffusion and decrease stress
- 6,221,789 Thin oxides of silicon
- 6,214,679 Cobalt salicidation method on a silicon germanium film
- 6,198,142 Transistor with minimal junction capacitance and method of fabrication
- 6,191,016 Method of patterning a layer for a gate electrode of a MOS transistor
- 6,165,826 Transistor with low resistance tip and method of fabrication in a CMOS process
- 6,140,251 Method of processing a substrate
- 6,124,171 Method of forming gate oxide having dual thickness by oxidation process
- 6,121,100 Method of fabricating a MOS transistor with a raised source/drain extension
- 6,048,769 CMOS integrated circuit having PMOS and NMOS devices with different gate dielectric layers
- 6,046,494 High tensile nitride layer
- 5,908,313 Method of forming a transistor
- 5,891,809 Manufacturable dielectric formed using multiple oxidation and anneal steps
- 5,856,697 Integrated dual layer emitter mask and emitter trench for BiCMOS processes
- 5,783,478 Method of fabricating a MOS transistor having a composite gate electrode
- 5,780,346 N2O nitrided-oxide trench sidewalls and method of making isolation structure
- 5,763,922 CMOS integrated circuit having PMOS and NMOS devices with different gate dielectric layers
- 5,710,450 Transistor with ultra shallow tip and method of fabrication
- 5,633,202 High tensile nitride layer
- 5,625,217 MOS transistor having a composite gate electrode and method of fabrication
- 5,488,003 Method of making emitter trench BiCMOS using integrated dual layer emitter mask
- 5,434,093 Inverted spacer transistor
- 5,244,843 Process for forming a thin oxide layer

Publications/Speakerships

- S. Datta, T. Ashley, J. Brask, L. Buckle, M. Doczy, M. Emeny, D. Hayes, K. Hilton, R. Jefferies, T. Martin, T.J. Phillips, D. Wallis, P. Wilding and R. Chau, "85nm Gate Length Enhancement and Depletion mode InSb Quantum Well Transistors for Ultra High Speed and very Low Power Digital Logic Applications," International Electron Devices Meeting (IEDM) Technical Digest, 2005, pp. 783-786.
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- R. Chau, J. Brask, S. Datta, G. Dewey, M. Doczy, B. Doyle, J. Kavalieros, B. Jin, M. Metz, A. Majumdar, and M. Radosavljevic, "Emerging Silicon and Non-Silicon Nanoelectronic Devices: Opportunities and Challenges for Future High-Performance and Low-Power Computational Applications," Proceedings of Technical Papers, IEEE VLSI-TSA International Symposium on VLSI Technology, Hsinchu, Taiwan, April 2005, pp. 13-16.
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- Panelist of the 2001 VLSI Technology Symposium Rump Session on "High-K Gate Dielectrics: Is it Necessary? If So, When, What, How?" in Kyoto, Japan — June 2001.
- Panel member of the 2001 International Electron Devices Meeting (IEDM) Panel Discussion on "The 10-nm MOSFET Barrier" in Washington, DC — Dec. 2001.
- Panel member of the 2001 Silicon Nanoelectronics Workshop Panel Discussion on "Prospects of Novel CMOS Device Structures" in Kyoto, Japan — June 2001.
- Speaker of the 5th Topical Research Conference on Reliability on "Advanced Depleted-Substrate Transistors" in Austin, Texas — Oct. 2002.
- Speaker of the 4th International Symposium on Nanostructures and Mesoscopic Systems (NanoMES 2003) on "Silicon Nano-transistors for Logic Applications" in Tempe, Arizona — Feb. 2003.
- Speaker of the 1st Korea-U.S. NanoForum on "Silicon Nano-transistors and Silicon Nanotechnology for High-Performance Logic Applications" in Seoul, Korea — Oct. 2003.
- Speaker of the Nanotechnology Seminar at the Center for Nanotechnology at the University of Washington on "Nano-transistor Research for High-Performance, Low-Power Microprocessor Applications" — May 2003.
- Speaker of the 32nd Annual Northern California Electronic Materials Symposium on "Silicon Nanotechnologies to Extend Moore's Law" — April 2004.
- Panel member of the 4th IEEE Conference on Nanotechnology Panel Discussion on "Teaching Nanotechnology" in Munich, Germany — Aug. 2004.
- Speaker of the Functional Engineered Nano Architectonics (FENA) Collaborative Workshop on "Silicon and Non-Silicon Nanotechnologies for High-Performance and Low-Power Transistor Applications" at UCLA — Dec. 2004.
- Speaker of the 46th TMS Electronic Materials Conference on "New Metal Gate/High-K Dielectric Stacks for Continual Electrical Toxe Scaling and High-Performance CMOS Applications" in Notre Dame, Indiana — June 2004.
- Panelist of the 2004 VLSI Technology Symposium Rump Session on "What's Beyond the Planar MOSFET?" in Honolulu, Hawaii — June 2004.
- Panel member of the 2004 International Electron Devices Meeting (IEDM) Panel Discussion on "Nanoelectronics: Now or Never?" in San Francisco — Dec. 2004.

- Speaker of the 2005 TechMakers Lecture Series at Purdue University on 'Si and Non-Si Nanotechnologies and their Benchmarking for High-Performance, Low-Power Logic Applications' — March 2005
- Speaker of the 2005 IEEE VLSI-TSA International Symposium on VLSI Technology on "Emerging Si and Non-Si Nanoelectronic Devices: Opportunities and Challenges for Future High-Performance and Low-Power Computational Applications" in Hsinchu, Taiwan — April 2005
- Speaker of the 2005 ECE Distinguished Seminar Series at The Ohio State University on "Advanced Si Nanotechnolgies and Emerging Non-Si Nanoelectronic Devices for High-Performance and Low-Power Logic Applications" — March 2005
- Speaker of the Microsystems Technology Laboratories (MTL) VLSI Seminar Series at MIT on "Device Scaling and Technology Challenge for High-Performance Sub-20nm Gate Length Transistors for the 45nm Logic Generation Node" — April 2001
- Speaker of the Solid State Technology and Devices Seminar at the University of California at Berkeley on "Transistor R&D for Logic Applications" — April 2002
- Speaker of the 14th Conference on Insulating Films on Semiconductors (INFOS 2005) on "Enabling Silicon and Non-Silicon Logic Nanotechnology using High-K Gate Dielectrics and Metal Gate Electrodes" in Leuven, Belgium — June 2005

Professional Affiliations

- Fellow of the Institute of Electrical and Electronics Engineers (IEEE).