John Crawford

Intel Corporation
2200 Mission College Blvd.
Santa Clara, CA 95052
(408)-765-4575
john.h.crawford@intel.com

EXPERIENCE: 1977-Present – Intel Corporation, Santa Clara

Intel Fellow: 2002-Present

I provide technical direction to a team of architects and chip developers defining future server microprocessors with an emphaisis on power-efficiency and reliability.

Intel Fellow, Architecture Manager: 1992-2002

I managed a team of architects and software developers responsible for defining Intel's 64-bit microprocessor architectures, and validating their functional completeness and performance. During this time I managed the joint Intel/HP team that defined the Itanium Processor Family instruction set architecture, and directed aspects of Itanium processor product development.

Design Manager, Pentium® Processor: 1989-1992

I co-managed the development of Intel's Pentium microprocessor from its start in late 1989 through samples delivered in 1992. I managed a team of architects, microprogram developers, test developers, and chip design specialists that varied from 20 to 50 over various phases of the project.

Chief Architect, Intel486™ Processor: 1987-1989

I was the chief architect of the Intel486™ microprocessor, responsible for the product specifications, performance analysis, microarchitecture, microprogram development, and test program development. I also contributed to the definition of cache support chips for the Intel486 CPU.

Chief Architect, Intel386™ Processor: 1982-1987

I was the chief architect of the Intel386™ microprocessor, responsible for defining Intel's 32-bit architectural extensions to the already successful 8086/186/286 16-bit product line. After setting the architectural direction, I participated in the design of the processor with responsibility for microarchitecture and microprogram design, and test program generation. I received an Intel Corporate Individual Achievement award in 1986 for defining the Intel386 architecture.

Software Engineer: 1977-1982

I developed a number of software products for the 8086, including assemblers, compilers, and linkers. My biggest technical contribution was the code generation phase of Intel's Pascal compiler for the 8086, for which I received an Intel Corporate Individual Achievement award in 1982.

EDUCATION:

1977 MS Computer Science, U. of North Carolina at Chapel Hill. Thesis topic: "Module Specifications for a Program Optimizer".

1975 ScB Computer Science, Brown University, Providence, Rhode Island. Magna Cum Laude. Rohn Truell Premium in Applied Mathematics.

PROFESSIONAL ACTIVITIES:

IEEE Senior Member

Member of the IEEE 754R Standard committee, 2004-2008.

Member of the NAE Gordon Prize awards committee, 2003-2005.

Member of Hot Chips Symposium Program committee, 2003, 2000, 1991.

Co-Chairman of Hot Chips II Symposium Program committee, 1990.

Coach of Redwood Middle School MathCounts team, 1999 and 2000.

Engineer's Week National All-Star Team, 1994-1996. Engineer's week spokesman for Intel.

Member of the editorial board of IEEE Micro December, 1986 to Sept. 1992.

AWARDS:

March 2002, Elected to National Academy of Engineering, "For the architectural design of widely used microprocessors."

February 2002, Infoworld Top 10 Technology Innovators of the Year 2001.

August 1997, IEEE Computer Society Certificate of Appreciation, "For service to the IEEE Computer Society by serving as a Program o-Chair of the 1990 Hot Chips Symposium"

June 1997, IEEE Ernst Weber Engineering Leadership Recognition, "For leadership in the development of microprocessors for the personal computer industry".

June 1995, ACM/IEEE Eckert-Mauchly Award for contributions to Computer and Digital Systems architecture, "For important contributions to the continuing development of microprocessor architectures and their supporting technology."

December 1993, PC Magazine Technical Excellence Award, Components category, shared with 9 other members of the Pentium® processor team, for the Pentium processor.

June 1993, Peninsula Intellectual Property Lawyers Association "Inventor of the Year" award, "for his Contributions to the Field of Microprocessor Systems".

May 1989, Intel Corporate Achievement Award for protecting Intel's intellectual property in the 387 and Intel386™ processors.

November 1988, PC Magazine "Man of the Year", shared with 5 other members of the Intel386 Design and Manufacturing Team.

Sept. 30, 1986, IEEE Santa Clara Valley Chapter Best Technical Presentation of 1985/86 monthly colloquia series.

May 1986, Intel Corporate Achievement Award for defining the Intel386 architecture.

May 1982, Intel Corporate Achievement Award for developing the 8086 Pascal compiler's code generator.

PATENTS:

1) 7,984,248: Sailesh Kottapalli, John H. Crawford, Kushagra Vaid, “Transaction Based Shared Data Operations in a Multiprocessor Environment”, issued July 19, 2011.

2) 7,937,709: Sailesh Kottapalli, John H. Crawford, “Synchronizing multiple threads efficiently”, issued May 3, 2011.

3) 7,877,666: John H. Crawford, Tsvika Kurts, Moty Mehalel, “Tracking Health of Integrated Circuit Structures”, issued January 25, 2011.

4) 7,669,009: Sailesh Kottapalli, John H. Crawford, “Method and apparatus for run-ahead victim selection to reduce undesirable replacement behavior in inclusive caches”, issued February 23, 2010.

5) 7,607,048: Ugonna C. Echeruo, George Z. Chrysos, John H. Crawford, Shubhendu S. Mukherjee, “Method and Apparatus for Protecting TLB’s VPN from Soft Errors”, issued October 20, 2009.

6) 7,395,415: Gary Hammond, Carl Scafidi, John H. Crawford, “Method and Apparatus to Provide a Source Operand for an Instruction in a Processor”, issued July 1, 2008.

7) 7,395,304: Bharat Bhushan, Vinod Sharma, Edward Grochowski, John H. Crawford, “Method and Apparatus for Performing Single-cycle Addition or Subtraction and Comparison in Redundant Form Arithmetic”, issued July 1, 2008.

8) 7,383,468: Nhon T. Quach, John H. Crawford, Chakravarthy Kosaraju, Venkatesh Nagapudi, “Apparatus and Method for Protecting Critical Resources in High Performance Microprocessor”, issued January 4, 2005.

9) 7,315,920: Nhon Quach, John H. Crawford, Greg S. Mathews, Edward Grochowski, Chakravarthy Kosaraju , “Circuit and Method for Protecting Vector Tags in a Cache in High Performance Microprocessors”, issued January 1, 2008.

10) 7,010,671: John H. Crawford, Donald Alpert, “Computer System and Method for Executing Interrupt Instructions in Two Operating Modes”, issued March 7, 2006.

11) 6,904,502: Nhon Quach, John H. Crawford, Greg S. Mathews, Edward Grochowski, Chakravarthy Kosaraju, “Circuit and Method for Protecting 1-Hot and 2-Hot Vector Tags in High Performance Microprocessors”, issued June 7, 2005.

12) 6,839,814: Nhon T. Quach, John H. Crawford, Greg S. Mathews, Edward Grochowski, Chakravarthy Kosaraju, “Circuit and Method for Protecting 1-Hot and 2-Hot Vector Tags in High Performance Processors”, issued January 4, 2005.

13) 6,826,588: Bharat Bhushan, Edward Grochowski, Vinod Sharma, John H. Crawford, “Method and Apparatus for a Fast Comparison in Redundant Form Arithmetic”, issued November 30, 2004.

14) 6,813,628 : Bharat Bhushan, Edward Grochowski, Vinod Sharma, John H. Crawford, “Method and Apparatus for Performing Equality Comparison in Redundant Form Arithmetic”, issued November 2, 2004.

15) 6,775,746: Nhon T. Quach, John H. Crawford, Greg S. Mathews, Edward Grochowski, Chakravarthy Kosaraju, “Circuit and Method for Protecting 1-Hot and 2-Hot Vector Tags in High Performance Processors”, issued August 10, 2004.

16) 6,763,368 : Bharat Bhushan, Vinod Sharma, Edward Grochowski, John H. Crawford, “Method and Apparatus for Performing Single-Cycle Addition or Subtraction and Comparison in Redundant Form Arithmetic”, issued July 13, 2004.

17) 6,754,689: Bharat Bhushan, Edward Grochowski, John H. Crawford, “Method and Apparatus for Performing Subtraction in Redundant Form Arithmetic”, issued June 22, 2004

18) 6,675,266: Nhon T. Quach, John H. Crawford, Greg S. Mathews, Edward Grochowski, Chakravarthy Kosaraju, “Circuit and Method for Protecting 1-Hot and 2-Hot Vector Tags in High Performance Processors”, issued January 6, 2004.

19) 6,654,909: Nhon T. Quach, John H. Crawford, Chakravarthy Kosaraju, and Venkatesh Nagapudi, "Apparatus and Method for Protecting Critical Resources Against Soft Errors in High Performance Microprocessors", issued November 25, 2003.

20) 6,604,184: Achmed R. Zahir, Gary N. Hammond, and John H. Crawford, "virtual Memory Mapping Using Region-based Page Tables", issued August 5, 2003.

21) 6,542,966: John H. Crawford, Gautam Doshi, Stuart E. Sailer, John Wai Cheong Fu, Gregory S. Mathews, and "Method and Apparatus for Managing Temporal and non-Temporal Data in a Single Cache Structure", issued April 1, 2003.

22) 6,385,718: John H. Crawford and Donald Alpert, "Computer System and Method for Executing Interrupt Instructions in Operating Modes", issued May 7, 2002.

23) 6,163,764: Carole Dulong and John H. Crawford, "Emulation of an Instruction Set on an Instruction Set Architecture Transition", issued December 19, 2000.

24) 5,948,099: John H. Crawford and Mustafiz R. Choudhury, "Apparatus and Method for Swapping the Byte Order of a Data Item to Effectuate Memory Format Conversion", issued September 7, 1999.

25) 5,809,314: Douglas M. Carmean and John H. Crawford, "Method of Monitoring System Bus Traffic by a CPU Operating with Reduced Power", issued September 15, 1998.

26) 5,669,003: Douglas M. Carmean and John H. Crawford, "Method of Monitoring System Bus Traffic by a CPU Operating with Reduced Power", issued September 16, 1997.

27) 5,530,932: Douglas M. Carmean and John H. Crawford, "Cache Coherent Multiprocessing Computer System with Reduced Power Operating Features", issued June 25, 1996.

28) 5,321,836: John H. Crawford and Paul S. Ries, "Virtual Memory Management Method and Apparatus Utilizing Separate and Independent Segmentation and Paging Mechanism", issued June 14, 1994.

29) 5,255,378: John H. Crawford and Edward T. Grochowski, "Method of Transferring Burst Data in a Microprocessor", issued October 19, 1993.

30) 5,210,845: John H. Crawford, Sundaravarathan R. Iyengar, and James Nadir, "Controller for Two-Way Set Associative Cache", issued May 11, 1993.

31) 5,201,043: John H. Crawford and Ashish B. Dixit, "System Using Both a Supervisor Level Control Bit and a User Level Control Bit to Enable/Disable Memory Reference Alignment Checking", issued April 6, 1993.

32) 5,173,872: John H. Crawford and Paul S. Ries, "Content Addressable Memory for Microprocessor System", issued December 22, 1992.

33) 5,131,083: John H. Crawford and Edward T. Grochowski, "Method of Transferring Burst Data in a Microprocessor", issued July 14, 1992.

34) 4,972,338: John H. Crawford and Paul S. Ries, "Memory Management for Microprocessor System", issued November 20, 1990.

BOOKS:

J. Crawford and P. Gelsinger, *"Programming the 80386"*, Sybex Inc., Alameda, CA, 1987.

PUBLICATIONS/CONFERENCES:

Bhat, M., Crawford, J., Morin, R., Shiv, K., “Performance Characterization of Decimal Arithmetic in Commercial Java Workloads”, IEEE International Symposium on Performance Analysis of Systems & Software (ISPASS), 25 April 2007, pp. 54-61.

Cornea, Marius, and Crawford, John, “IEEE 754R Decimal Floating-Point Arithmetic: Reliable and Efficient Implementation for Intel® Architecture Platforms”, Intel Technology Journal, vol. 11, issue 01, Feb. 15, 2007, pp. 91-93.

“IEEE 754 Decimal Floating-Point —— in Binary” talk at Gelato conference, San Jose, CA, April 26, 2006.

J. Crawford, “System Level Design for Soft Errors”, Panel discussion, SELSE-II conference, U. or Illinois, April 12, 2006.

J. Crawford, “1000x in 17 years: Performance growth of Intel® Microprocessors”, NAE Regional Meeting, March 9, 2004.

J. Crawford, “Future of the Supercomputer”, testimony to National Research Council, Washington DC, March 6, 2003.

J. Crawford, “The Billion-Transistor Budget: A Different Kind of Real Estate Development”, Keynote at Microprocessor Forum, October 15, 2002.

J. Crawford, “The Itanium Processor Features for High Availability and Reliability”, Seminar at U. of Washington, Seattle, 10/27/2000.

J. Crawford, “Guest Editor’s Introduction: Introducing the Itanium Processors”, IEEE Micro Vol. 20, No. 5, Sept/Oct 2000, p. 9-11.

J. Crawford and J. Huck, “IA-64 Architecture Innovations”, Intel Developer Forum, February 23, 1999.

J. Crawford and J. Huck, “Next Generation Instruction Set Architecture”, Microprocessor Forum, October 14, 1997.

J. Crawford, “Microprocessors Yesterday to Today”, 25th Anniversary of the Microprocessor Tour, November 1996.

J. Crawford, D. Alpert, Beatrice Fu, “An Overview of Intel’s Pentium Processor”, The Distinguished Lecture Series VI, University Video Communications, June 29, 1993.

J. Crawford, "The P5 Microarchitecture", Microprocessor Forum, Oct. 14-15, 1992, Burlingame, CA.

J. Crawford, "Design Strategies for High-Performance Microprocessors", panel session with Motorola, IBM, HaL, DEC, QED, Sun, and HP at Microprocessor Forum, Oct. 14-15, 1992, Burlingame, CA.

J. Crawford, "What does it mean to be PC Compatible", panel session with AMD, Chips & Technology, and Nexgen at Microprocessor Forum, Nov. 7, 1991, Burlingame, CA.

J. Crawford, "The Execution Pipeline of the Intel i486 CPU", *Proceedings of COMPCON Spring 90*, Feb. 26-March 2, 1990, San Francisco, CA, pp. 254-258.

J. Crawford, "The i486 CPU: Executing Instructions in One Clock Cycle", *IEEE Micro Vol. 10, No. 1 (February 1990)*, pp. 27-36.

J. Crawford, "Intel's i486 Microprocessor", Microprocessor Forum, Sept. 21-22, 1989, San Jose, CA.

J. Crawford, "Overview of the Intel i486 CPU", Santa Clara ACM Chapter, Sunnyvale, CA, August 1989.

J. Crawford, "The Intel i486 CPU", Hot Chips Symposium, June 26-27, 1989, Palo Alto, CA, pp. 9-1 to 9-17.

J. Crawford, "The Intel i486 CPU", Santa Clara IEEE Society Colloquia Series, Cupertino, CA, May 1989.

J. Grimes and J. Crawford, "What Have We Learned from RISC", WESCON/88, session 23/4, Nov. 15-17 1988, Anaheim.

Panel Member, Microprocessors 89 Symposium, San Jose, CA, Nov. 3, 1988.

J. Crawford, "Architecture and Implementation of the Intel 80386 Microprocessor", Boston Computer Society Software Engineering Forum, Boston, MA, May, 1987.

J. Crawford, "Architecture of the Intel 80386", *Proceedings ICCD '86,* IEEE, October 1986, pp. 155-160.

J. Crawford, "Overview of the Intel 80386 Microprocessor", Santa Clara Valley IEEE Colloquia series, Cupertino, CA, May 1986.

R. Childs, J. Crawford, D. House, R. Noyce, "A Microprocessor Family for Personal Computers", *Proceedings of the IEEE,* Vol. 72, No. 3, March 1984, pp. 363-376.

J. Crawford, R. Schue, "Integrating Virtual Memory Management into the CPU", *Proceedings of SOUTHCON Conference,* 1983.

J. Crawford, R. Schue, "Integrating Virtual Memory Management into the CPU", *Proceedings of MIDCON Conference,* 1983.

G. Alexy, B. Childs, J. Crawford, "Integrating Memory Management into the CPU", *Electronic Products,* Oct. 25, 1982, pp. 55-62.

J. Crawford, "Engineering a Production Code Generator", *Proceedings of the SIGPLAN 82 Symposium on Compiler Construction,* Boston, June 23-25, 1982, pp. 205-215.

M. Moore, J. Crawford, et. al., "iAPX 86 System Benchmark Report", Intel Corp. Application Note, February 1982.

J. Crawford, M. Jazayeri, "On Operator Strength Reduction", U. of N. Carolina Technical Report TR 80-003.

J. Crawford, M. Jazayeri, "A New Approach to Code Motion and its Application to Hoisting", *Computer Languages,* Vol. 5, pp. 29-36.

J. Crawford, M. Jazayeri, "Engineering a Program Optimizer", *Proceedings of ACM '78.*

J. Crawford, M. Jazayeri, "Module Specifications for a Program Optimizer", *Proceedings of Southeast Regional ACM conference, 1977.*