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Patents

- 6,675,192, Temporary halting of thread execution until monitoring of armed events to memory location identified in working registers, 1/6/2004
- 6,493,741, Method and apparatus to quiesce a portion of a simultaneous multithreaded central processing unit, 12/10/2002
- 6,470,443, Pipelined multi-thread processor selecting thread instruction in inter-stage buffer based on count information, 10/22/2002
- 6,073,159, Thread properties attribute vector based thread selection in multithreading processor, 6/6/2000
- 5,829,051, Apparatus and method for intelligent multiple-probe cache allocation, 10/27/1998
- 5,349,651, System for translation of virtual to physical addresses by operating memory management processor for calculating location of physical address in memory concurrently with cache comparing virtual addresses for translation, 9/20/1994
- 5,285,323, Integrated circuit chip having primary and secondary random access memories for a hierarchical cache, 2/8/1994
- 5,222,224, Scheme for insuring data consistency between a plurality of cache memories and the main memory in a multi-processor system, 6/22/1993
- 5,222,223, Method and apparatus for ordering and queueing multiple memory requests, 6/22/1993
- 5,175,837, Synchronizing and processing of memory access operations in multiprocessor systems using a directory of lock bits, 12/29/1992
- 5,168,573, Memory device for storing vector registers, 12/1/1992
- 5,155,854, System for arbitrating communication requests using multi-pass control unit based on availability of system resources, 10/13/1992
- 5,148,528, Method and apparatus for simultaneously decoding three operands in a variable length instruction when one of the operands is also of variable length, 9/15/1992
- 5,142,634, Branch prediction, 8/25/1992
- 5,142,631, System for queuing individual read or write mask and generating respective composite mask for controlling access to general purpose register, 8/25/1992
- 5,125,083, Method and apparatus for resolving a variable number of potential memory access conflicts in a pipelined computer system, 6/23/1992
- 5,113,521, Method and apparatus for handling faults of vector instructions causing memory management exceptions, 5/12/1992

- 5,109,495, Method and apparatus using a source operand list and a source operand pointer queue between the execution unit and the instruction decoding and operand processing units of a pipelined data processor, 4/28/1992
- 5,093,775, Microcode control system for digital data processing system, 3/3/1992
- 5,067,069, Control of multiple functional units with parallel operation in a microcoded execution unit, 11/19/1991
- 5,019,965, Method and apparatus for increasing the data storage rate of a computer system having a predefined data path width, 5/28/1991
- 4,995,041, Write back buffer with error correcting capabilities, 2/19/1991
- 4,994,996, Pipelined floating point adder for digital computer, 2/19/1991
- 4,985,825, System for delaying processing of memory access exceptions until the execution stage of an instruction pipeline of a virtual memory system based digital computer, 2/15/1991
- 4,982,402, Method and apparatus for detecting and correcting errors in a pipelined computer system, 1/1/1991
- 4,980,817, Vector register system for executing plural read/write commands concurrently and independently routing data to plural read/write ports, 12/25/1990
- 4,949,250, Method and apparatus for executing instructions for a vector processing system, 8/14/1990
- 4,888,679, Method and apparatus using a cache and main memory for both vector processing and scalar processing by prefetching cache blocks including vector data elements, 12/19/1989
- 4,742,451, Instruction prefetch system for conditional branch instruction for central processor unit, 5/3/1988
- 4,583,222, Method and apparatus for self-testing of floating point accelerator processors, 4/15/1986