Glenn J. Hinton
Intel Fellow, Intel Architecture Group
Director, IA-32 Microarchitecture Development
INTEL CORPORATION

Patents

- 6,735,688, Processor having replay architecture with fast and slow replay paths, 5/11/2004
- 6,721,866, Unaligned memory operands, 4/13/2004
- 6,694,426, Method and apparatus for staggering execution of a single packed data instruction using the same circuit, 2/17/2004
- 6,687,810, Method and apparatus for staggering execution of a single packed data instruction using the same circuit, 2/3/2004
- 6,487,675, Processor having execution core sections operating at different clock rates, 11/26/2002
- 6,425,073, Method and apparatus for staggering execution of an instruction, 7/23/2002
- 6,425,055, Way-predicting cache memory, 7/23/2002
- 6,393,550, Method and apparatus for pipeline streamlining where resources are immediate or certainly retired, 5/21/2002
- 6,378,062, Method and apparatus for performing a store operation, 4/23/2002
- 6,378,061, Apparatus for issuing instructions and reissuing a previous instructions by recirculating using the delay circuit, 4/23/2002
- 6,256,745, Processor having execution core sections operating at different clock rates, 7/3/2001
- 6,230,257, Method and apparatus for staggering execution of a single packed data instruction using the same circuit, 5/8/2001
- 6,216,234, Processor having execution core sections operating at different clock rates, 4/10/2001
- 6,185,671, Checking data type of operands specified by an instruction using attributes in a tagged array architecture, 2/6/2001
- 6,170,038, Trace based instruction caching, 1/2/2001
- 6,105,111, Method and apparatus for providing a cache management technique, 8/15/2000
- 6,101,597, Method and apparatus for maximum throughput scheduling of dependent operations in a pipelined processor, 8/8/2000
- 6,079,014, Processor that redirects an instruction fetch pipeline immediately upon detection of a mispredicted branch while committing prior instructions to an architectural state, 6/20/2000
- 6,047,369, Flag renaming and flag masks within register alias table, 4/4/2000

- » 6,018,786, Trace based instruction caching, 1/25/2000
- » 5,987,600, Exception handling in a processor that performs speculative out-of-order instruction execution, 11/16/1999
- » 5,974,523, Mechanism for efficiently overlapping multiple operand types in a microprocessor, 10/26/1999
- » 5,944,817, Method and apparatus for implementing a set-associative branch target buffer, 8/31/1999
- » 5,918,046, Method and apparatus for a branch instruction pointer table, 6/29/1999
- » 5,913,050, Method and apparatus for providing address-size backward compatibility in a processor using segmented memory, 6/15/1999
- » 5,903,751, Method and apparatus for implementing a branch target buffer in CISC processor, 5/11/1999
- » 5,881,262, Method and apparatus for blocking execution of and storing load operations during their execution, 3/9/1999
- » 5,870,599, Computer system employing streaming buffer for instruction preetching, 2/9/1999
- » 5,860,154, Method and apparatus for calculating effective memory addresses, 1/12/1999
- » 5,854,914, Mechanism to improved execution of misaligned loads, 12/29/1998
- » 5,845,100, Dual instruction buffers with a bypass bus and rotator for a decoder of multiple instructions of variable length, 12/1/1998
- » 5,842,036, Circuit and method for scheduling instructions by predicting future availability of resources required for execution, 11/24/1998
- » 5,828,868, Processor having execution core sections operating at different clock rates, 10/27/1998
- » 5,826,109, Method and apparatus for performing multiple load operations to the same memory location in a computer system, 10/20/1998
- » 5,826,094, Register alias table update to indicate architecturally visible state, 10/20/1998
- » 5,812,839, Dual prediction branch system having two step of branch recovery process which activated only when mispredicted branch is the oldest instruction in the out-of-order unit, 9/22/1998
- » 5,809,325, Circuit and method for scheduling instructions by predicting future availability of resources required for execution, 9/15/1998
- » 5,809,271, Method and apparatus for changing flow of control in a processor, 9/15/1998
- » 5,778,407, Methods and apparatus for determining operating characteristics of a memory element based on its physical location, 7/7/1998
- » 5,778,245, Method and apparatus for dynamic allocation of multiple buffers in a processor, 7/7/1998

- 5,768,576, Method and apparatus for predicting and handling resolving return from subroutine instructions in a computer processor, 6/16/1998
- 5,751,996, Method and apparatus for processing memory-type information within a microprocessor, 5/12/1998
- 5,751,986, Computer system with self-consistent ordering mechanism, 5/12/1998
- 5,751,983, Out-of-order processor with a memory subsystem which handles speculatively dispatched load operations, 5/12/1998
- 5,748,937, Computer system that maintains processor ordering consistency by snooping an external bus for conflicts during out of order execution of memory access instructions, 5/5/1998
- 5,729,728, Method and apparatus for predicting, clearing and redirecting unpredicted changes in instruction flow in a microprocessor, 3/17/1998
- 5,724,536, Method and apparatus for blocking execution of and storing load operations during their execution, 3/3/1998
- 5,721,855, Method for pipeline processing of instructions by controlling access to a reorder buffer using a register file outside the reorder buffer, 2/24/1998
- 5,717,882, Method and apparatus for dispatching and executing a load operation to memory, 2/10/1998
- 5,708,843, Method and apparatus for handling code segment violations in a computer system, 1/13/1998
- 5,706,492, Method and apparatus for implementing a set-associative branch target buffer, 1/6/1998
- 5,694,574, Method and apparatus for performing load operations in a computer system, 12/2/1997
- 5,689,674, Method and apparatus for binding instructions to dispatch ports of a reservation station, 11/18/1997
- 5,687,338, Method and apparatus for maintaining a macro instruction for refetching in a pipelined processor, 11/11/1997
- 5,680,572, Cache memory system having data and tag arrays and multi-purpose buffer assembly with multiple line buffers, 10/21/1997
- 5,680,565, Method and apparatus for performing page table walks in a microprocessor capable of processing speculative instructions, 10/21/1997
- 5,671,444, Methods and apparatus for caching data in a non-blocking manner using a plurality of fill buffers, 9/23/1997
- 5,664,137, Method and apparatus for executing and dispatching store operations in a computer system, 9/2/1997
- 5,627,985, Speculative and committed resource files in an out-of-order processor, 5/6/1997
- 5,623,628, Computer system and method for maintaining memory consistency in a pipelined, non-blocking caching bus request queue, 4/22/1997

- 5,615,385, Method and apparatus for zero extension and bit shifting to preserve register parameters in a microprocessor utilizing register renaming, 3/25/1997
- 5,613,083, Translation lookaside buffer that is non-blocking in response to a miss for use within a microprocessor capable of processing speculative instructions, 3/18/1997
- 5,608,885, Method for handling instructions from a branch prior to instruction decoding in a computer which executes variable-length instructions, 3/4/1997
- 5,606,670, Method and apparatus for signalling a store buffer to output buffered store data for a load operation on an out-of-order execution computer system, 2/25/1997
- 5,604,878, Method and apparatus for avoiding writeback conflicts between execution units sharing a common writeback path, 2/18/1997
- 5,604,877, Method and apparatus for resolving return from subroutine instructions in a computer processor, 2/18/1997
- 5,604,753, Method and apparatus for performing error correction on data from an external memory, 2/18/1997
- 5,588,126, Methods and apparatus for forwarding buffered store data on an out-of-order execution computer system, 12/24/1996
- 5,586,278, Method and apparatus for state recovery following branch misprediction in an out-of-order microprocessor, 12/17/1996 (with David Papworth)
- 5,584,038, Entry allocation in a circular buffer using wrap bits indicating whether a queue of the circular buffer has been traversed, 12/10/1996 (with David Papworth, Andrew F. Glew, Michael A. Fetterman, Robert P. Colwell, Steven J. Griffith, Shantanu R. Gupta, and Narayan Hegde)
- 5,584,037, Entry allocation in a circular buffer, 12/10/1996 (with David Papworth, Andrew F. Glew, Michael A. Fetterman, Robert P. Colwell, Steven J. Griffith, Shantanu R. Gupta, and Narayan Hegde)
- 5,584,001, Branch target buffer for dynamically predicting branch instruction outcomes using a predicted branch history, 12/10/1996 (with Bradley D. Hoyt, Andrew F. Glew, and Subramanian Natarajan)
- 5,577,200, Method and apparatus for loading and storing misaligned data on an out-of-order execution computer system, 11/19/1996 (with Jeffrey M. Abramson, Haitham Akkary, Andrew F. Glew, Kris G. Konigsfeld, Paul D. Madland)
- 5,574,942, Hybrid execution unit for complex microprocessor, 11/12/1996 (with Robert P. Colwell, David B. Papworth, Michael A. Fetterman, Andrew F. Glew, Stephen M. Coward, Grace C. Chen)
- 5,574,871, Method and apparatus for implementing a set-associative branch target buffer, 11/12/1996 (with Bradley D. Hoyt, David B. Papworth, Ashwani

K. Gupta, Michael A. Fetterman, Subramanian Natarajan, Sunil Shenoy, and Reynold D'Sa)

- 5,564,111, Method and apparatus for implementing a non-blocking translation lookaside buffer, 10/8/1996 (with Andrew F. Glew, Haitham Akkary, Robert P. Colwell, David B. Papworth and Michael A. Fetterman)
- 5,564,056, Method and apparatus for zero extension and bit shifting to preserve register parameters in a microprocessor utilizing register renaming, 10/8/1996 (with Michael A. Fetterman, Andrew F. Glew, David B. Papworth, and Robert P. Colwell)
- 5,561,814, Methods and apparatus for determining memory operating characteristics for given memory locations via assigned address ranges, 10/1/1996 (with Andrew F. Glew, David B. Papworth, Michael A. Fetterman, Robert P. Colwell, and Frederick J. Pollack)
- 5,555,432, Circuit and method for scheduling instructions by predicting future availability of resources required for execution, 9/10/1996 (with Robert W. Martell, Michael A. Fetterman, David B. Papworth, and James L. Schwartz)
- 5,553,256, Apparatus for pipeline streamlining where resources are immediate or certainly retired, 9/3/1996 (with Michael A. Fetterman, Robert W. Martell, and David B. Papworth)
- 5,546,597, Ready selection of data dependent instructions using multi-cycle cams in a processor performing out-of-order instruction execution, 8/13/1996 (with Robert W. Martell, Michael A. Fetterman, David B. Papworth, Robert P. Colwell, and Andrew F. Glew)
- 5,526,510, Method and apparatus for implementing a single clock cycle line replacement in a data cache unit, 6/11/1996 (with Haitham Akkary, Mandar S. Joshi, Rob Murray, Brent E. Lince, Paul D. Madland, and Andrew F. Glew)
- 5,519,864, Method and apparatus for scheduling the dispatch of instructions from a reservation station, 5/21/1996 (with Robert W. Martell)
- 5,500,948, Translating instruction pointer virtual addresses to physical addresses for accessing an instruction cache, 3/19/1996 (with Robert M. Riches, Jr.)
- 5,490,280, Apparatus and method for entry allocation for a resource buffer, 2/6/1996 (with Shantanu R. Gupta, and James S. Griffith)
- 5,471,633, Idiom recognizer within a register alias table, 11/28/1995 (with Robert P. Colwell, Andrew F. Glew, David B. Papworth, and David W. Clift)
- 5,452,426, Coordinating speculative and committed state register source data and immediate source data in a processor, 9/19/1995 (with David B. Papworth, Michael A. Fetterman, Robert P. Colwell and Andrew F. Glew)
- 5,448,707, Mechanism to protect data saved on a local register cache during inter-subsystem calls and returns, 9/5/1995 (with Gyanendra Tiwary)
- 5,434,987, Method and apparatus for preventing incorrect fetching of an instruction of a self-modifying code sequence with dependency on a buffered

store, 7/18/1995 (Jeffrey M. Abramson, Haitham Akkary, Andrew F. Glew, Kris G. Konigsfeld, and Paul D. Madland)

- 5,428,811, Interface between a register file which arbitrates between a number of single cycle and multiple cycle functional units, 6/27/1995 (with Frank S. Smith, and Randy Steck)
- 5,423,014, Instruction fetch unit with early instruction fetch mechanism, 6/6/1995 (with Robert M. Riches, Jr.)
- 5,420,991, Apparatus and method for maintaining processing consistency in a computer system having multiple processors, 5/30/1995 (with Kris G. Konigsfeld, Jeffrey M. Abramson, Haitham Akkary, and Andrew F. Glew)
- 5,335,333, Guess mechanism for faster address calculation in a pipelined microprocessor, 8/2/1994 (with Gyanendra Tiwary)
- H1,291, Microprocessor in which multiple instructions are executed in one clock cycle by providing separate machine bus access to a register file for different types of instructions, 2/1/1994 (with Frank S. Smith)
- 5,185,872, System for executing different cycle instructions by selectively bypassing scoreboard register and canceling the execution of conditionally issued instruction if needed resources are busy, 2/9/1993 (with James M. Arnold, and Frank S. Smith)
- 5,023,844, Six-way access ported RAM array cell, June 11, 1991 (with James M. Arnold, and Frank S. Smith)
- 4,811,208, Stack frame cache on a microprocessor chip, March 7, 1989 (with Glenford J. Myers, Konrad Lai, Michael T. Imel, Robert Riches)