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Patents

- 7,877,619 Power mode control method and circuitry
- 7,451,295 Early data return indication mechanism for data cache to detect readiness of data via an early data ready indication by scheduling, rescheduling, and replaying of requests in request queues
- 7,269,711 Methods and apparatus for address generation in processors
- 7,111,153 Early data return indication mechanism
- 6,526,485 Apparatus and method for bad address handling
- 6,484,240 Mechanism for reordering transactions in computer systems with snoop-based cache consistency protocols
- 6,470,435 Dual state rename recovery using register usage
- 6,389,517 Maintaining snoop traffic throughput in presence of an atomic operation a first port for a first queue tracks cache requests and a second port for a second queue snoops that have yet to be filtered
- 6,347,360 Apparatus and method for preventing cache data eviction during an atomic operation
- 6,321,303 Dynamically modifying queued transactions in a cache memory system
- 6,311,254 Multiple store miss handling in a cache memory memory system
- 6,286,082 Apparatus and method to prevent overwriting of modified cache entries prior to write back
- 6,269,427 Multiple load miss handling in a cache memory system
- 6,073,212 Reducing bandwidth and areas needed for non-inclusive memory hierarchy by using dual tags
- 6,029,006 Data processor with circuit for regulating instruction throughput while powered and method of operation
- 5,974,505 Method and system for reducing power consumption of a non-blocking cache within a data processing system
- 5,909,697 Reducing cache misses by snarfing writebacks in non-inclusive memory systems
- 5,897,654 Method and system for efficiently fetching from cache during a cache fill operation
- 5,873,123 Processor and method for translating a nonphysical address into a physical address utilizing a selectively nonsequential search of page table entries

- 5,787,479 Method and system for preventing information corruption in a cache memory caused by an occurrence of a bus error during a linefill operation
- 5,737,751 Cache memory management system having reduced reloads to a second level cache for enhanced memory performance in a data processing system
- 5,721,867 Method and apparatus for executing single beat write store instructions during a cache store linefill operation