## P. Geoffrey Lowney

Intel Fellow, Intel Architecture Group
Director, Compiler and Architecture Advanced Development
INTEL CORPORATION


### Patents

- 6,704,861, Mechanism for executing computer instructions in parallel, 3/9/2004
- 6,470,493, Computer method and apparatus for safe instrumentation of reverse executable program modules, 10/22/2002
- 6,324,689, Mechanism for re-writing an executable having mixed code and data, 11/27/2001
- 6,163,821, Method and apparatus for balancing load vs. store access to a primary data cache, 12/19/2000
- 6,158,049, User transparent mechanism for profile feedback optimization, 12/5/2000
- 5,923,863, Software mechanism for accurately handling exceptions generated by instructions scheduled speculatively due to branch elimination, 7/13/1999
- 5,901,308, Software mechanism for reducing exceptions generated by speculatively scheduled instructions, 5/4/1999
- 5,634,023, Software mechanism for accurately handling exceptions generated by speculatively scheduled instructions, 5/17/1997
- 5,627,981, Software mechanism for accurately handling exceptions generated by instructions scheduled speculatively due to branch elimination, 5/6/1997
- 5,421,022, Apparatus and method for speculatively executing instructions in a computer system, 5/30/1995
- 5,420,990, Mechanism for enforcing the correct order of instruction execution, May 30, 1995.

## Publications

- "Carrier Arrays: An Idiom-preserving Extension to APL," Proceedings of the 8th ACM Symposium on the Principles of Programming Languages, January, 1981.
- "The Multiflow Trace Scheduling Compiler," The Journal of Supercomputing, 7(1/2),1993, pp. 51-142 (with S.M. Freudenberger, T.J. Karzes, W.D. Lichtenstein, R.P. Nix, J.S. O'Donnell, and J.C. Ruttenberg).
- "Avoidance and Suppression of Compensation Code in a Trace Scheduling Compiler," ACM Transactions of Programming Languages and Systems, 16(4), July 1994, pp. 1156-1214 (with S.M. Freudenberger and T.R. Gross).
- "Hot Cold Optimization of Large Windows/NT Applications," MICRO-29, Paris, France, (December, 1996): 80-89 (with R. Cohn).
- "Optimizing Alpha Executables on Windows NT with Spike," Digital Technical Journal, 9(4), 1997, pp. 3-20 (with R. Cohn and D. Goodwin).
- Compiler Writer's Guide for the Alpha 21264. Compaq Computer, June 1999. (with R. Cohn and S. Root).
- "Design and analysis of profile-based optimization in Compaq's compilation tools for Alpha", Journal of Instruction Level Parallelism, vol. 2, May 2000 (with R. Cohn).
- "Code Layout Optimizations for Transaction Processing Workloads", Proceedings of the 28 th Intl. Symposium on Computer Architecture, pp. 155-164, June 2001 (with A. Ramirez, L. Barroso, K. Gharachorloo, R. Cohn, J. Larriba-Pey, M. Valero)
- "Tarantula: A Vector Extension to the Alpha Architecture". Proceedings of the 29th International Symposium on Computer Architecture (ISCA 2002), May 2002 (with R. Espasa, M. Mattina, A. Seznec, F. Ardanaz, J. Emer, S. Felix, J. Gago, R. Gramunt, I. Hernandez, T. Juan)
- "Profile-guided Post-link Stride Prefetching", Proceedings of the 16th International Conference on Supercomputing, June 2002 (with C.K. Luk, R. Muth, H. Patil, R. Weiss, R. Cohn)
- "Ispike: A Post-link Optimizer for the Intel® Itanium® Architecture" Proceedings of the international symposium on Code generation and optimization: feedback-directed and runtime optimization, March 2004 (with C.K. Luk, R. Muth, H. Patil, R. Cohn)