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Patents

- » 8,230,158 Memory devices and methods of storing data on a memory device
7/24/2012
- » 7,835,187 Boosting seed voltage for a memory device 11/16/2010
- » 6,943,071 Integrated memory cell and method of fabrication 9/13/2005
- » 6,518,618, Integrated memory cell and method of fabrication, 2/11/2003
- » 6,376,899, Planar guard ring, 4/23/2002
- » 6,137,155, Planar guard ring, 10/24/2000
- » 5,977,639, Metal staples to prevent interlayer delamination, 11/2/1999
- » 5,566,194, Method and apparatus to improve read reliability in semiconductor memories, 10/15/1996
- » 5,455,800, Apparatus and a method for improving the program and erase performance of a flash EEPROM memory array, 10/3/1995
- » 5,452,311, Method and apparatus to improve read reliability in semiconductor memories, 9/19/1995
- » 5,386,388, Single cell reference scheme for flash memory sensing and program state verification, 1/31/1995
- » 5,377,147, Method and circuitry for preconditioning shorted rows in a nonvolatile semiconductor memory incorporating row redundancy, 12/27/1994
- » 5,347,489, Method and circuitry for preconditioning shorted rows in a nonvolatile semiconductor memory incorporating row redundancy, 9/13/1994
- » 5,339,272, Precision voltage reference, 8/16/1994
- » 5,327,383, Method and circuitry for erasing a nonvolatile semiconductor memory incorporating row redundancy, 7/5/1994
- » 5,309,012, Protected erase voltage discharge transistor in a nonvolatile semiconductor memory, 5/3/1994
- » 5,301,150, Flash erasable single poly EPROM device, 4/5/1994
- » 5,245,570, Floating gate non-volatile memory blocks and select transistors, 9/14/1993
- » 5,239,505, Floating gate non-volatile memory with blocks and memory refresh, 8/24/1993
- » 5,237,535, Method of repairing overerased cells in a flash memory, 8/17/1993
- » 5,220,528, Compensation circuit for leakage in flash EPROM, 6/15/1993
- » 4,963,825, Method of screening EPROM-related devices for endurance failure, 10/16/1990

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- » Li, S.-R.; Lu, Y.-L.R.; McMahon, W.; Yung-Huei Lee; Mielke, N.; RTS and 1/f Noise in Flash Memory, RTS and 1/f Noise in Flash Memory, IEEE Symposium on VLSI Technology, Systems and Applications, 2007
- » Lee, Y.-H.; Mielke, N.; McMahon, W.; Yin-Lung Ryan Lu; Pae, S.; Thin-Gate-Oxide Breakdown and CPU Failure-Rate Estimation, IEEE Trans. Device and Materials Reliability Vol 7, Issue 1, March 2007 Page(s): 74 - 83
- » Lee, Y.-H.; McMahon, W.; Mielke, N.; Yin-Lung Ryan Lu; Walstra, S.; Managing Bias-Temperature Instability for Product Reliability, Managing Bias-Temperature Instability for Product Reliability, IEEE Symposium on VLSI Technology, Systems and Applications, 2007
- » Lee, Y.-H.; Mielke, N.; Agostinelli, M.; Gupta, S.; Lu, R.; McMahon, W.; Prediction of Logic Product Failure Due To Thin-Gate Oxide Breakdown, IEEE Reliability Physics Symposium, 2006 Page(s): 18 - 28
- » Mielke, N.; Belgal, H.P.; Fazio, A.; Meng, Q.; Righos, N.; Recovery Effects in the Distributed Cycling of Flash Memories, IEEE Reliability Physics Symposium, 2006 Page(s): 29 - 35
- » Gu, C.; Kwasnick, R.F.; Mielke, N.R.; Monroe, E.M.; Shirley, C.G.; Ambient Use-Condition Models for Reliability Assessment, IEEE Reliability Physics Symposium, 2006 Page(s): 299 - 306
- » Mielke, N.; Belgal, H.; Kalastirsky, I.; Kalavade, P.; Kurtz, A.; Qingru Meng; Righos, N.; Jie Wu; Flash EEPROM threshold instabilities due to charge trapping during program/erase cycling, Device and Materials Reliability, IEEE Transactions on Volume 4, Issue 3, Sept. 2004 Page(s):335 - 344
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- » Rangan, S.; Mielke, N.; Yeh, E.C.C.; Universal recovery behavior of negative bias temperature instability [PMOSFETs] Electron Devices Meeting, 2003. IEDM '03 Technical Digest. IEEE International 8-10 Dec. 2003 Page(s):14.3.1 - 14.3.4
- » Yung-Huei Lee; Mielke, N.; Sabi, B.; Stadler, S.; Nachman, R.; Hu, S.; Effect of pMOST bias-temperature instability on circuit reliability performance, Electron Devices Meeting, 2003. IEDM '03 Technical Digest. IEEE International 8-10 Dec. 2003 Page(s):14.6.1 - 14.6.4
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