

Randy Mooney

Intel Fellow, Intel Labs
Director, I/O Research
INTEL CORPORATION

Patents

- » 5,623,644, Point-To-Point Phase-Tolerant Communication, 4/22/1997
- » 5,410,267, 3.3v To 5v Supply Interface Buffer, 4/25/1995
- » 5,604,450, High Speed Bidirectional Signaling Scheme, 2/18/1997
- » 5,546,023, Daisy Chained Clock Distribution Scheme, 8/13/1996
- » 6,087,847, Impedance Control Circuit, 7/11/2000
- » 5,905,391, Master-Slave Delay Locked Loop For Accurate Delay Or Non-Periodic Signals, 5/18/1999
- » 6,452,428, Slew Rate Control Circuit, 9/17/2002
- » 6,744,287, Slew Rate Control Circuit, 6/1/2004
- » 6,798,265, Low Jitter External Clocking, 9/28/2004
- » 6,411,151, Low Jitter External Clocking, 6/25/2002
- » 6,453,422, Reference Voltage Distribution For Multiload I/O Systems, 9/17/2002
- » 6,594,769, Reference Voltage Distribution For Multiload I/O Systems, 7/15/2003
- » 6,351,191, Differential Delay Cell With Common Delay Control And Power Supply, 2/26/2002
- » 6,348,811, Apparatus And Methods For Testing Simultaneous Bi-Directional I/O Circuits, 2/19/2002
- » 6,639,426, Apparatus For Testing Simultaneous Bi-Directional I/O Circuits, 10/28/2003
- » 6,377,103, Symmetric, Voltage-Controlled Cmos Delay Cell With Closed-Loop Replica Bias, 4/23/2002
- » 6,348,826, Digital Variable-Delay Circuit Having Voltage-Mixing Interpolator And Methods Of Testing Input/Output Buffers Using Same, 2/19/2002
- » 6,362,657, Small Aperture Latch For Use With A Differential Clock, 3/26/2002
- » 6,377,108, Low Jitter Differential Amplifier With Negative Hysteresis, 4/23/2002
- » 6,304,141, Complementary Input Self-Biased Differential Amplifier With Gain Compensation, 10/16/2001
- » 6,424,175, Biased Control Loop Circuit For Setting Impedance Of Output Driver, 7/23/2002
- » 6,445,170, Current Source With Internal Variable Resistance And Control Loop For Reduced Process Sensitivity, 9/3/2002
- » 6,812,757, Phase Lock Loop Apparatus, 11/2/2004

- » 6,420,912, Voltage To Current Converter, 7/16/2002
- » 6,448,811, Integrated Circuit Current Reference, 9/10/2002
- » 6,741,107, Synchronous Clock Generator For Integrated Circuits, 5/25/2004
- » 6,373,289, Data And Strobe Repeater Having A Frequency Control Unit To Re-Time The Data And Reject Delay Variation In The Strobe, 4/16/2002
- » 6,441,649, Rail-To-Rail Input Clocked Amplifier, 8/27/2002
- » 6,437,601, Using A Timing Strobe For Synchronization And Validation In A Digital Logic Device, 8/20/2002
- » 6,538,502, High Bandwidth Switched Capacitor Input Receiver, 3/25/2003
- » 6,456,133, Duty Cycle Control Loop, 9/24/2002
- » 6,747,474, Integrated Circuit Stubs In A Point-To-Point System, 6/8/2004
- » 6,538,584, Transition Reduction Encoder Using Current And Last Bit Sets, 3/25/2003
- » 6,847,617, Systems For Interchip Communication, 1/25/2005
- » 6,536,025, Receiver Deskewing Of Multiple Source Synchronous Bits From A Parallel Bus, 3/18/2003
- » 6,522,174, Differential Cascode Current Mode Driver, 2/18/2003
- » 6,774,678, Differential Cascode Current Mode Driver, 8/10/2004
- » 6,507,225, Current Mode Driver With Variable Equalization, 1/14/2003
- » 6,774,686, Method For Minimizing Jitter Using Matched, Controlled-Delay Elements Slaved To A Closed-Loop Timing Reference, 8/10/2004
- » 6,845,424, Memory Pass-Band Signaling, 1/18/2005
- » 6,529,037, Voltage Mode Bidirectional Port With Data Channel Used For Synchronization, 3/4/2003
- » 6,791,356, Bidirectional Port With Clock Channel Used For Synchronization, 9/14/2004
- » 6,803,790, Bidirectional Port With Clock Channel Used For Synchronization, 10/12/2004
- » 6,501,256, Trimmable Bandgap Voltage Reference, 12/31/2002
- » 6,653,893, Voltage Margin Testing Of A Transmission Line Analog Signal Using A Variable Offset Comparator In A Data Receiver Circuit, 11/25/2003
- » 6,628,168, Multiple Input, Fully Differential, Wide Common-Mode, Folded-Cascode Amplifier, 9/30/2003
- » 6,597,198, Current Mode Bidirectional Port With Data Channel Used For Synchronization, 7/22/2003
- » 6,639,423, Current Mode Driver With Variable Termination, 10/28/2003
- » 6,621,323, Signal Sampling Circuits, Systems, And Methods, 9/16/2003
- » 6,621,330, Discrete-Time Analog Filter, 9/16/2003
- » 6,747,490, Sampling Pulse Generation, 6/8/2004
- » 6,791,399, Discrete-Time Analog Filter, 9/14/2004

Publications

- » Bloechel, Bradley; Borkar, Nitin; Borkar, Shekhar; De, Vivek; Dermer, Gregory; Erraguntla, Vasantha; Govindarajulu, Venkatesh; Haycock, Matthew; Keshavarzi, Ali; Mooney, Randy; Nair, Raj; Narendra, Siva; Pangal, Amaresh; Seligman, Erik; Vangal, Sriram; Wilson, Howard, "1.1V 1GHz Communications Router with On-Chip Body Bias in 150nm CMOS," ISSCC 2002, Session 16, High Speed I/O, 16.4 (paper and presentation).
- » "1264 ISTR IO CircuitsReport," 1264 ISTR I/O Circuits Report - July 16, 2001
- » Haycock, Matt; Mooney, Randy, "3.2GHz 6.4Gb-per-second per Wire Signaling in 0.18um CMOS" 2001 IEEE International Solid-State Circuits Conference.
- » Casper, Bryan; Jaussi, James; Kennedy, Joe; Martin, Aaron; Mooney, Randy, "8Gb-per-second differential simultaneous bidirectional link with 4mV 9ps waveform capture diagnostic capability," ISSCC 2003, Session 4, Clock Recovery And Backplane Transceivers, Paper 4.5 and presentation.
- » Haycock, Matt; Mooney, Randy, "A 2.5Gbs Bidirectional Signaling Technology." (Paper)
- » Haycock, Matt; Mooney, Randy, "A 2.5Gbs Bidirectional Signaling Technology," Hot Interconnects Symposium V, 8/22/1997 (Presentation)
- » Taylor, Greg; Arabi, Tawfik; Jose, Ken; Jones, Jeff; Kim, Songmin; Kuppuswamy, Ravi; Mooney, Randy; Price, Jack; Sarangi, Ananda, "A 2MB, 3.6GB-per-second Back-side Bus Cache for an IA32 450 MHz Microprocessor" 1998 Symposium on VLSI Circuits Digest of Technical Papers.
- » Borkar, Shekhar; Dike, Charles; Mooney, Randy, "A 900 Mb-per-second Bidirectional Signaling Scheme(Presentation)," ISSC95, 2/15/1995.
- » Borkar, Shekhar; Dike, Charles; Mooney, Randy, "A 900 Mb-per-second Bidirectional Signaling Scheme" IEEE Journal of Solid-State Circuits, Vol. 30, No. 12, December 1995.
- » Casper, Bryan; Jaussi, James E.; Kennedy, Joe; Martin, Aaron; and Mooney, Randy, "An 8-GB(per)s simultaneous bidirectional link with on-die waveform capture," IEEE Journal Of Solid-State Circuits, Vol. 38, No. 12, December 2003.
- » Casper, Bryan K.; Haycock, Matthew; Mooney, Randy, "An Accurate and Efficient Analysis Method for Mult-Gb-per-second Chip-to-Chip Signaling Schemes," 2002 Symposium on VLSI Circuits Digest of Technical Papers.
- » Casper, Bryan; Hanumolu, Pavan Kumar; Moon, Un-Ku; Mooney, Randy; Wei, Gu-Yeon; "Analysis of PLL clock jitter in high-Speed Serial Links," IEEE Transactions On Circuits And Systems-II: Analog And Digital Signal Processing, Vol. 50, No. 11, November 2003.
- » Kennedy, Joe; Mooney, Randy; Price, Jack; Wilson, Howard, "Design of a 433MT(per)s Backside Bus" "Gizmo Impedance and Slew Rate Control," 2/15/2005.
- » "IO Techniques and Trends," ISSCC, 2/5/1997.
- » Haycock, Matt; Mooney, Randy, "3.2 GHz, 6.4 Gb/s per wire signaling in a 0.18µm CMOS," ISSCC 2001.

- » "Point-To-Point Signaling Technology," Microcomputer Research Labs 1997 Open House.
- » Haycock, Matt; Mooney, Randy, "Point-to-Point Signaling Test Report," 5/30/1997.
- » Casper, Bryan; Martin, Aaron; Mix, Jason; Mooney, Randy, "Shannon's Limits for Copper/FR4 Interconnect," P1264 I/O ISTR.
- » Burton, Ted; Jex, Jerry; Nag, Prantik; Mooney, Randy, "Split FIFO Phase Synchronization for High Speed Interconnect," IEEE 1995.
- » "Source Synchronous Interfaces," Intel Development Labs.
- » Haycock, Matt; and Mooney, Randy, "Stellar Signalling," MRL Open House, 3/30/1999.