Anand S. Murthy
Intel Fellow, Technology and Manufacturing Group
Director, Strained Silicon Process Technology
Intel Corporation

U.S. Patents

- 7902009, Graded high germanium compound films for strained semiconductor devices
- 7871916, Transistor gate electrode having conductor material layer
- 7858981, Strained NMOS transistor featuring deep carbon doped regions and raised donor doped source and drain
- 7833883, Precursor gas mixture for depositing an epitaxial carbon-doped silicon film
- 7821044, Transistor with improved tip profile and method of manufacture thereof
- 7812394, CMOS transistor junction regions formed by a CVD etching and deposition sequence
- 7732285, Semiconductor device having self-aligned epitaxial source and drain extensions
- 7704833, Method of forming abrupt source drain metal gate transistors
- 7682916, Field effect transistor structure with abrupt source/drain junctions
- 7678631, Formation of strain-inducing films
- 7663192, CMOS device and method of manufacturing same
- 7662689, Strained transistor integration for CMOS
- 7642610, Transistor gate electrode having conductor material layer
- 7517772, Selective etch for patterning a semiconductor film deposited non-selectively
- 7517768, Method for fabricating a heterojunction bipolar transistor
- 7494858, Transistor with improved tip profile and method of manufacture thereof
- 7492017, Semiconductor transistor having a stressed channel
- 7479432, CMOS transistor junction regions formed by a CVD etching and deposition sequence
- 7479431, Strained NMOS transistor featuring deep carbon doped regions and raised donor doped source and drain
- 7473947, Process for ultra-thin body SOI devices that incorporate EPI silicon tips and article made thereby
- 7436035, Method of fabricating a field effect transistor structure with abrupt source/drain junctions
- 7427775, Fabricating strained channel epitaxial source/drain transistors
- 7422971, Process for ultra-thin body SOI devices that incorporate EPI silicon tips and article made thereby

- 7402872, Method for forming an integrated circuit
- 7391087, MOS transistor structure and method of fabrication
- 7364976, Selective etch for patterning a semiconductor film deposited non-selectively
- 7358547, Selective deposition to improve selectivity and structures formed thereby
- 7338873, Method of fabricating a field effect transistor structure with abrupt source/drain junctions
- 7274055, Method for improving transistor performance through reducing the salicide interface resistance
- 7226842, Fabricating strained channel epitaxial source/drain transistors
- 7223679, Transistor gate electrode having conductor material layer
- 7202514, Self aligned compact bipolar junction transistor layout and method of making same
- 7195985, CMOS transistor junction regions formed by a CVD etching and deposition sequence
- 7129139, Methods for selective deposition to improve selectivity
- 7064042, Self aligned compact bipolar junction transistor layout, and method of making same
- 7060576, Epitaxially deposited source/drain
- 7005359, Bipolar junction transistor with improved extrinsic base region and method of fabrication
- 6974733, Double-gate transistor with enhanced carrier mobility
- 6972228, Method of forming an element of a microelectronic circuit
- 6952040, Transistor structure and method of fabrication
- 6949482, Method for improving transistor performance through reducing the salicide interface resistance
- 6933589, Method of making a semiconductor transistor
- 6927140, Method for fabricating a bipolar transistor base
- 6887762, Method of fabricating a field effect transistor structure with abrupt source/drain junctions
- 6885084, Semiconductor transistor having a stressed channel
- 6861318, Semiconductor transistor having a stressed channel
- 6812086, Method of making a semiconductor transistor
- 6797556, MOS transistor structure and method of fabrication
- 6723622, Method of forming a germanium film on a semiconductor substrate that includes the formation of a graded silicon-germanium buffer layer prior to the formation of a germanium layer
- 6703291, Selective NiGe wet etch for transistors with Ge body and/or Ge source/drain extensions
- 6653700, Transistor structure and method of fabrication
- 6621131, Semiconductor transistor having a stressed channel
- 6605498, Semiconductor transistor having a backfilled channel material

- 6579771, Self aligned compact bipolar junction transistor layout, and method of making same
- 6541343, Methods of making field effect transistor structure with partially isolated source/drain junctions
- 6373112, Polysilicon-germanium MOSFET gate electrodes
- 6235568, Semiconductor device having deposited silicon regions and a method of fabrication
- 6214679, Cobalt salicidation method on a silicon germanium film

Selected Publications

- 30 nm physical gate length CMOS transistors with 1.0 ps n-MOS and 1.7 ps p-MOS gate delays. International Electron Devices Meeting 2000. Technical Digest. IEDM p. 45-8.
- A 65nm logic technology featuring 35nm gate lengths, enhanced channel strain, 8 Cu interconnect layers, low-k ILD and 0.57 μm2 SRAM cell. 2004 International Electron Devices Meeting (IEEE Cat. No.04CH37602). Piscataway, NJ, USA: IEEE, 2005. p. 657-60.
- A 90-nm logic technology featuring strained-silicon. IEEE Transactions on Electron Devices, vol.51, no.11, Nov. 2004. p. 1790-7.
- A logic nanotechnology featuring strained-silicon. IEEE Electron Device Letters, vol.25, no.4, April 2004. p. 191-3.
- Delaying forever: Uniaxial strained silicon transistors in a 90nm CMOS technology. 2004 Symposium on VLSI Technology. Digest of Technical Papers. Honolulu, HI, USA, 15-17 June 2004
- High performance fully-depleted tri-gate CMOS transistors. IEEE Electron Device Letters, vol.24, no.4, April 2003. p. 263-5.
- A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors. IEEE International Electron Devices Meeting 2003. Pisacataway, NJ, USA: IEEE, 2003. p. 11.6.1-3.
- Integration of mixed-signal elements into a high-performance digital CMOS process. Intel Technology Journal, no.2, 2002
- Transistor elements for 30nm physical gate lengths and beyond. Intel Technology Journal, no.2, 2002.
- A 90 nm logic technology featuring 50 nm strained silicon channel transistors, 7 layers of Cu interconnects, low k ILD, and 1 mu m/sup 2/ SRAM cell. International Electron Devices Meeting. Technical Digest (Cat. No.02CH37358). Piscataway, NJ, USA: IEEE, 2002. p. 61-4.
- A 90 nm communication technology featuring SiGe HBT transistors, RF CMOS, precision R-L-C RF elements and 1 mu m/sup 2/ 6-T SRAM cell. International Electron Devices Meeting. Technical Digest (Cat. No.02CH37358). Piscataway, NJ, USA: IEEE, 2002. p. 73-6.
- High-frequency response of 100 nm integrated CMOS transistors with high-K gate dielectrics. International Electron Devices Meeting. Technical Digest (Cat. No.01CH37224). Piscataway, NJ, USA: IEEE, 2001. p. 10.6.1-4.
- A 50 nm depleted-substrate CMOS transistor (DST). International Electron Devices Meeting. Technical Digest (Cat. No.01CH37224). Piscataway, NJ, USA: IEEE, 2001. p. 29.1.1-4.
- High performance 32 nm logic technology featuring 2nd generation high-k + metal gate transistors. 2009 IEEE International Electron Devices Meeting (IEDM 2009) Pages: 4 pp. Published: 2009.

» High performance hi-k + metal gate strain enhanced transistors on (110) silicon. IEDM 2008. IEEE International Electron Devices Meeting. Technical Digest Pages: 4 pp. Published: 2008
» A 32 nm logic technology featuring 2nd-generation high-k+ metal-gate transistors, enhanced channel strain and 0.171 μ m2 SRAM cell size in a 291 Mb array. IEDM 2008. IEEE International Electron Devices Meeting. Technical Digest Pages: 3 pp. Published: 2008
» Past, Present and Future: SiGe and CMOS Transistor Scaling, ECS Transactions, 33 (6) 3-17, 2010.