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Patents

- 6,393,550, Method and apparatus for pipeline streamlining where resources are immediate or certainly retired, 5/21/2002
- 6,349,380, Linear address extension and mapping to physical memory using 4 and 8 byte page table entries in a 32-bit microprocessor, 2/19/2002
- 6,101,597, Method and apparatus for maximum throughput scheduling of dependent operations in a pipelined processor, 8/8/2000
- 6,079,014, Processor that redirects an instruction fetch pipeline immediately upon detection of a mispredicted branch while committing prior instructions to an architectural state, 6/20/2000.
- 5,987,600, Exception handling in a processor that performs speculative out-of-order instruction execution, 11/16/1999.
- 5,974,523, Mechanism for efficiently overlapping multiple operand types in a microprocessor, 10/26/1999
- 5,944,817, Method and apparatus for implementing a set-associative branch target buffer, 8/31/1999
- 5,918,046, Method and apparatus for a branch instruction pointer table, 6/29/1999
- 5,913,050, Method and apparatus for providing address-size backward compatibility in a processor using segmented memory, 6/15/1999
- 5,903,751, Method and apparatus for implementing a branch target buffer in CISC processor, 5/11/1999
- 5,842,036, Circuit and method for scheduling instructions by predicting future availability of resources required for execution, 11/24/1998
- 5,826,109, Method and apparatus for performing multiple load operations to the same memory location in a computer system, 10/20/1998
- 5,826,094, Register alias table update to indicate architecturally visible state, 10/20/1998
- 5,812,839, Dual prediction branch system having two step of branch recovery process which activated only when mispredicted branch is the oldest instruction in the out-of-order unit, 9/22/1998
- 5,809,325, Circuit and method for scheduling instructions by predicting future availability of resources required for execution, 9/15/1998
- 5,809,271, Method and apparatus for changing flow of control in a processor, 9/15/1998
- 5,778,407, Methods and apparatus for determining operating characteristics of a memory element based on its physical location, 7/7/1998

- 5,778,245, Method and apparatus for dynamic allocation of multiple buffers in a processor, 7/7/1998
- 5,768,576, Method and apparatus for predicting and handling resolving return from subroutine instructions in a computer processor, 6/16/1998
- 5,751,986, Computer system with self-consistent ordering mechanism, 5/12/1998
- 5,751,983, Out-of-order processor with a memory subsystem which handles speculatively dispatched load operations, 5/12/1998
- 5,729,728, Method and apparatus for predicting, clearing and redirecting unpredicted changes in instruction flow in a microprocessor, 3/17/1998
- 5,721,855, Method for pipeline processing of instructions by controlling access to a reorder buffer using a register file outside the reorder buffer, 2/24/1998
- 5,717,882, Method and apparatus for dispatching and executing a load operation to memory, 2/10/1998
- 5,706,492, Method and apparatus for implementing a set-associative branch target buffer, 1/ 6/1998
- 5,687,338, Method and apparatus for maintaining a macro instruction for refetching in a pipelined processor, 11/11/1997
- 5,627,985, Speculative and committed resource files in an out-of-order processor, 5/6/1997
- 5,615,385, Method and apparatus for zero extension and bit shifting to preserve register parameters in a microprocessor utilizing register renaming, 3/25/1997
- 5,606,670, Method and apparatus for signalling a store buffer to output buffered store data for a load operation on an out-of-order execution computer system, 2/25/1997
- 5,604,878, Method and apparatus for avoiding writeback conflicts between execution units sharing a common writeback path, 2/18/1997
- 5,604,877, Method and apparatus for resolving return from subroutine instructions in a computer processor, 2/8/1997
- 5,604,753, Method and apparatus for performing error correction on data from an external memory, 2/18/1997
- 5,588,126, Methods and apparatus for forwarding buffered store data on an out-of-order execution computer system, 12/24/1996
- 5,586,278, Method and apparatus for state recovery following branch misprediction in an out-of-order microprocessor, 12/17/1996
- 5,584,038, Entry allocation in a circular buffer using wrap bits indicating whether a queue of the circular buffer has been traversed, 12/10/1996
- 5,584,037, Entry allocation in a circular buffer, 12/10/1996
- 5,574,942, Hybrid execution unit for complex microprocessor, 11/12/1996
- 5,574,871, Method and apparatus for implementing a set-associative branch target buffer, 11/12/1996

- 5,564,111, Method and apparatus for implementing a non-blocking translation lookaside buffer, 10/8/1996
- 5,564,056, Method and apparatus for zero extension and bit shifting to preserve register parameters in a microprocessor utilizing register renaming, 10/8/1996
- 5,561,814, Methods and apparatus for determining memory operating characteristics for given memory locations via assigned address ranges, 10/1/1996
- 5,555,432, Circuit and method for scheduling instructions by predicting future availability of resources required for execution, 9/10/1996
- 5,553,256, Apparatus for pipeline streamlining where resources are immediate or certainly retired, 9/3/1996
- 5,546,597, Ready selection of data dependent instructions using multi-cycle cams in a processor performing out-of-order instruction execution, 8/13/1996
- 5,471,633, Idiom recognizer within a register alias table, 11/28/1995
- 5,452,426, Coordinating speculative and committed state register source data and immediate source data in a processor, 9/19/1995
- 5,404,473, Apparatus and method for handling string operations in a pipelined processor, 4/4/1995
- 5,307,506, High bandwidth multiple computer bus apparatus, 4/26/1994
- 5,179,680, Instruction storage and cache miss recovery in a high speed multiprocessing parallel processing apparatus, 1/12/1993
- 5,057,837, Instruction storage method with a compressed format using a mask word, 10/15/1991
- 4,920,477, Virtual address table look aside buffer miss recovery method and apparatus, 4/24/ 1990
- 4,833,599, Hierarchical priority branch handling for parallel execution in a parallel processor, 5/23/1989
- 4,777,594, Data processing apparatus and method employing instruction flow prediction, 10/11/1988
- 4,760,519, Data processing apparatus and method employing collision detection and prediction, 7/26/1988
- 4,561,051, Memory access method and apparatus in multiple processor systems, 12/24/1985
- US5410710, Multiprocessor programmable interrupt controller system adapted to functional redundancy checking processor systems, 4/25/1995