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Patents

- 6907487, Enhanced Highly Pipelined Bus Architecture, 6/14/2005
- 6880031, Snoop Phase In A Highly Pipelined Bus Architecture, 4/12/2005
- 6807592, Quad Pumped Bus Architecture And Protocol , 10/19/2004
- 6804735, Response And Data Phases In A Highly Pipelined Bus Architecture, 10/12/2004
- Re38388, Method And Apparatus For Performing Deferred Transactions, 1/13/2004
- 6609171, Quad Pumped Bus Architecture And Protocol, 8/19/2003
- 6601121, Quad Pumped Bus Architecture And Protocol, 7/29/2003
- 6594756, Multi-Processor System For Selecting A Processor Which Has Successfully Written It's Id Into Write-Once Register After System Reset As The Boot-Strap Processor, 7/15/2003
- 6557071, Memory System Including A Memory Controller Having A Data Strobe Generator And Method For Accessing A Memory Using A Data Storage, 4/29/2003
- 6487655, Computer System Formed With A Processor And A System Board Provided With Complementary Initialization Support, 11/26/2002
- 6446154, Method And Mechanism For Virtualizing Legacy Sideband Signals In A Hub Interface Architecture, 9/3/2002
- 6418496, System And Apparatus Including Lowest Priority Logic To Select A Processor To Receive An Interrupt Message, 7/9/2002
- 6415367, Apparatus For Reducing Asynchronous Service Latency In A Time Slot-Based Memory Arbitration Scheme, 7/2/2002
- 6412060, Method And Apparatus For Supporting Multiple Overlapping Address Spaces On A Shared Bus, 6/25/2002
- 6412049, Method For Minimizing Cpu Memory Latency While Transferring Streaming Data, 6/25/2002
- 6405271, Data Flow Control Mechanism For A Bus Supporting Two-And Three-Agent Transactions, 6/11/2002
- 6401153, Mechanisms For Converting Interrupt Request Signals On Address And Data Lines To Interrupt Message Signals, 6/4/2002
- 6381665, Mechanisms For Converting Interrupt Request Signals On Address And Data Lines To Interrupt Message Signals, 4/30/2002
- 6374321, Mechanisms For Converting Address And Data Signals To Interrupt Message Signals, 4/16/2002

- 6363461, Apparatus For Memory Resource Arbitration Based On Dedicated Time Slot Allocation, 3/26/2002
- 6263397, Mechanism For Delivering Interrupt Messages, 7/17/2001
- 6253302, Method And Apparatus For Supporting Multiple Overlapping Address Spaces On A Shared Bus, 6/26/2001
- 6219741, Transactions Supporting Interrupt Destination Redirection And Level Triggered Interrupt Semantics, 4/17/2001
- 6195712, Dynamic Discovery Of Wireless Peripherals, 2/27/2001
- 6178206, Method And Apparatus For Source Synchronous Data Transfer, 1/23/2001
- 6151663, Cluster Controller For Memory And Data Cache In A Multiple Cluster Processing System, 11/21/2000
- 6148356, Scalable Computer System, 11/14/2000
- 6108735, Method And Apparatus For Responding To Unclaimed Bus Transactions, 8/22/2000
- 5996042, Scalable, High Bandwidth Multicard Memory System Utilizing A Single Memory Controller, 11/30/1999
- 5978737, Method And Apparatus For Hazard Detection And Distraction Avoidance For A Vehicle, 11/2/1999
- 5961621, Mechanism For Efficiently Processing Deferred Order-Dependent Memory Access Transactions In A Pipelined System, 10/5/1999
- 5956516, Mechanism For Converting Interrupt Request Signals On Address And Data Lines To Interrupt Message Signals, 9/21/1999
- 5923857, Method And Apparatus For Ordering Writeback Data Transfers On A Bus, 7/13/1999
- 5919254, Method And Apparatus For Switching Between Source-Synchronous And Common Clock Data Transfer Modes In A Multiple Agent Processing System, 7/6/1999
- 5911053, Method And Apparatus For Changing Data Transfer Widths In A Computer System, 6/8/1999
- 5905876, Queue Ordering For Memory And I/O Transactions In A Multiple Concurrent Transaction Computer System, 5/18/1999
- 5906001, Method And Apparatus For Performing Tlb Shutdown Operations In A Multiprocessor System Without Invoking Interrupt Handler Routines, 5/18/1999
- 5903916, Computer Memory Subsystem And Method For Performing Opportunistic Write Data Transfers During An Access Latency Period Within A Read Or Refresh Operation, 5/11/1999
- 5848279, Mechanism For Delivering Interrupt Messages, 12/8/1998
- 5829052, Method And Apparatus For Managing Memory Accesses In A Multiple Multiprocessor Cluster System, 10/27/1998

- 5812803, A Method And Apparatus For Controlling Data Transfers Between A Bus And A Memory Device Using A Multi-Chip Memory Controller, 9/22/1998
- 5796977, Highly Pipelined Bus Architecture, 8/18/1998
- 5784579, Method And Apparatus For Dynamically Controlling Bus Access From A Bus Agent Based On Bus Pipeline Depth, 7/21/1998
- 5696910, Method And Apparatus For Tracking Transactions In A Pipelined Bus, 12/9/1997
- 5615343, Method And Apparatus For Performing Deferred Transactions, 3/25/1997
- 5550533, High Bandwidth Self-Timed Data Clocking Scheme For Memory Bus Implementation, 8/27/1996
- 5548734, Equal Length Symmetric Computer Bus Topology, 8/20/1996
- 5537640, Asynchronous Modular Bus Architecture With Cache Consistency, 7/16/1996
- 5513331, Method And Apparatus For Automatically Configuring System Memory Address Space Of A Computer System Having A Memory Subsystem With Indeterministic Number Of Memory Units Of Indeterministic Sizes During System Reset, 4/30/1996
- 5471637, Method And Apparatus For Conducting Bus Transactions Between Two Clock Independent Bus Agents Of A Computer System Using A Transaction By Transaction Deterministic Request/Response Protocol And Burst Transfer, 11/28/1995
- 5455957, Method And Apparatus For Conducting Bus Transactions Between Two Clock Independent Bus Agents Of A Computer System, 10/3/1995
- 5301299, Optimize Write Protocol For Memory Accesses Utilizing Row And Column Strobes, 4/5/1994
- 5239638, Two Strobed Memory Access, 8/24/1993

Speakerships

- EMEA Academic Forum, "Where is computing going?" April 2004
- IDF, Beijing, Architecting the Tera-Era Keynote, April 2004
- Peking University, Institute of Computing Technology, "Where is computer going?" April 2004
- IDF, Taipei, Radio Renaissance R&D Keynote, April 2004
- Intel Higher Ed Summit, "Where is computing going?" February 2004
- I/O Horizons, December 2003
- MicroVentures Technology Outlook, December 2003
- MTL Sr. Technical Female, December 2003
- MMT Panel Discussion, November 2003
- WCA Keynote, "Radio Free Intel," November 2003
- Dr. Young, Intel Board Member visit "Radio Free Intel," October 2003
- IDF, San Jose, September 2003
- US State Dept visit "Intel Research Overview" and "Photonics in Communications," August 2003
- Software Strategy Summit, May 2003
- UK House of Lords visit "Intel's Wireless Vision," May 2003
- SLRP Wi-Fi, May 2003
- IDF, Berlin, Intel's Wireless Vision, April 2003
- Mikro-Sys, Keynote Speaker, April 2003
- Nizhny, Intel's Wireless Vision, April 2003
- VEECO TAB Keynote Speaker, March 2003
- IDF, Santa Clara, Intel's Wireless Vision, February 2003
- Meptec RF Conference Keynote Speaker, February 2003
- IEEE Workshop, AZ State University, Future Opportunities in Wireless Communication in 2010, Nov. 2002
- Nizhny-Novgorod State University, Russia, Intel Wireless Research, October 2002
- Russia Academy of Science, Nizhniy-Novgorod, Memory Roadmap Strategy and Challenges for 2003, October 2002
- IEEE TC Computer Elements Wkshp, "Challenges of integrating RF analog circuits in a digital CMOS Process," June 2002
- IDF, Beijing, Challenges of Integrating RF into CMOS Technology, April 2002
- IDF, Taipei, Challenges of Integrating RF into CMOS Technology, April 2002
- Caltech, Challenges of Integrating RF into CMOS Technology, March 2002

Professional Affiliations

- President's Advisory Council, Oregon Institute of Technology
- Mentor to faculty and students, Oregon Institute of Technology
- Advisor to the OGI School of Science & Engineering during its recent merger with Oregon Health & Sciences University
- Saturday Academy Board of Advisors