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Patents

- 6,792,516, Memory arbiter with intelligent page gathering logic, 9/14/2004
- 6,762,765, Bandwidth reduction for zone rendering via split vertex buffers, 7/13/2004
- 6,760,031, Upgrading an integrated graphics subsystem, 7/6/2004
- 6,710,784, Method and apparatus for performing a vertical scale filter function in a graphics device using a single line buffer, 3/23/2004
- 6,639,598, Method and apparatus for effective level of detail selection, 10/28/2003
- 6,466,226, Method and apparatus for pixel filtering using shared filter resource between overlay and texture mapping engines, 10/15/2002
- 6,433,790, Methods and systems for rendering line and point features for display, 8/13/2002
- 6,393,579, Method and apparatus for saving power and improving performance in a collapsible pipeline using gated clocks, 5/21/2002
- 6,330,646, Arbitration mechanism for a computer system having a unified memory architecture, 12/11/2001
- 6,204,857, Method and apparatus for effective level of detail selection, 3/20/2001
- 6,191,793, Method and apparatus for texture level of detail dithering, 2/20/2001
- 6,091,428, Frame buffer memory system for reducing page misses when rendering with color and Z buffers, 7/18/2000
- 6,072,505, Method and apparatus to efficiently interpolate polygon attributes in two dimensions at a prescribed clock rate, 6/6/2000
- 5,367,615, Spatial augmentation of vertices and continuous level of detail transition for smoothly varying terrain polygon density, 11/22/1994
- 4,958,305, Polygon edge clipping, 9/18/1990
- 6,816,167, Anisotropic filtering technique, 11/9/2004
- 6,633,299, Method and apparatus for implementing smart allocation policies for a small frame buffer cache serving 3D and 2D streams, 10/14/2003