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Patents

- 7820550, Negative tone double patterning method
- 7816061, Lithography masks for improved line-end patterning
- 7759028, Sub-resolution assist features
- 7755082, Forming self-aligned nano-electrodes
- 7709866, Method for forming semiconductor contacts
- 7648803, Diagonal corner-to-corner sub-resolution assist features for photolithography
- 7632610, Sub-resolution assist features
- 7572557, Non-collinear end-to-end structures with sub-resolution assist features
- 7521157, Cross-shaped sub-resolution assist feature
- 7374865, Methods to pattern contacts using chromeless phase shift masks
- 7358111, Imageable bottom anti-reflective coating for high resolution lithography
- 7312155, Forming self-aligned nano-electrodes
- 7288344, Accommodating diffraction in the printing of features on a substrate
- 7265431, Imageable bottom anti-reflective coating for high resolution lithography
- 7258965, Pre-exposure of patterned photoresist films to achieve critical dimension reduction during temperature reflow
- 7179570, Chromeless phase shift lithography (CPL) masks having features to pattern large area line/space geometries
- 7056645, Use of chromeless phase shift features to pattern large area line/space geometries
- 6977219, Solvent vapor-assisted plasticization of photoresist films to achieve critical dimension reduction during temperature reflow
- 6968532, Multiple exposure technique to pattern tight contact geometries
- 6927082, Method of evaluating the quality of a contact plug fill
- 6774037, Method integrating polymeric interlayer dielectric in integrated circuits
- 6649515, Photoimageable material patterning techniques useful in fabricating conductive lines in circuit structures
- 6406995, Pattern-sensitive deposition for damascene processing
- 6384481, Single step electroplating process for interconnect via fill and metal line patterning

- 6365529, Method for patterning dual damascene interconnects using a sacrificial light absorbing material
- 6350670, Method for making a semiconductor device having a carbon doped oxide insulating layer
- 6329118, Method for patterning dual damascene interconnects using a sacrificial light absorbing material
- 6037255, Method for making integrated circuit having polymer interlayer dielectric
- 6020266, Single step electroplating process for interconnect via fill and metal line patterning
- 5933759, Method of controlling etch bias with a fixed lithography pattern for sub-micron critical dimension shallow trench applications