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Patents

- 5,636,374, M&A for performing operations based upon the addresses of microinstructions
- 5,724,527, fault-tolerant boot strap mechanism for a multiprocessor system
- 6,708,269, M&A for multi-mode fencing in a microprocessor system
- 6,496,925, M&A for processing an event occurrence within a multithreaded processor
- 7,039,794, M&A for processing an event occurrence within a multithreaded processor
- 7,353,370, Method and apparatus for processing an event occurrence within a multithreaded processor
- 35495/p18869, A technique for broadcasting messages on a point-to-point interconnect
- 40436/p21873, Opportunistic transmission of software state information within a link based computing system
- 35493/p21947, Virtualization of pin functionality in a point-to-point interface
- 44576/p22021, Address space emulation
- 55269/p25429, Creation of logical apic id with cluster id and intra-cluster id
- 57800/p26369, Processor selection for an interrupt based on willingness to accept the interrupt and on priority
- 57801/p26370, Processor selection for an interrupt identifying a processor cluster
- 58443/p27061, Register interface for extended advanced processor interrupt controller