Past, Present and Future: SiGe and CMOS Transistor Scaling

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This paper discusses the historical role that SiGe has played in driving the CMOS scaling roadmap, including discussion of NMOS biaxial strain and PMOS uniaxial strain. The paper also discusses the potential future role that Ge or SiGe may play in CMOS scaling as a high mobility replacement for the Si channel. Challenges such as poor quality germanium oxide and the small Ge bandgap are reviewed in light of recent developments (high-k metal gate, and ultra-thin body devices) in MOSFET scaling.

Introduction

For the past 45 years, relentless focus on Moore's Law transistor scaling has provided ever-increasing CMOS transistor performance and density. For much of this time, Moore's Law transistor scaling meant "classic" Dennard scaling (1) where oxide thickness (T_{ox}), transistor length (L_g) and transistor width (W) were scaled by a constant factor ($1/k$) in order to provide a delay improvement of $1/k$ at constant power density. However, in recent years, Dennard scaling has become less influential, having been supplanted by the use of performance enhancers (such as strain and high-k metal gate). This paper will address the significant role that SiGe has played in the past on enhancing CMOS transistor performance, provide some information on present and developing uses of SiGe for CMOS scaling, and speculate on the role that SiGe will play in future CMOS technology generations.

The Basic Physics

Conduction band:

Pure Si has a conduction band structure formed from 6 equi-energy valleys along principal crystal directions. Pure Ge has a conduction band structure formed from 8 equi-energy valleys along <±1±1±1> crystal directions (see Figure 1).

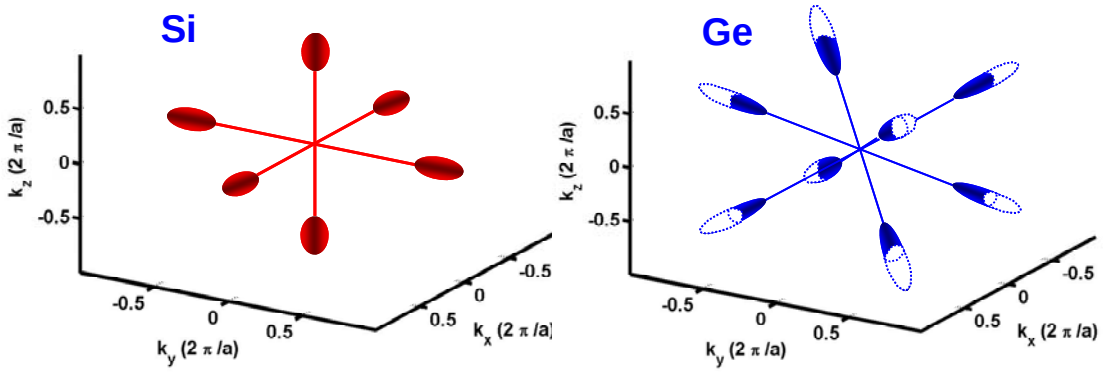
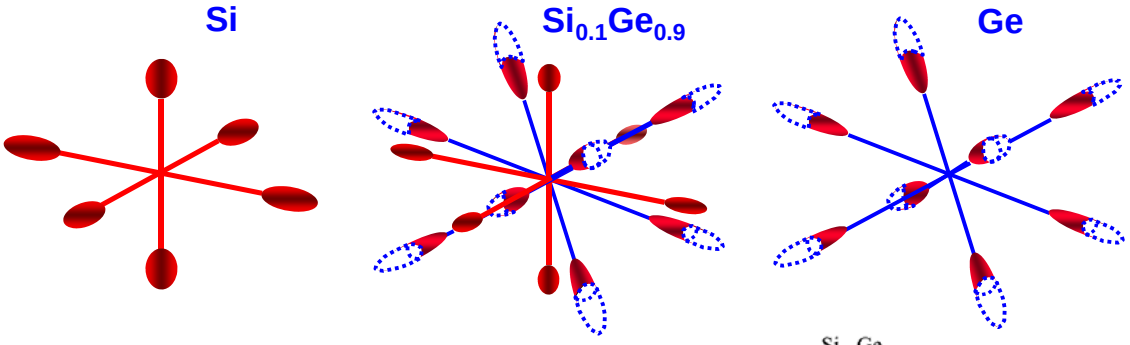


Figure 1. Si (left) and Ge (right) equi-energy valleys.

The conduction band minima at Δ in Si and *L* in Ge cross at $Si_{0.14}Ge_{0.86}$ changing both E_g and the bandstructure. For Ge<Ge~0.8x, SiGe has a bandstructure similar to Si. At $Si_{0.14}Ge_{0.86}$, the bandstructure is a amalgam of the two (see Figure 2).



Unit : m_o	Surface	Channel direction	1st ladder		
			m_x	m_y	m_z
Si	(100)	<001>	0.19	0.19	0.916
		<011>			
	(110)	<001>	0.19	0.553	0.315
		<110>	0.553	0.19	
Ge	(100)	<001>	0.153	0.153	0.12
		<011>	0.085	1.12	
			1.12	0.085	
	(110)	<001>	0.601	0.082	
		<110>	0.082	0.601	

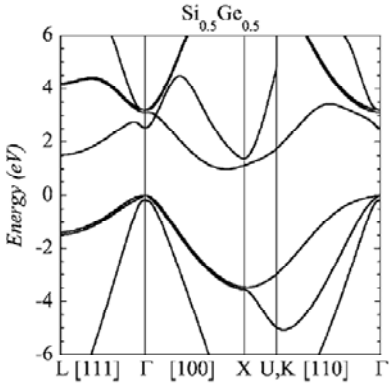


Figure 2. The conduction band minima at Δ in Si and *L* in Ge cross at $Si_{0.14}Ge_{0.86}$. Note the equi-energy diagram for the cross-over point (upper middle) and the band-diagram at $Si_{0.5}Ge_{0.5}$ (lower right). Richard (2), Oh (2A).

The conduction band responds to strain largely through energy band splitting (see Figure 8 and discussion later) but recently (3-5) it has been recognized that band-warping also occurs (see Figure 3 below).

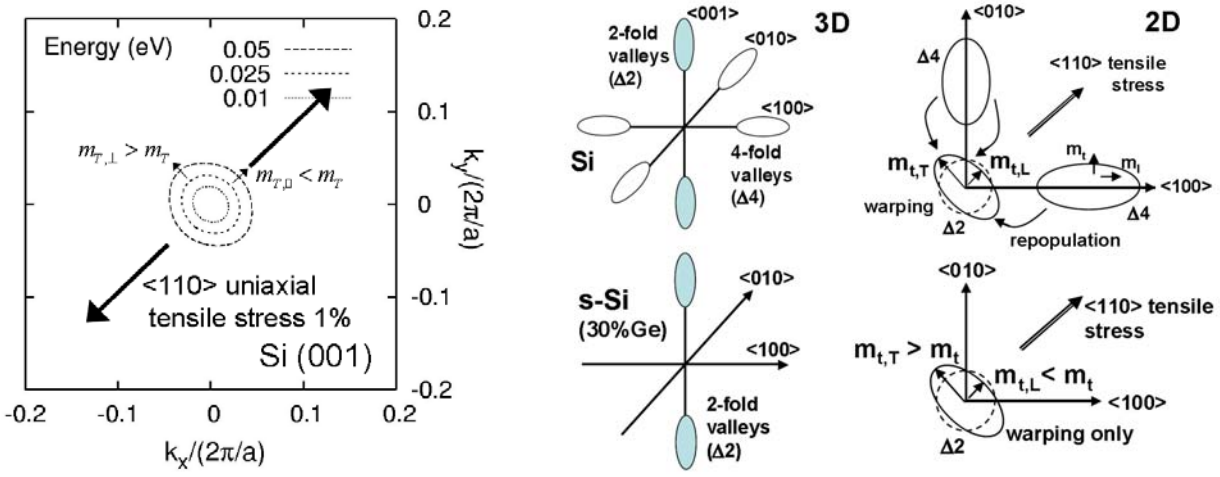
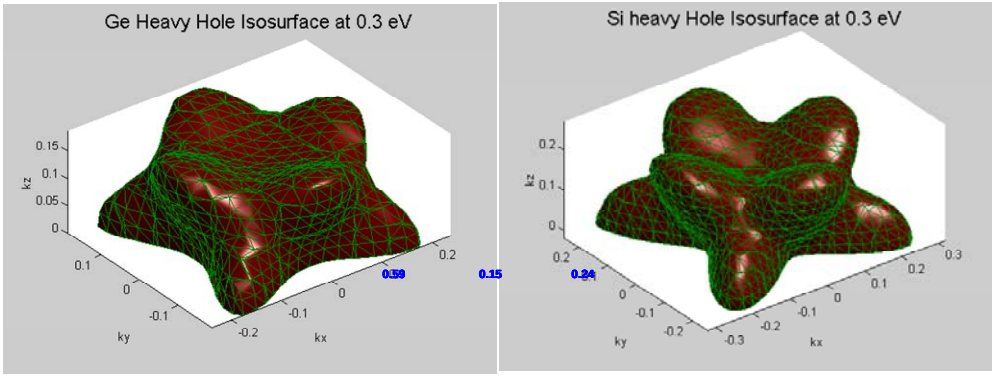


Figure 3. Band-warping in the conduction band of Si. Left: Uchida (3). Right: Weber (4).

Valence band:

Somewhat in contrast to the conduction band, the band structure of the valence band is very similar for both Si and Ge (see Figure 4). The band maxima and minima are at matched crystal orientations, and the overall shape is the same. However, the Ge band structure is less anisotropic than Si and the effective mass is lower. In addition, germanium responds to stress in a similar way as silicon, but possesses an improved stress response over Si at inversion (see Figure 5).



Band Masses at Gamma point (using kp parameters, in m_e):

	HH	LH	SO
Si	0.59	0.15	0.24
Ge	0.38	0.04	0.07

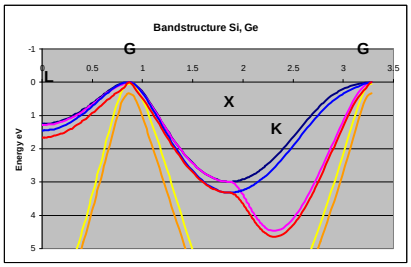


Figure 4. Ge and Si have similar valence band structures; note however, the significantly lower effective mass for Ge.

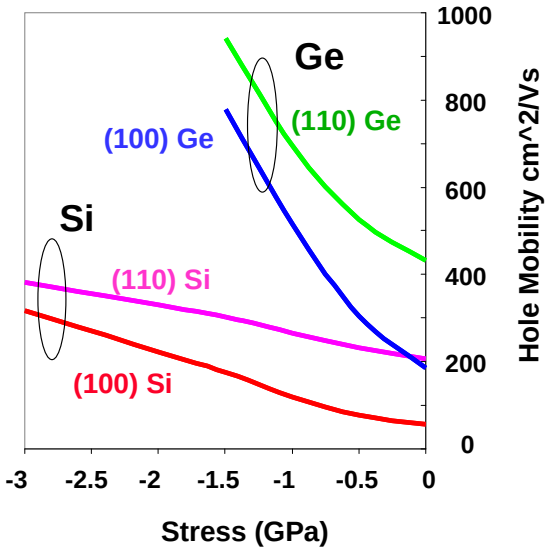


Figure 5. Low field long channel mobility of Si and Ge as a function of stress. Si valence band deformation potentials were calibrated to match mobility stress response data (data from Packan, 6) with a= 2.1 eV, b=-1.9 eV, and d=-2.7 eV. For Ge, values from Fischetti (7) a=2.0 eV, b=-2.16 eV, d=-6.06 eV were used.

Gemanium oxide:

Germanium oxide (Figure 6) exists in several morphologies (some of which are hydroscopic and volatile). Note that GeO_2 is soluble in water, but doesn't sublimate; while GeO(s) is insoluble in water and sublimates at 700°C. GeO_2 on Ge decomposes into solid GeO(s) as well as gas-phase GeO(g) at a temperature of ~400°C (GeO_2+Ge → 2GeO(s) or 2GeO(g) at ~400°C) (8).

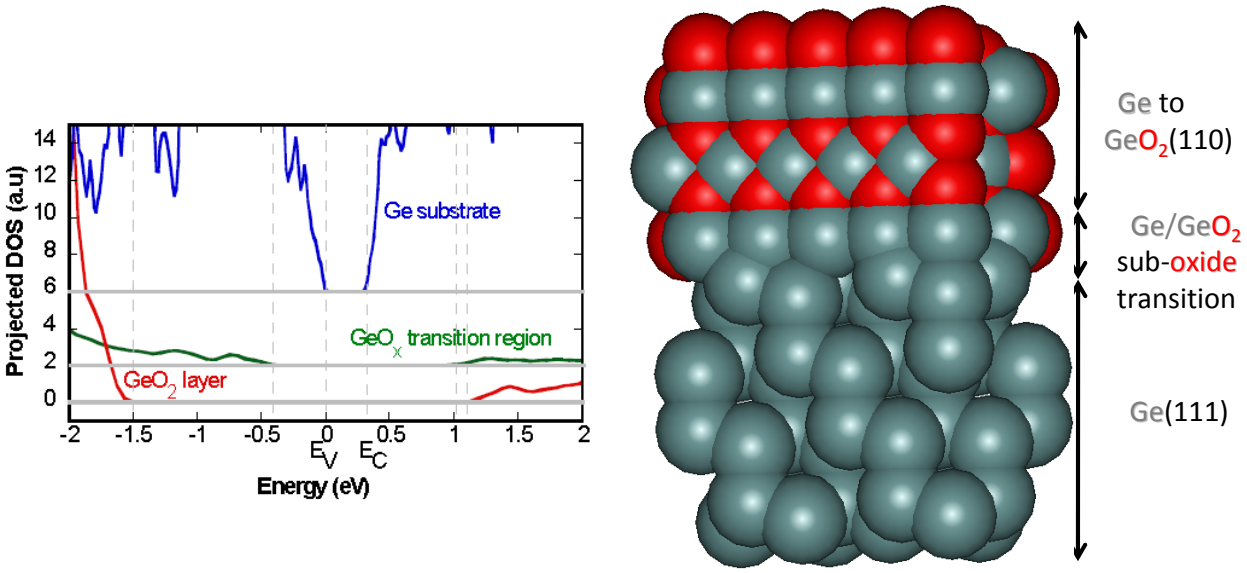


Figure 6. GeO_x on Ge. Left, Heynes (9). Right, from this work.

CMOS and SiGe: Past Successes

Strain has had tremendous impact in advancing the transistor scaling roadmap (Figure 7, refs. 10-37). The next section will review the history of MOSFET channel strain generated using Si/SiGe, both to place this development in the historical context, as well as to provide ideas for future strain enhancement.

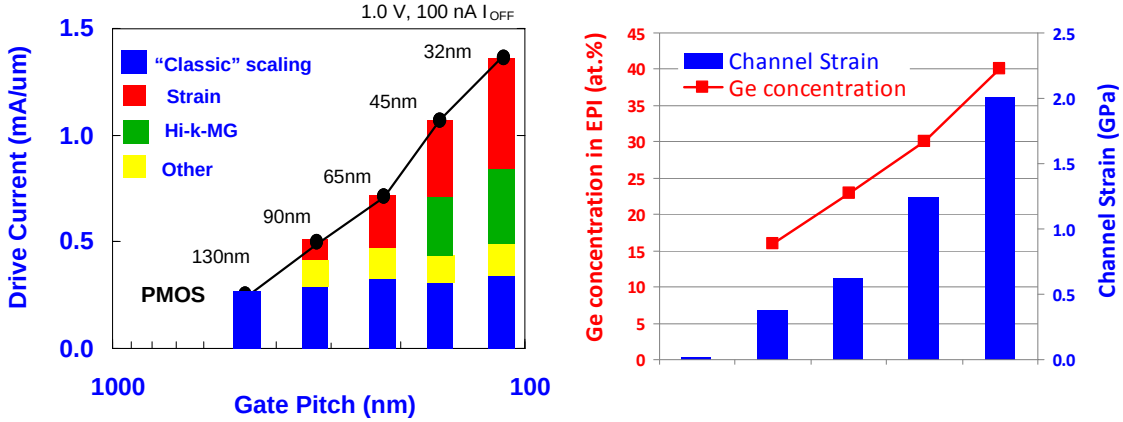
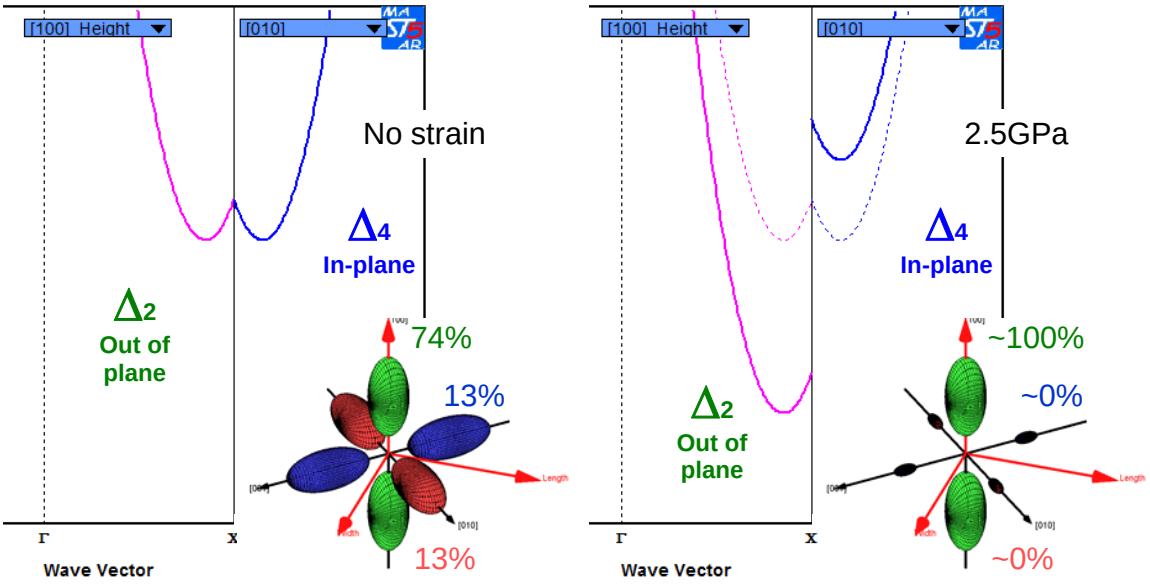


Figure 7a (left) overall importance of strain in CMOS scaling (10).
Figure 7b (right) PMOS strain improvement per generation from Ge scaling.

Substrate induced strain using epitaxial growth of lattice-mismatched Si/SiGe

Biaxial tensile strain is of particular interest for NMOS silicon channels. Strain can be introduced by epitaxial growth of lattice mismatched Si on SiGe. Because the Si lattice is smaller than the SiGe (or Ge) lattice, the Si layer will be stretched in two directions (biaxially). This biaxial stretching places the channel in biaxial tension and breaks the symmetry of the six-fold conduction band valleys. The out-of-plane valleys (lower transport mass) drop in energy, thus electrons move to populate these lower mass valleys. Furthermore, the energy separation between valleys is increased, reducing scattering between bands and valleys (see Figure 8).



Biaxial tension (confined)
(100) Surface: <110> channel

Biaxial tension (confined)
(100) Surface: <110> channel

Calculated using MASTAR (http://www.itrs.net/models.html)

Figure 8. Biaxial tensile strain in NMOS (11).

The seminal work in this area was done by Welser in 1992/4 (12,13) when he first quantified the strain enhancement for NMOS in strained Si on relaxed SiGe. This was followed by Rim in 2000-2 (14-16) with a series of comparative studies with both strained and unstrained Si surface channels. Hoyt in 2002 (17) expanded on the work of Welser and Rim by exploring the strain enhancement with vertical effective field and doping. Uchida in 2005 (3) added to the vertical field understanding by demonstrating experimentally that repopulation and reduction of scattering due to valley splitting with stress resulted in a reduction of biaxial stress at high fields. (In contrast, due to band warping of the conduction band, uniaxial stress gains are only weakly dependent on field.)

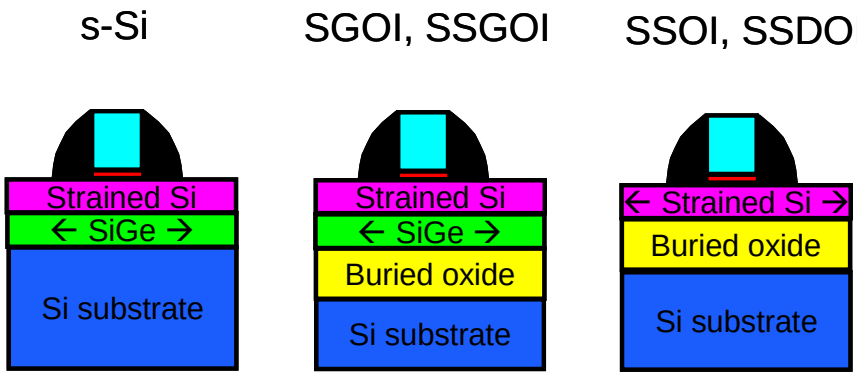
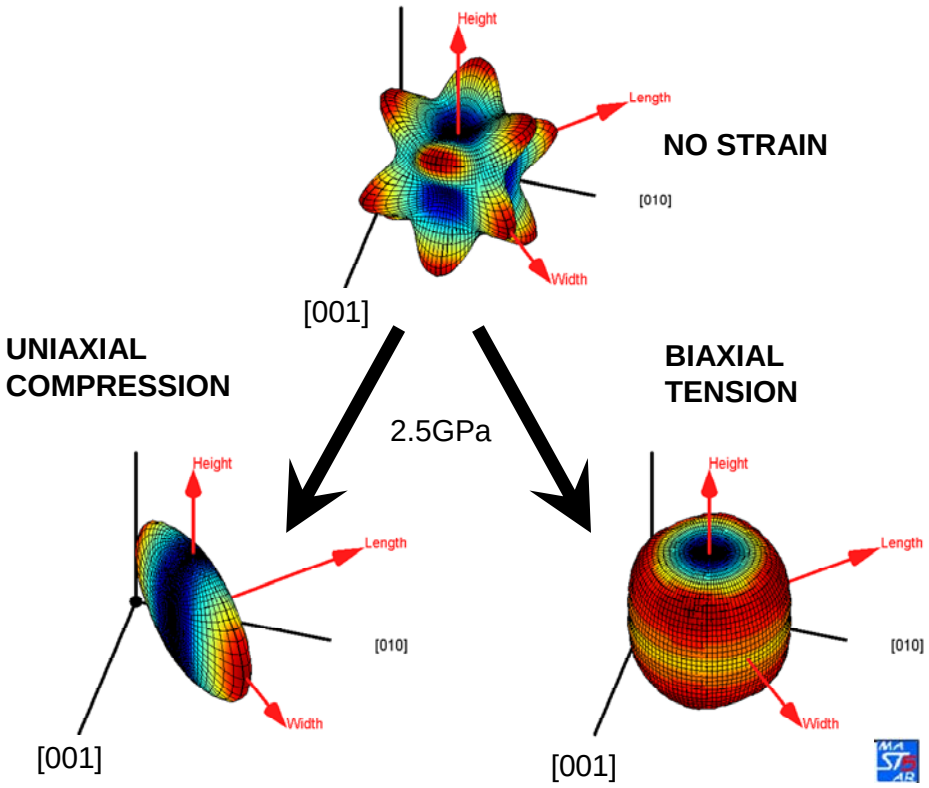


Figure 9. Three ways to fabricate strained silicon on relaxed SiGe on SOI (Chan, 18). Left – strained silicon on relaxed SiGe (s-Si). Middle – strained silicon on relaxed SiGe on SOI (variously called SSOI, SGOI or SSGOI). Right - strained silicon directly on insulator without a SiGe layer (typically fabricated with a wafer bonding and variously called SSOI, or SSDOI).

Strained Si on relaxed SiGe is just one of several process options for obtaining biaxial strain using Si/SiGe systems (see Figure 9). Two other common techniques include strained silicon on relaxed SiGe on SOI (variously called SSOI, SGOI or SSGOI) and strained silicon directly on insulator without a SiGe layer (typically fabricated with a wafer bonding and variously called SSOI, or SSDOI). Some of the earliest work was done by Mizuno in 1999 (19) through fabrication of a SiGe layer on a insulating layer using SIMOX and re-growth. Subsequently, Tezuaka in 2002 (20) produced strain-relaxed SiGe-on-insulator substrates using a Ge-condensation technique. Huang in 2001 (21) fabricated SGOI substrates with high Ge using wafer bonding. Lango in 2002 (22), produced strained silicon with no SiGe layer also through use of wafer bonding and Rim in 2003 (23) demonstrated a related technique through transfer of a tensile-strained Si layer to form a strained Si directly on insulator structure.

Uniaxial strain from embedded SiGe (e-SiGe)

Uniaxial compressive strain along <110> channel direction is of particular interest for PMOS silicon channels. Uniaxial strain can be produced by growing lattice mismatched SiGe inside Si source-drain regions. Because the SiGe lattice is larger than the Si lattice, and because the source-drain regions run parallel to the channel, the SiGe layer will push on the source-drain regions (and thus the channel) in only one direction. This single direction pushing places the channel in uniaxial compression and both warps and splits the valence band structure of silicon. The bandwarping produces improved effective transport mass for the heavy hole band (which is the ground state in the confined hole channel.) The uniaxial stress further increases the light-hole to heavy-hole band separation reducing the inter-band scattering. Uniaxial strain along <110> channel direction has a significant advantage over biaxial strain due to the presence of shear strain components which are responsible for strong anisotropic warping of the bands leading to repopulation of carriers to the bandstructure regions with the lighter transport mass. See Figure 10, Giles (24), Cea (25), and Mistry (26). In addition, since, bandwarping effects depend only weakly on confinement, uniaxial strain gains show a minimal dependence on effective field. (In contrast, tensile biaxial gains are significantly reduced at higher effective field.) See Thompson (30), Rim (27), Uchida (3).



Calculated using MASTAR (http://www.itrs.net/models.html)

Figure 10. Valence bandwarping of Si with strain
Left – uniaxial compression; Right – biaxial tension (11)

The seminal work on e-SiGe as a highly-manufacturable uniaxial PMOS strain solution was presented by Thompson in 2002 (28-30). Ghani expanded on this work in 2003 (31), and Chidambaram in 2004 (32). This elegant technique caught on quickly and by 2005 many researchers were exploring this, with representative examples including Lee with e-SiGe with SOI (33), Ohta illustrating the impact of e-SiGe profile engineering (34), and Zhang demonstrating e-SiGe on thin body SOI (35). As an additional enhancement, Wang in 2007 (36) and Auth in 2008 (37) demonstrated that a replacement gate flow enabled additional PMOS strain enhancement as a consequence of first straining the PMOS with e-SiGe and then removing the gate (Figure 11).

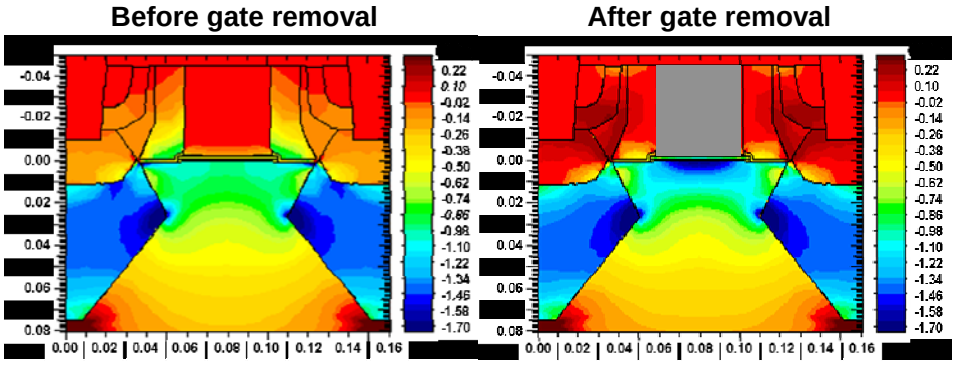


Figure 11. Removal of poly gate increases channel stress by 50% (37)

Measurement techniques for strain

X-ray diffraction (XRD) and Raman scattering are the most common techniques for assessing strain on large area (usually test structures) and nano-beam and convergent beam diffraction (NBD and CBED) are the most common techniques used for assessing strain within the channel itself.

XRD uses Bragg scattering at x-ray wavelengths to determine the configuration of atoms in a crystal (see Figure 12). In an X-ray diffraction measurement, the sample is mounted on a goniometer and rotated to produce a diffraction pattern. XRD can determine epilayer in-plane and out of plane strain components through analysis of symmetric and asymmetric diffraction patterns (<50ppm resolution). For SiGe samples of interest, XRD can determine the Ge content in buffer and graded layers, the strain of SiGe buffer and/or epilayer and (sometimes) determine dislocation type and density. However, XRD cannot measure small structures, has limited depth resolution and poor sensitivity to ultrathin films/surface layers.

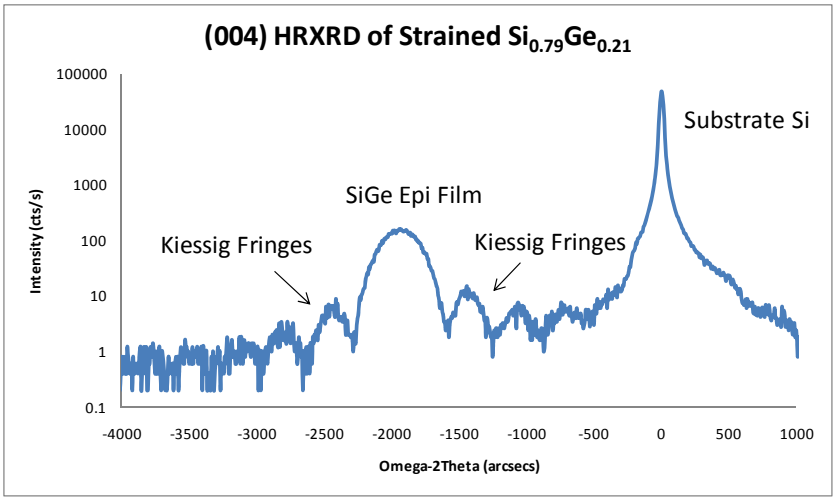


Fig 12. HRXRD (004) data of strained SiGe layer. Calculations from (004) and (115) data shows a fully strained layer with 21% Ge. Presence of Kiessig fringes indicates excellent interface quality and allows for calculation of epilayer thickness.

Raman scattering is the inelastic scattering of photons from vibration–induced phonon modes in a material. Raman scattering is a two–photon process ($h\omega_{laser}$ - $h\omega_{scattered}$ = $h\omega_{phonon}$) whose probability is dependent on the polarizability change in the bond during phonon motion. A laser source is typically used for Raman spectroscopy and the recorded spectrum shows the scattering intensity relative to the shift in frequency of the laser. In crystalline materials such as silicon and SiGe, the presence of stress causes a shift of phonon peak positions. The magnitude and direction of the shift can be correlated to the amount and sign (compressive/tensile) of the strain (see Figure 13). By accessing the Ge-Ge, Si-Ge and Si-Si phonon modes one can derive Ge content and strain independently for SiGe systems including Si epilayers. Inherently Raman is an indirect measure of the lattice constant(s) of the system and suffers from phonon broadening effects such as laser heating. As such, XRD offers better accuracy and precision, but Raman is much faster, has a significantly better spot size (~1 micron), and delivers improved surface sensitivity (dependent on laser wavelength).

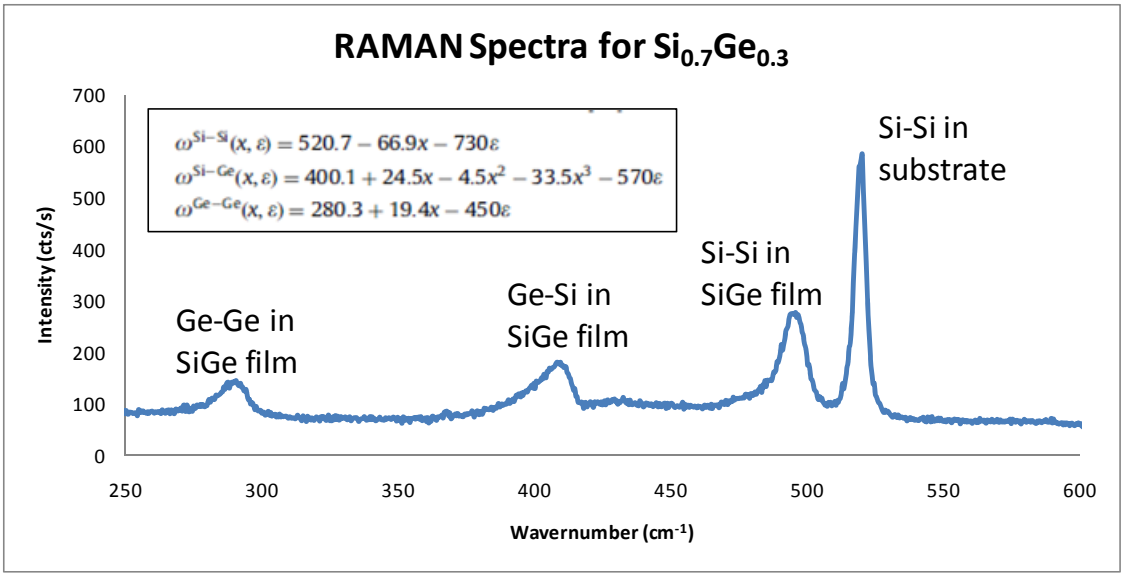


Figure 13. Raman spectra of a strained $Si_{0.70}Ge_{0.30}$ film on Si. Formula can be solved independently for Ge content (x) and strain (ε) (Pezzoli, 38)

Unfortunately, neither XRD nor Raman has sufficient spatial resolution to measure strain directly in a single transistor channel. In recent years, the higher resolution nano-beam and convergent beam diffraction (NBD and CBED) techniques have been used to directly measure channel strain. NBD uses a nearly parallel electron beam 15–25nm in diameter, which gives a traditional electron diffraction pattern. Strain can be determined from the separations of the diffraction spots that shift with strain and are inversely proportional to its magnitude. CBED uses a focused nanometer sized probe that gives rise to diffraction patterns with disks. For certain crystallographic directions, the central disk of a CBED pattern contains well–defined high–order Laue zone (HOLZ) lines that shift with strain. Strain can be determined from line shifts by fitting simulated CBED patterns to experimental ones. In both techniques, it is essential to have an unstrained area within the field of view to collect reference (zero strain) patterns so that experimental errors can be minimized. The CBED technique is inherently more sensitive for strain determination (0.05%) when compared to NBD (0.1%), because CBED is based on higher order diffraction reflections, which are more sensitive to changes in interplaner spacings. However, CBED suffers from the requirement to tilt samples for well–defined HOLZ patterns (Belyansky, 39, and Figure 14).

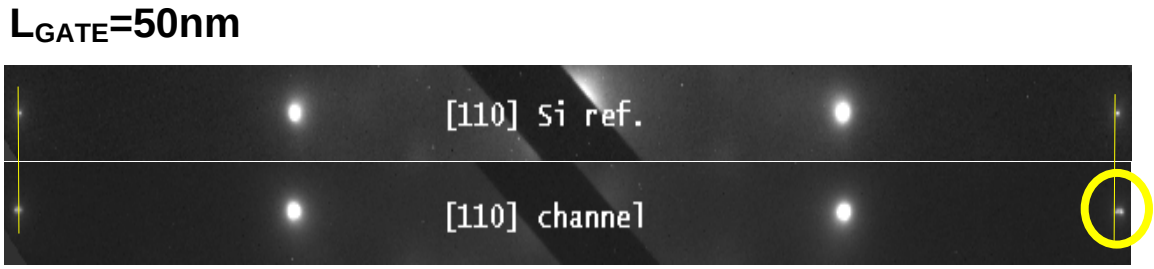


Figure 14. Measurement of stress using nano-beam diffraction (NBD) (26)

CMOS and SiGe: Past and Future challenges

While the use of strain as a performance enhancer is expected to continue as a key contributor to the CMOS scaling roadmap for some time, the most intriguing future use of Ge or SiGe in CMOS scaling is as a high mobility replacement for the Si channel (40-42, Figures 15-16). Recall that Ge was the primary transistor material from the invention of the transistor in 1947 until the 1960s, when MOS became technologically important. The two most critical reasons for switching from Ge to Si for early MOS technology remain the two most critical issues today; namely the poor quality of GeO_2 compared to SiO_2 and the smaller bandgap of Ge compared to Si. The critical changes between 1960 and 2010 leading to reconsideration of Ge channels are: 1. advent of manufacturable high-k technologies (6, 43-44), 2. decreasing voltages of modern products (45), and 3. development of highly quantum confined devices (UTB etc.) which increase the effective bandgap (46).

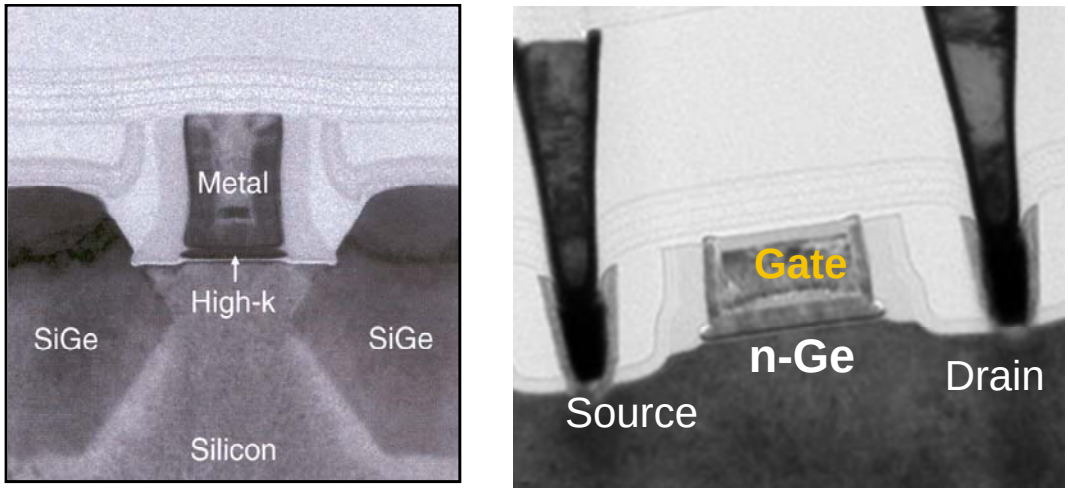


Figure 15. The advent of manufacturable high-k technologies is leading to the reconsideration of Ge channels. Left: 45nm high-k device (43). Right: Ge channel device.

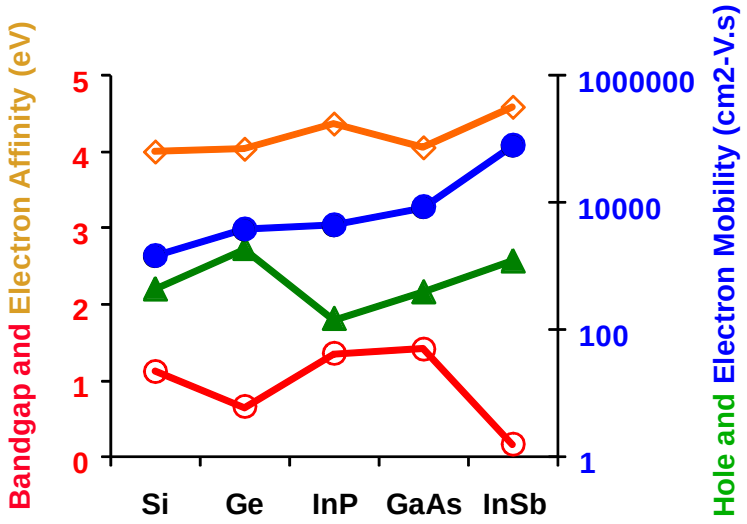


Figure 16. Key electronic parameters for major semiconductors.
Note the improved mobility for Ge vs Si, along with the degraded bandgap (47).

Competitive dielectric thicknesses without degrading mobility

The key challenge with Ge (and SiGe) is that both industry and academic data show rapid degradation in mobility with decreasing electrical oxide thickness (Figure 17). The primary model for this degradation is poor quality germanium oxide at the Ge/dielectric interface. Thus, the goal is to create a high quality interface between the dielectric and the SiGe. Note that this issue exists even if a high-k dielectric is used, because an interface layer between the Ge and the high-k is still formed. (In fact, use of a high-k dielectric may further complicate the issue by altering the chemistry of the GeO_2 film).

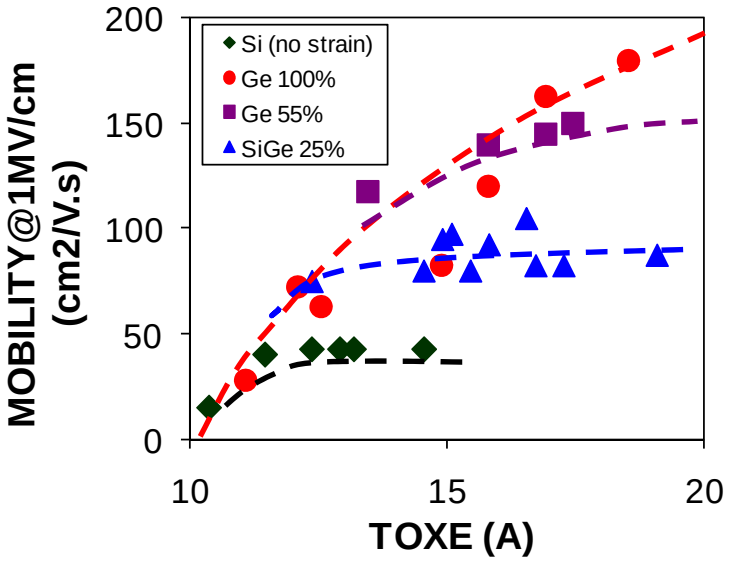


Figure 17. Industry and academic data show rapid degradation in mobility with decreasing electrical oxide thickness.

There are two major strategies being researched for resolving this issue, one is the use of an ultra-thin Si cap and the second is thermally-grown GeO_2.

The use of a thin Si-cap (or Si-passivation layer) is the most mature of the technologies under investigation. In the seminal 2006 work by Zimmerman (48) a Si surface passivation and HfO_2 dielectric was used to obtain low field hole mobilities of up to 358 $cm^2/V{\cdot}sec$ for PMOS devices with L_g down to 125nm. Ge pMOS drain current was 790 uA/um at $Vg = Vd = -1.5V$ for an L_g of 190nm. Subsequent work in 2008 by Mitard (49) showed low field hole mobilities ~300 $cm^2/V{\cdot}sec$ for PMOS devices with L_g ~100nm and *Ion/Ioff* at 478µA/µm and 37nA/µm at Vdd=-1V for devices with L_g at 65nm. Later work in 2009 by Hellings (50) reported PMOS devices with *Ion/Ioff*: 622µA/µm and 900nA/µm at *Vdd*=-1.2V with L_g at 70nm. Additional work by Mitard in 2009 (51) focused on EOT reduction in PMOS devices, and showed EOT scaling down to 0.85nm with leakage below $0.2A/cm^2$. Batail in 2008 (52) took a different approach (although still using a Si passivation layer) by comparing Ge-condensation process with epitaxy of a pure ultra-thin 2.3nm thick Ge layer directly on Si. Batail reported PMOS devices with low field long channel hole mobilities ~140 $cm^2/V{\cdot}sec$ and *Ion/Ioff* at 600µA/µm and 1000 nA/µm at *Vdd*=-1.1V with L_g at 75nm.

Historically, GeO_2 was considered a poor passivation material and most effort focused on Si-cap (see above). However recent studies have re-awakened interest in GeO_2, with particular emphasis on enabling NMOS. As an example, a detailed analysis by Kita in 2009 (53) works through the details of GeO desorption and thermodynamic control of the GeO_2/Ge system through use of temperature and high pressure oxidation (HPO). Kita proposes optical absorption in the subgap region of GeO_2 as a monitor for observing GeO desorption. With these techniques, they showed mid-gap D_{it} reduction down to the order of 10^{10} $cm^{-2}eV^{-1}$. Using related concepts in pressure and temperature control, Lee in 2009 (54) demonstrated NMOS long channel low field mobility of 1100 $cm^2/V{\cdot}sec$ on Ge (111) and 800 $cm^2/V{\cdot}sec$ on Ge (100) using high-pressure oxidation (HPO) and low temperature oxygen annealing (LOA). Kuzum in 2009 (55,56) took a related approach, using ozone-oxidation, low activation anneals, and a GeO_2/ Al_2O_3 gate stack. Low field long channel hole mobilities ~300 $cm^2/V{\cdot}sec$ with D_{it} at $4{\cdot}10^{11}$ $cm^{-2}eV^{-1}$ were reported for PMOS and ~500 $cm^2/V{\cdot}sec$ with D_{it} at $4{\cdot}10^{11}$ $cm^{-2}eV^{-1}$ for NMOS. Bellenger in 2010 (57) reports on a similar strategy with GeO_2/Al_2O_3 gate stacks at 3.7-nm EOT with mobility reaching 235 $cm^2/V{\cdot}sec$ for electrons and 265 $cm^2/V{\cdot}sec$ for holes at a D_{it} of $2{\cdot}10^{11}$ for valence band-edge (PMOS) and $2{\cdot}10^{12}$ $cm^{-2}eV^{-1}$ for conduction band edge (NMOS). Another interesting strategy in this space was reported by Xie in 2008 (58) with the twist of using post-gate treatment with fluorine. Xie observed that F incorporation improved the frequency dispersion and *C-V* stretch-out as well as reducing the interface trap density. Xie reported low field long channel hole mobility ~400 $cm^2/V{\cdot}sec$ with a D_{it} of $2{\cdot}10^{12}$ $cm^{-2}eV^{-1}$.

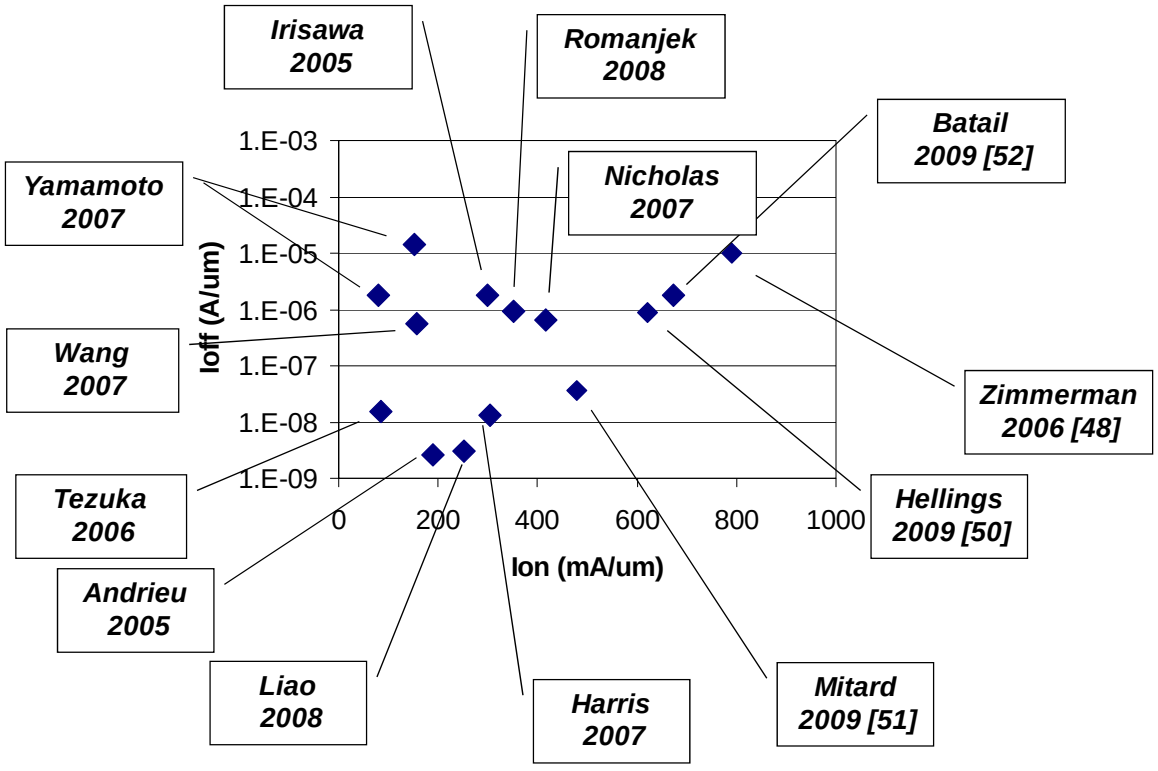


Figure 18. Summary of reported literature results (52 updated with 48,50,51).

Challenges of narrow bandgap

Another key challenge with Ge (and SiGe) is the significant reduction in energy bandgap with increasing Ge percentage (see Figure 19, references 7, 60).

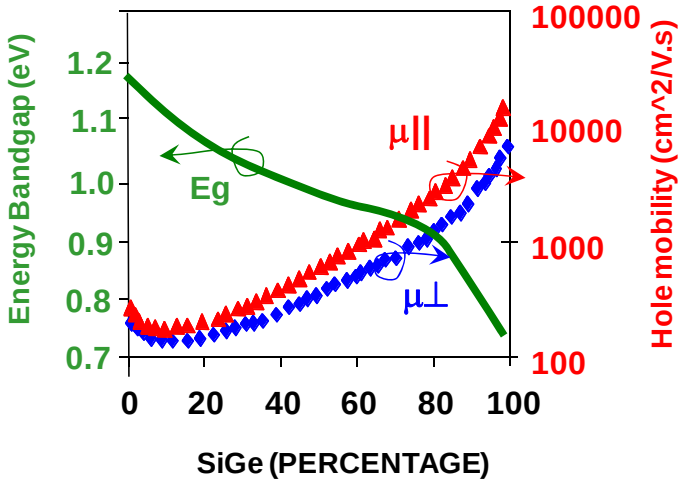


Figure 19. Relationship between mobility and bandgap for SiGe compounds (7,60).

A major concern for Ge is the low bandgap, which results in high off-state leakage (*Ioff*) due to band-to-band tunneling (Figures 20-21). Straining germanium (for further mobility improvement) has the unfortunate side effect of further degrading the bandgap.

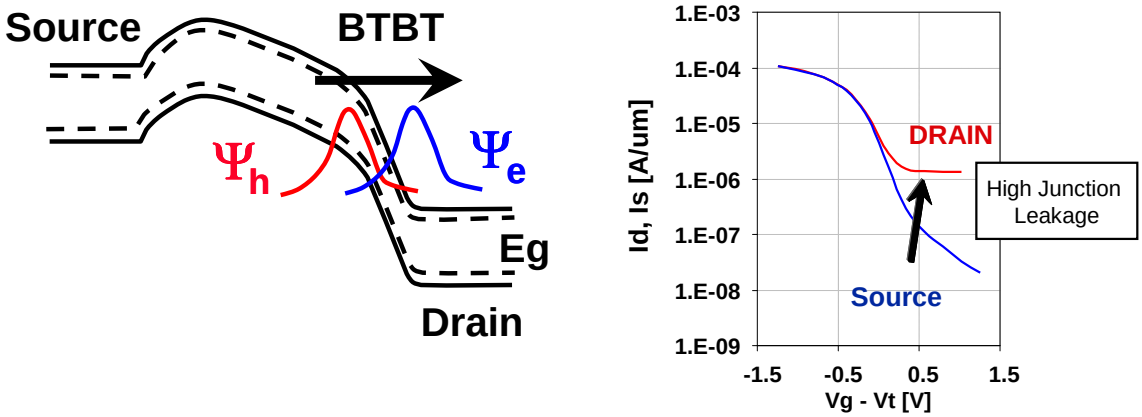


Figure 20. Band to band tunneling effects can cause off-state leakage issues (59-60).

There are basically two solutions to this problem. The first is to selectively apply Ge (SiGe) devices to low-voltage products where $V_{nom} < Eg$. This may represent an excellent solution for low-power and mobility applications (where Ge/SiGe performance delivers better *Ion* than strained-Si for a given *Ioff*), but may pose an issue for products (mainstream desktops, laptops and servers) which operate at voltages where strained silicon can deliver higher *Ion* for a given *Ioff*. The second strategy is to fabricate these devices in a quantum confined system (for example, an ultra-thin body or nanowire, Figure 21) where the quantum confinement generates strong quantization of the energy levels and a larger effect bandgap. In these systems, the wavefunction decays faster in the forbidden gap and reduces the overlap between the quantized hole and electron wavefunctions, thus leading to a reduced BTBT rate.

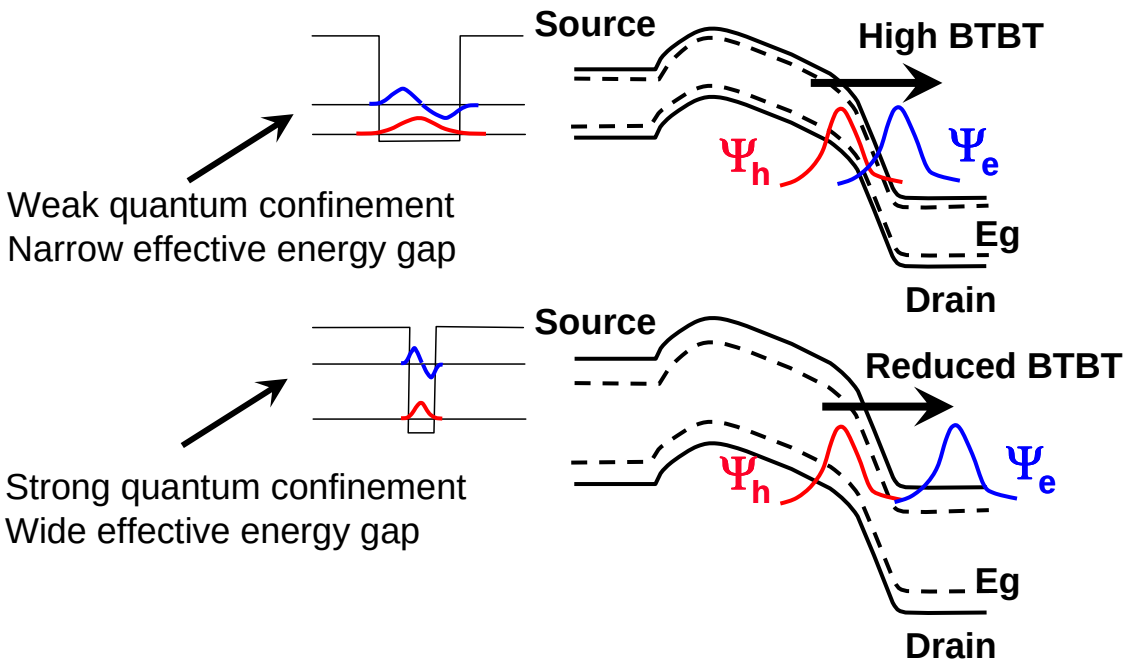


Figure 21. In quantum confined systems the overlap between the quantized hole and electron wavefunctions is reduced leading to reduced BTBT (59, 60).

Conclusions

SiGe has played a very significant role in driving the modern CMOS scaling roadmap through its use as a PMOS stressor. SiGe (and Ge) may play a significant future role in CMOS scaling as a high mobility replacement for the Si channel. Challenges such as poor quality germanium oxide and the small Ge bandgap must be resolved for SiGe (and Ge) to be successful as a Si channel replacement.

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