The Ultimate CMOS Device and Beyond

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Abstract

For the past 40 years, relentless focus on Moore's Law transistor scaling has delivered ever-improving CMOS transistor density. This paper discusses architectural and materials options which will contribute to the ultimate CMOS device. In addition, the paper reviews device options beyond the ultimate CMOS device.

Introduction

Manufacturing implementation of strain (90nm, [1]), high-k / metal gate (45nm, [2]), and non-planar TriGate devices (22nm, [3]) continues to support and energize the Moore's Law performance roadmap (Fig. 1). *CV/I* and CV^2 have steadily improved over time, even in the presence of dramatic shifts in transistor targeting driven by consumer demand for lower power mobile products (Fig. 2). An important question for the semiconductor industry is, "What options lie ahead to drive Moore's Law forward?"

To address this question, this paper will discuss architectures for improved short channel control (TriGate, nanowire), advanced channel materials (Ge, III-V, carbon nanotube), techniques for improving R_{ext} (including metal source/drain devices), ultra-steep sub-threshold devices (tunnel FETs, relays), and non-charge-based (spin) technologies.

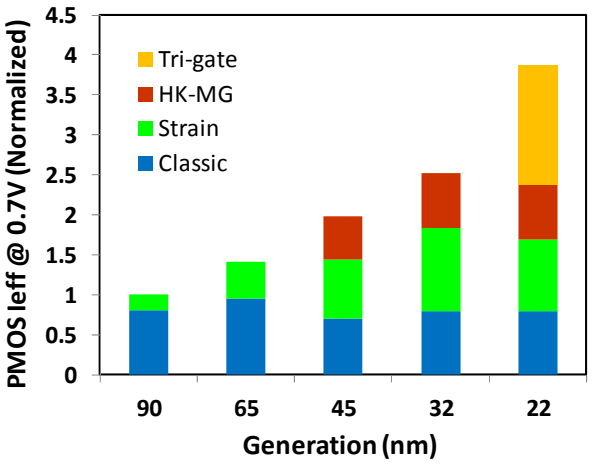

Fig. 1. Manufacturing implementation of strain, high-k / metal gate, and non-planar TriGate devices continues to support and energize the Moore's Law performance roadmap.

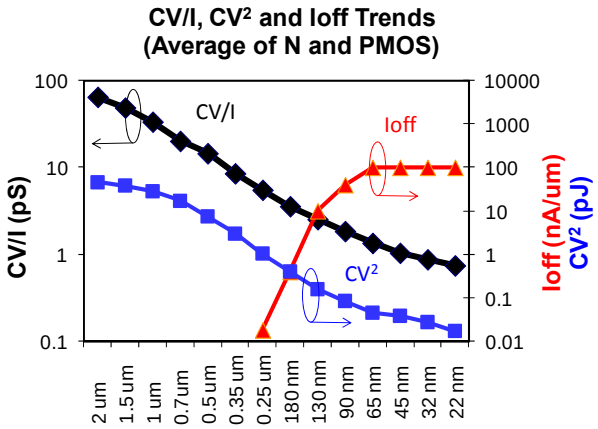

Fig. 2. *CV/I* and CV^2 have steadily improved over time, even in the presence of dramatic shifts in transistor targeting.

Architectures for Improved Short Channel Control

A variety of advanced architectures for improved electrostatic control have been proposed (Fig. 3, [4]).

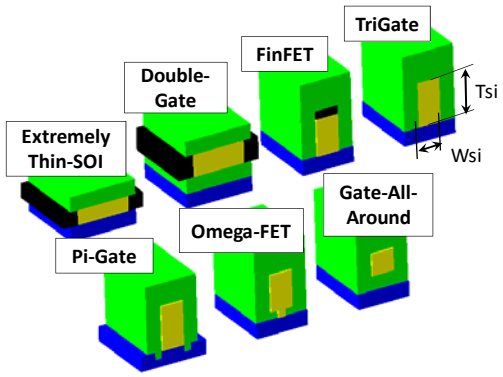

Fig. 3. Advanced architectures for improved electrostatic control [4]

The introduction of the TriGate device in the 22nm node [3] marked the end of the planar device era. The TriGate has a gate surrounding the channel on three sides (Fig. 4). The superior electrostatic control of the 22nm TriGate architecture has been shown to deliver >35% performance improvement over the 32nm generation at 0.7V at 40nA/um I_{off} (Fig. 5, [3]). However, implementation of non-planar architectures into manufacturing is not trivial. For example, successfully integrating e-SiGe PMOS with TriGate required innovative new manufacturing techniques (Fig. 6, [3]).

The most extreme of the advanced architectures is the gate-all-around (GAA) architecture (Fig. 7). In the GAA architecture, the gate entirely surrounds the channel. This architecture has the benefit of superb short channel control (Fig. 8), but at the potential cost of decreased mobility due to increased scattering at smaller dimensions (Fig. 9, [5-6]).

Advanced materials

A number of non-silicon channel materials are under consideration for advanced CMOS devices. These materials include the more traditional semiconductor materials such as SiGe, Ge and GeSn (PMOS) as well as various III-V materials combinations including InGaAs and GaAs (NMOS). In addition, carbon based materials such as carbon-nanotubes (CNT) and graphene are under consideration.

The benefit of the more traditional semiconductor materials (SiGe, Ge, GeSn, InGaAs, GaAs etc.) is the low effective mass (Fig. 10, [4]). Many of these materials also display effective mass or scattering improvements under stress, further enhancing their value for device fabrication (Fig. 11, [7]). However, a critical challenge in all these materials is fabricating high quality gate dielectrics on the channel (Fig. 12).

The benefit of the carbon-based materials (for example, carbon nanotube devices, Fig. 13) is reduction or elimination of scattering. Some of these carbon-based systems also offer improved effective mass. A characteristic of these materials is degraded I_{off} due to small/non-existent bandgaps (Fig. 14, [8]). A key challenge in both carbon nanotube (CNT) devices and graphene, is that the highest mobility materials also have the lowest bandgaps and thus the poorest I_{off} (Fig 15).

Parasitic R_{ext}

Parasitic resistance continues to be a significant challenge in modern devices. A key component of parasitic resistance is the resistance at the Schottky contact to the source/drain (S/D) region. A variety of approaches are under consideration to reduce the Schottky Barrier Height (SBH) at the S/D interface. These approaches include more traditional approaches (implant and alloy techniques) as well as more exotic approaches (charge and dipoles) (ref. [4] and references therein).

The most extreme of the R_{ext} techniques is to replace the semiconductor S/D regions with metal (Fig. 16). Such devices have the benefit of performance improvement resulting from R_{ext} reduction (Fig. 17). The challenge of metal S/D devices is the sensitivity of the performance to SBH as well as the lack of experimentally achieved SBHs in the right range (Fig. 18). Additionally ambipolar conduction in these devices can limit I_{on}/I_{off} ratios (Fig. 16).

Ultra-steep Sub-threshold Slope

Another path to achieving performance enhancement is by circumventing the 60mV/decade subthreshold limit of energy barrier devices. As one example, tunnel FETs (TFETs) operate by tunneling through the S/D barrier (Fig. 19, [9]). TFETs offer the benefit (Fig. 20, [9]) of improved subthreshold slope but face the challenge of requiring offset bandedges only achieved in exotic heterostructures (Fig. 21).

A more exotic approach to subthreshold improvement is moving to mechanical devices, such as nanorelay devices (Fig. 22). Such devices have the potential for improved switching energy (Fig. 23) but face the challenge of achieving aggressive dimensions (dimensions on the order of the size of the contact asperity) without adhesion issues (Fig. 24).

Spin

In recent years, interest has increased in non-charge-based device technologies. An example of this is the spin-torque device, where the orientation of the spin of the electron is used to carry information (Fig. 25, [10]). Area efficient majority logic can be created where the signal is passed by spin transfer, not charge transfer (Fig. 26, [11]). Such spin devices have the benefits of smaller area (due to the ability to be stacked and majority logic), less power per gate, and non-volatility, but face the challenges of being slower (limited by slow magnet precession dynamics), with less throughput per unit area (Fig. 27, [11]).

Conclusion

The semiconductor device roadmap remains strong, both with near term options for achieving the ultimate CMOS device and longer term options for beyond CMOS architectures.

References:

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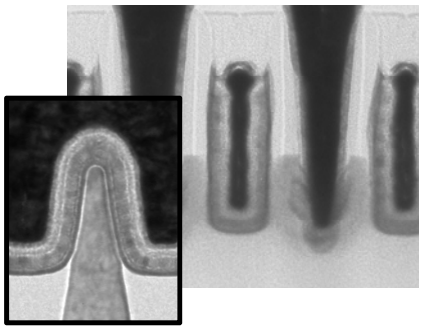

Fig. 4. The TriGate architecture is a non-planar architecture with the gate surrounding the channel on three sides [3].

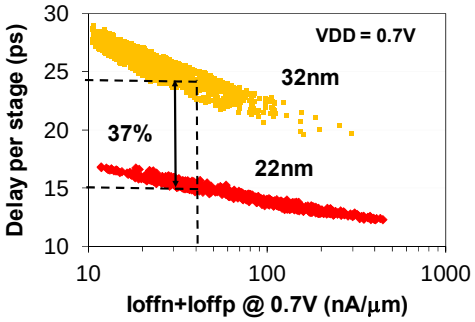

Fig. 5. The 22nm TriGate architecture delivers performance improvements over 32nm of 37% at 0.7V at 40nA/μm I_{off} [3].

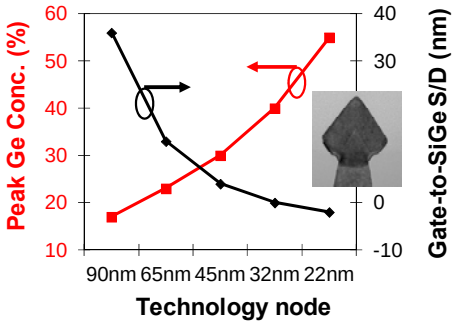

Fig. 6. Successfully integrating e-SiGe PMOS with TriGate required innovative new manufacturing techniques [3].

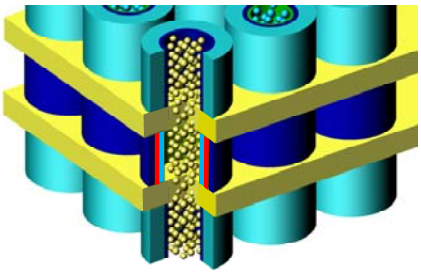

Fig. 7. The most extreme of the advanced architectures is the gate-all-around (GAA) architecture [4].

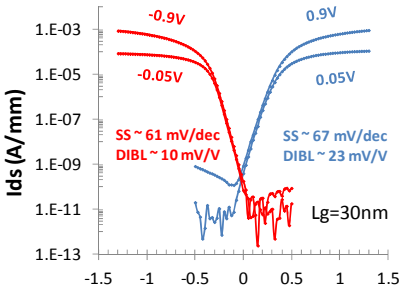

Fig. 8. GAA devices have the benefit of superb short channel control.

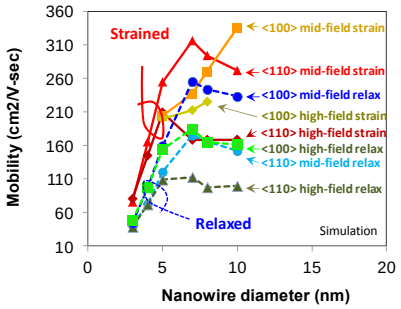

Fig. 9. GAA devices face the challenge of mobility degradation at small diameter due to scattering effects [5, 6].

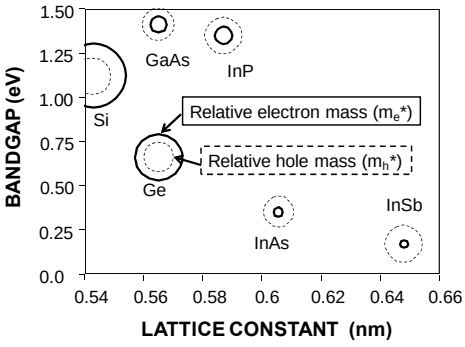

Fig. 10. The benefit of the Ge and III-V advanced materials is reduced effective mass [4].

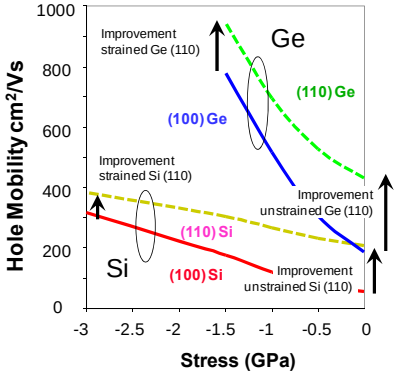

Fig. 11. Many advanced materials (such as Ge, illustrated here) display mobility improvements under stress [7].

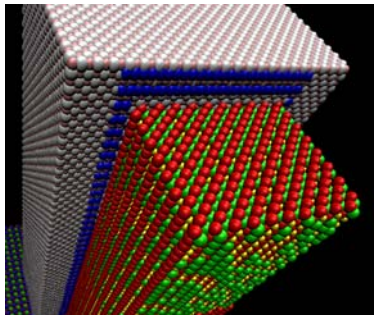

Fig. 12. Advanced materials face the challenge of fabricating high quality gate dielectrics on the channel.

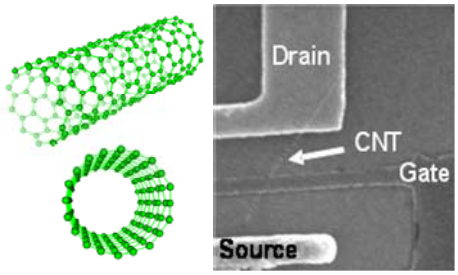

Fig. 13. The benefit of CNT devices is the reduction or elimination of scattering [8].

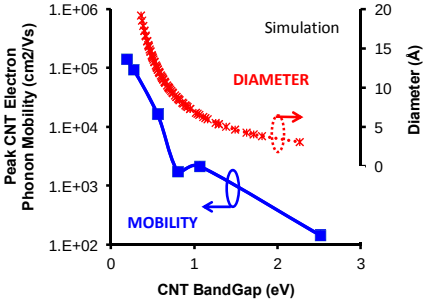

Fig. 14. CNT devices have the potential for high mobility, where high mobility is correlated to reduced bandgap [8].

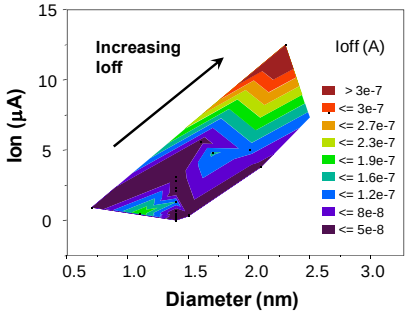

Fig. 15. CNT devices face the challenge of degraded I_{off} due to the correlation between lower bandgap, larger diameter, and higher mobility.

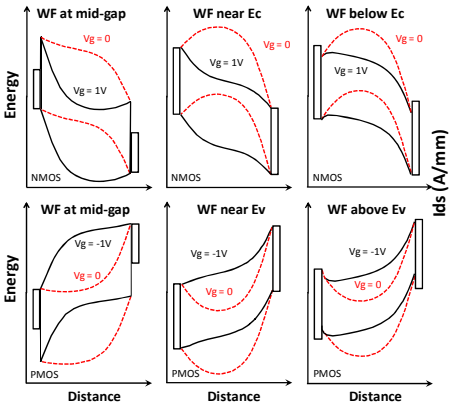

Fig. 16. The energy gap location of metal S/D devices as a function of V_g and the SBH.

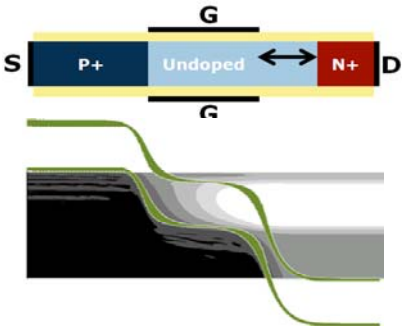

Fig. 19. Tunnel FETs (TFETs) operate by tunneling through the source/drain barrier [9].

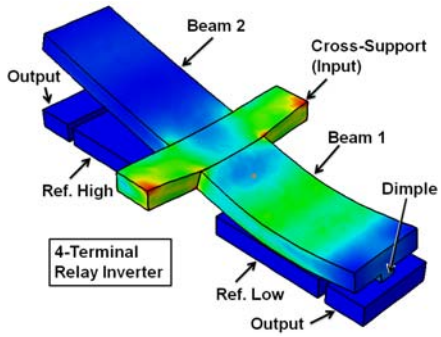

Fig. 22. Nanorelays offer an alternative to conventional electronic switches.

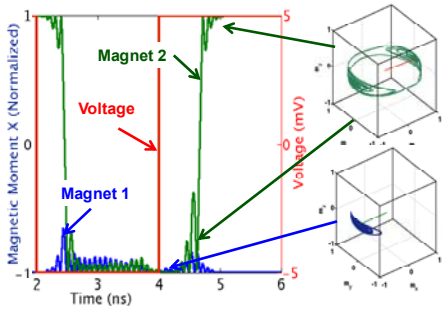

Fig. 25. Spin-torque devices use the orientation of the spin of the electron to carry information [10].

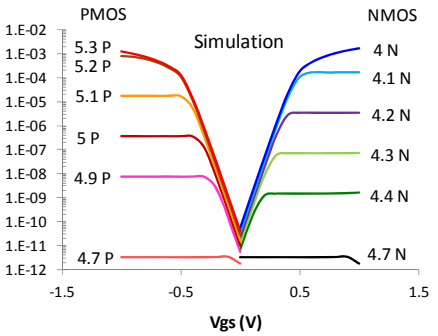

Fig. 17. Excellent I_D - V_G performance is possible in metal S/D devices with appropriate choice of SBH.

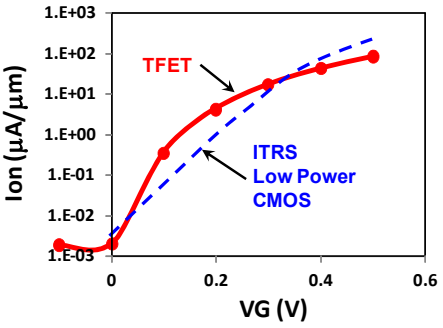

Fig. 20. TFETs offer the benefit of improved subthreshold slope [9].

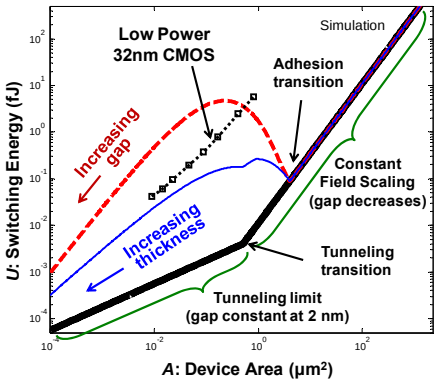

Fig. 23. Nanorelays have the potential for improved switching energy.

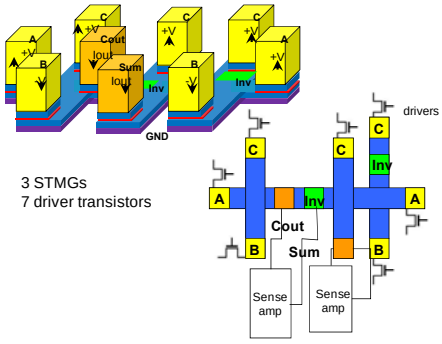

Fig. 26. An area-efficient spin torque majority gate adder circuit where the signal is passed by spin not charge [11].

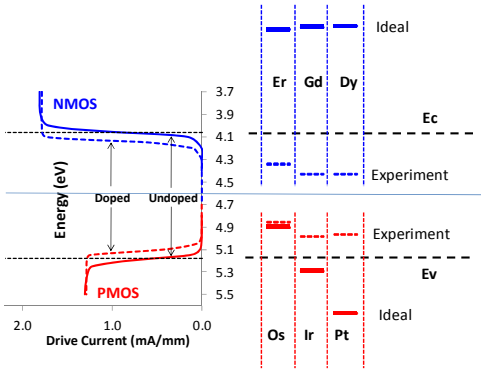

Fig. 18. Metal S/D devices face the challenge of experimental SBHs not sufficiently close to the bandedges.

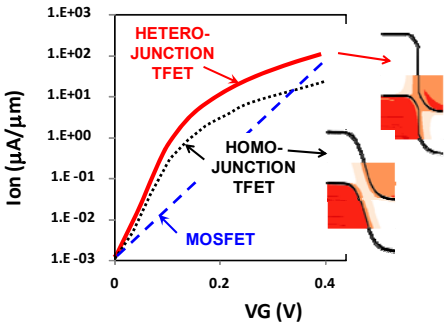

Fig. 21. TFETs face the challenge of requiring offset bandedges only achieved in exotic heterostructures.

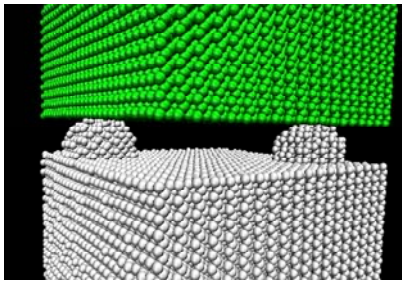

Fig. 24. Nanorelays face the challenge of achieving aggressive dimensions (on the order of the size of the contact asperity) without adhesion issues.

PARAMETER	CMOS	STMG	MTJ+CMOS
Area/gate (um²)	5.0	1.3	4.9
Switching time (pS)	16	2826	1.25
Power/gate active (μW)	70.6	45.6	163.0
Power/gate standby (μW)	0.81	0	0
Throughput/area Mops/nS/cm²	79.4	13.4	10.2
Non-volatile	No	Yes	Yes

Fig. 27. Spin-torque devices face the challenges of slower speed and less throughput per unit area [11].