Considerations for Ultimate CMOS Scaling

Kelin J. Kuhn, *Fellow, IEEE*

***Abstract*—This review paper explores considerations for ultimate CMOS transistor scaling. Transistor architectures such as extremely thin silicon-on-insulator and FinFET (and related architectures such as TriGate, Omega-FET, Pi-Gate), as well as nanowire device architectures, are compared and contrasted. Key technology challenges (such as advanced gate stacks, mobility, resistance, and capacitance) shared by all of the architectures will be discussed in relation to recent research results.**

***Index Terms*—Complementary metal-oxide semiconductor (CMOS), FinFET, mobility, nanowire, silicon on insulator (SOI), strain.**

I. Introduction

FOR THE past 40 years, relentless focus on Moore's Law transistor scaling has provided ever-increasing transistor performance and density [1]. As we look forward to the 7-nm node and beyond, we need to address both the familiar challenges of historical scaling and the new challenges associated with length scales on the order of atomic dimensions. In these advanced devices, the traditional issues of channel mobility, short-channel control, and parasitic resistance and capacitance are still critically important. However, in addition to these traditional issues, there are new issues of atomic spacing limiting critical dimensions, interface and support layers dominating the physical structures, and quantum confinement and scattering effects.

Consider, as an example, the illustration of an ultimate CMOS device as shown in Fig. 1. This is a device with a nanowire channel, a gate-all-around (GAA) architecture, a high-k gate dielectric, and a conductive gate electrode stack. The minimum channel dimensions will be determined by quantum confinement effects and scattering at atomic dimensions. The nanowire architecture is determined by electrostatic requirements to achieve the best possible short-channel control. Each of the various gate layers (interface layer (IL), high-k layer, threshold voltage (V_T) control layer, primary workfunction layer, conduction layer, and so on) is limited by material properties at atomic dimensions. This paper will discuss, at some level of detail, the progress to this ultimate device in each of the areas of parasitic resistance and capacitance, electrostatic confinement, and channel mobility.

II. Parasitics

From the transistor perspective, a key aspect of Moore's Law is achieving the desired $0.7\times$ dimensional scale factor in contacted gate pitch each generation (see Fig. 2). Scaling the contacted gate pitch can be accomplished by scaling the source/drain (S/D) regions, the spacer and overlap regions, or the channel length itself. However, there are trade-offs in determining the exact scale factors of each region. For example, a wider spacer will reduce parasitic capacitance (see Section II-B) but at the cost of a smaller S/D region and increased parasitic S/D resistance (see Section II-A). A shorter channel enabled by better electrostatics (see Section III-A and B) may enable a larger S/D region and reduced parasitic S/D resistance but at the cost of poorer gate fill and increased parasitic gate resistance (Section II-A). In practice, determining the exact scaling factors for each region requires detailed iterative evaluation including both device and circuit analysis.

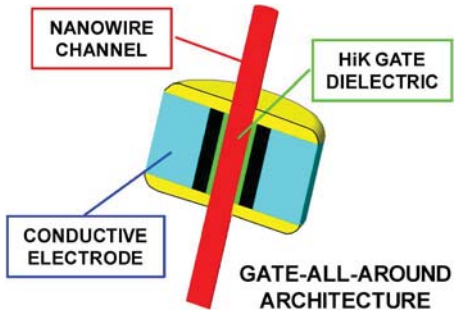

Fig. 1. Basic components of the ultimate CMOS device.

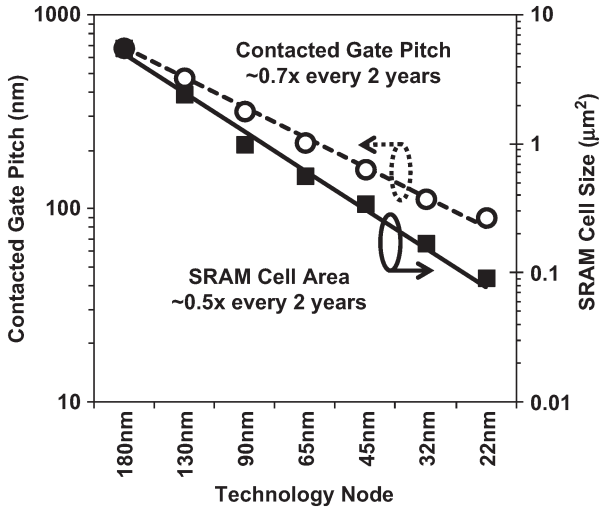

Fig. 2. Key aspect of Moore's Law is achieving the desired $0.7\times$ dimensional scale factor in contacted gate pitch and $0.5\times$ dimensional scale factor in SRAM cell area each generation [2].

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The author is with Intel Corporation, Hillsboro, OR 97124 USA.

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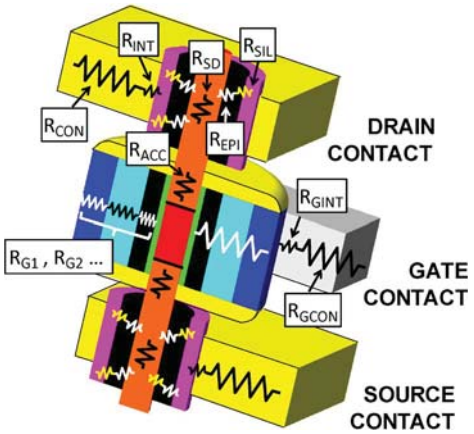

Fig. 3. Major resistance elements in the ultimate CMOS device.

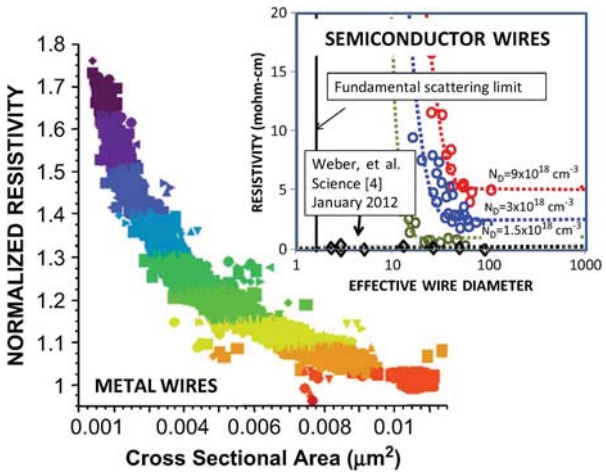

Fig. 4. (Main figure) Increased resistivity in metal wires with decreasing area due to scattering processes. (Inset) Increased resistivity of semiconductors with decreasing diameter and improvement with surface layer control [4].

A. Resistance and Next-Generation Transistors

Device parasitic resistance impacts circuit performance by reducing drive current and thus increasing delay. The major resistance components of the ultimate CMOS device are shown in Fig. 3. Overall, the device consists of a central gate region separated from the source and drain regions by spacers. The gate region includes a gate contact landing on a stack of gate metal layers (with both outer conduction and inner gate workfunction layers). The S/D regions at each end of the device include an S/D contact, a silicide (or equivalent) layer, and an epi (or equivalent) layer. Starting in the center of the device (and excluding the channel), there is a resistance associated with the S/D extension $(R_{\rm ACC})$, the S/D region itself $(R_{\rm SD})$, the raised S/D region and its interface $(R_{\rm EPI})$, the silicide region and its interface $(R_{\rm SIL})$, any interface resistance to the S/D contact metal $(R_{\rm INT})$, and the metal itself $(R_{\rm CON})$. For the gate resistances, there are resistances associated with the various gate layers $(R_{G1}, R_{G2}, R_{G3}\ldots)$, any interface resistance to the gate contact metal $(R_{\rm GINT})$, and the metal itself $(R_{\rm GCON})$.

The gate and S/D regions of the ultimate CMOS device have a number of features in common. Both require thin conductive layers to be deposited in a small space. In the case of the gate, the key requirements are conductivity and work-function tuning. In the case of the S/D regions, the key requirements are conductivity and minimizing Schottky barrier height. Perhaps equally important, both the gate and S/D regions incorporate (formerly insignificant!) high resistance layers which may limit scaling. In the case of the gate, these layers provide V_T tuning and reliability improvement. In the case of the S/D region, these layers serve as adhesion/barrier layers for the contact metals. Overall, the ultimate CMOS device will require significant advances in techniques to deposit thin conformal metals as well as increasing understanding of how to make barrier and adhesion layers more conductive.

One key limit is the fundamental resistivity of the metals and semiconductors used in the device. As is shown in Fig. 4, the resistivity of both metals and semiconductors increases with decreasing dimension due to scattering from the various surfaces. This suggests that the choice of materials will change as the dimensions get smaller (moving from materials of low bulk resistance to materials with good scattering properties). It also suggests developing new techniques to improve the scattering on wire surfaces, for example, coating wires with material which produces a density-of-states (DOS) similar to a perfect surface [3], [4].

S/D extension (tip) engineering will change significantly in the ultimate CMOS device due to the use of undoped channels (an undoped channel can be defined as a channel with a small (e.g., $< 1\%$) probability of having a single dopant atom in the channel, suggesting doping levels of $<$ 1E-16 cm^{-3} for undoped nanowire type structures). Undoped channels will be necessary in the ultimate device to enable improvements in variation and mobility. In an undoped device, there is little or no tip depletion, and thus, the S/D extension is short (or nonexistent) with associated improvements in overlap capacitance $(C_{\rm OV})$ and gate-induced drain leakage. The challenge is to create an abrupt and highly conductive S/D region that does not diffuse impurities into the hypershort channel. This is further complicated by the nonplanar and tight pitch architecture of the ultimate device, which will require new highly conformal (likely nonimplant) doping strategies. A variety of doping and annealing technologies are actively being researched to address these needs [5], [6].

Reducing the Schottky barrier height at the contact interface still remains critically important in the ultimate CMOS device. Techniques such as implant [7] and alloy [8] modulation, as well as more speculative techniques such as dipole modulation [9], are actively being researched. Metal S/D devices are an extension of these methods as they become an intriguing option when near-band-edge Schottky metal solutions are identified [10].

B. Capacitance and Next-Generation Transistors

Parasitic capacitance impacts circuit performance by increasing the capacitive load and thus increasing delay. In addition, the active power in a circuit is proportional to $C_{\rm dyn}V^2f$ (where $C_{\rm dyn}$ is the total dynamic capacitance, V is the operating voltage, and f is the frequency); thus, reducing $C_{\rm dyn}$ improves active power.

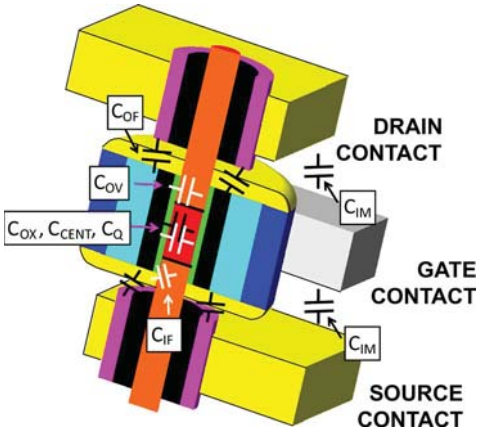

Fig. 5. Major capacitance elements in the ultimate CMOS device.

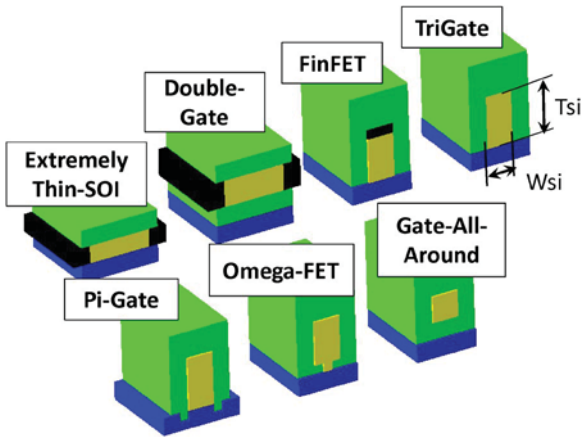

Fig. 6. Architectures which reduce source–drain interaction.

In many ways, capacitance may represent the most difficult challenge facing the ultimate CMOS device due to the decreasing distances between the gate and other parts of the device (such as the contact and the raised S/D region) and the 1/distance dependence of the parasitic capacitances.

The major capacitive components of the ultimate CMOS device are shown in Fig. 5. Starting in the center of the device, there are inversion, centroid and quantum capacitances associated with the gate and channel architecture ($C_{\rm OX}$, $C_{\rm CENT}, C_Q$), capacitance associated with the S/D extension ($C_{\rm OV}$), an inner fringe capacitance ($C_{\rm IF}$), an outer fringe capacitance largely determined by the spacer thickness ($C_{\rm OF}$), and the interlayer capacitances determined by distances between the various local transistor interconnects ($C_{\rm IM}$).

A key challenge in reducing capacitance around the transistor is incorporating spacer and contact etch stop materials that are simultaneously low-k and robust to processing. One approach is to develop new low-k materials that can withstand the processing conditions [11] (or alternatively to incorporate robust high-k materials that can be replaced by more fragile low-k materials later in the flow). A more exotic approach is to introduce air-gaps into the transistor section of the flow [12], [13]. While low-k dielectrics and air-gaps are strategies that are also evolving for Cu-interconnect use [14], [15], the additional challenges for air-gaps in the transistor region of the flow include integrating the contacts without shorting the contacts to the gate and supporting multiple selective etch steps (historically addressed by layers of Si_3N_4, SiC, and SiO_2 and associated selective etches).

III. Electrostatic Confinement

Improvements in electrostatics can enable beneficial tradeoffs for process and product integration. For example, improved electrostatics can enable much shorter effective channel length ($L_{\rm eff}$) at constant V_T and $I_{\rm off}$ (improving density scaling). Alternatively, much lower V_T can be obtained at constant $L_{\rm eff}$ and $I_{\rm off}$ (improving circuit performance). Another option is delivering a significant $I_{\rm off}$ benefit at constant $L_{\rm eff}$ and V_T (improving standby power).

There are two primary methods for improving the electrostatics: 1) implementing architectures which reduce S/D interaction (see Fig. 6) and 2) decreasing the effective electrical gate dielectric thickness.

A. Architectures Which Reduce Source–Drain Interaction

In conventional planar devices, minimizing the interaction between the source and drain is critical in improving the short-channel properties. The classic example is drain-induced barrier lowering (DIBL), where the drain voltage lowers the source barrier, forward biases the source junction, and increases the OFF-state leakage ($I_{\rm off}$)[16]. Measurements of DIBL and subthreshold slope (SS) are often used to characterize electrostatic confinement (with an ideal DIBL value ~0 mV/V and an ideal SS value ~60 mV/dec at room temperature).

An important caveat on the nearly universal use of DIBL/SS for electrostatic characterization is that effects other than electrostatics may also influence DIBL and SS measurements in advanced devices. Of particular interest is the degradation of DIBL and SS measurements in the presence of significant traps in the gate dielectric (see Section IV on Ge and III–V materials). This effect arises because interface traps ($D_{\rm it}$) can be viewed as dynamic charge which changes with applied bias. This bias-dependent dynamic charge creates different V_T shifts at different $V_{\rm gs}$ values and thus degrades DIBL and SS measurements. This $D_{\rm it}$-induced degradation can be misinterpreted as lack of electrostatic control of the device.

Historically, the accepted approach for improving short-channel effects in conventional planar devices was the following: 1) to create a retrograde (delta) profile under the channel; 2) to add an S/D extension (tip); 3) to add halo (pocket) implants under the S/D extension; and 4) to engineer the S/D extension for the smallest depth (X_J) while retaining respectable resistance [17]–[23].

1) ETSOI: It has been recognized since the mid-1980s that a silicon-on-insulator (SOI) device has the potential to improve planar short-channel properties by forming a channel in a silicon film whose thickness ($T_{\rm si}$) is thinner than the channel depletion depth [24], [25]. Such a device is called an extremely thin SOI (ETSOI) device [alternatively referred to as an ultrathin-body SOI device or a fully depleted SOI device(FDSOI)].

While SOI devices have been used as an alternative to bulk devices in the manufacturing environment for roughly the last decade, these production devices are partially depleted SOI (PDSOI) rather than ETSOI, with $T_{\rm si}$ dimensions significantly larger than the depletion depth. Such PDSOI devices do not offer the short-channel benefits of the ETSOI devices and suffer from other issues such as the floating body effect [17].

ETSOI devices benefit from using similar manufacturing to established PDSOI devices but possess improved short-channel properties and lower channel doping (with associated benefits in random-dopant fluctuations and mobility) and offer the possibility for body-bias [using thin buried oxide (BOX)].

The potential for body-bias in FDSOI devices is noteworthy. Body-bias is of interest to the design community (particularly to the system-on-chip (SOC) design community) as it permits active management of V_T in circuit design. Unfortunately, in conventional planar devices, body-bias effects decrease dramatically as the $L_{\rm eff}$ decreases [26], and in modern bulk and FinFET/TriGate devices, there is negligible body-bias. In contrast, ETSOI shows significant body-bias effect [27] as well as limited sensitivity of the body effect to $L_{\rm eff}$. This may offer some benefit to designers, particularly in the SOC product space. As a disadvantage, body-bias with thin BOX can degrade SS (if $V_B > 0$) by affecting the potential barrier at the back-gate. In addition, all body-bias schemes (particularly those which selectively alter the V_T of individual devices) must take into account the density degradation due to the additional routing and taps required to access the body.

The major challenge of ETSOI devices centers on the stringent ($<$ 10 nm) thickness requirements for $T_{\rm si}$. These small dimensions create several significant challenges, including the following: 1) thickness targeting and variation in ETSOI source material; 2) performance issues, including high parasitic S/D resistance and strain; and 3) quantum confinement and scattering effects.

While ETSOI is challenging to fabricate with production-worthy $T_{\rm si}$ thicknesses and tolerances, there has been a steady progression in the minimum achievable $T_{\rm si}$ moving from $\sim$100 nm in the 1980s and early 90s [28]–[30], down to the 15–20 nm range in early 2000 [31]–[33], and more recently to values below 10 nm [27], [34]–[42].

Performance issues, such as parasitic S/D resistance and strain, continue to be the most significant challenge in modern FDSOI devices. Traditional S/D extension engineering using ion implantation is difficult in these devices due to amorphization of the thin channel region, damage to the BOX, and dopant segregation [36]. Introducing strain is another major challenge in ETSOI devices (particularly for PMOS) as it is difficult to grow strained e-SiGe films on top of BOXs [36]–[38]. Quantum confinement effects also become critical in silicon ETSOI devices for $T_{\rm si}$ less than $\sim$5 nm. The primary impacts of quantum confinement are to increase the V_T and to alter the scattering behavior [43].

Overall, in spite of advances in resistance and strain engineering, ETSOI devices continue to perform with lower drive currents than comparable bulk planar or fully depleted devices created using multiple gate techniques (see Fig. 7).

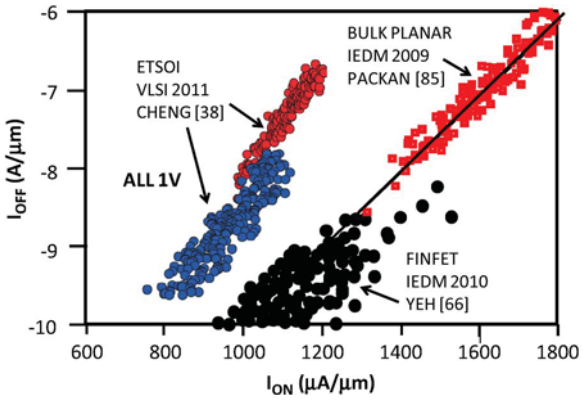

Fig. 7. Comparison of recent MOSFET results including FDSOI planar and fin architectures.

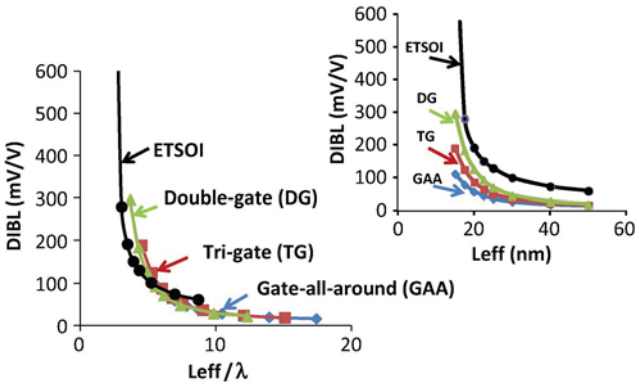

Fig. 8. (Main figure) Use of the "natural channel length" methodology to predict short-channel control for multiple gate devices. (Inset) Improvements in short-channel control as the gate number is increased from ETSOI to GAA.

2) MuGFETs: An alternative approach for short-channel control is to surround the channel with two (or more) opposing gates (see Fig. 6). Each additional gate improves the short-channel control (see Fig. 8). These gates can be oriented horizontally (a double-gate device [44], [45]) or vertically (a FinFET device [46]–[51]). SOI is not required in these multiple-gate devices (although it can be used to simplify manufacturing and reduce subfin leakage effects [52], [53]).

A simple but effective way to portray the improvement in fully depleted multiple gate devices is to use the "natural channel length" parameter λ_N (see Fig. 8). This parameter represents the extension of the electric field lines from the S/D regions into the channel region. A device will have minimal short-channel effects if $L_{\rm eff}$ is approximately 6$\times$ longer than λ_N. A generalized expression for λ_N can be written as

$$\lambda_N = \sqrt{\frac{\varepsilon_{\rm Si}}{N\varepsilon_{\rm ox}}} \cdot T_{\rm ox} T_{\rm si}$$

where $\varepsilon_{\rm ox}$ is the electrical permittivity of the gate dielectric, $\varepsilon_{\rm Si}$ is the electrical permittivity of the channel, N is the number of gates (ETSOI $= 1$, GAA $= 4$), $T_{\rm ox}$ is the gate dielectric thickness, and $T_{\rm si}$ is the film thickness (assuming for simplicity that film thickness $T_{\rm si}$ is equal to film width $W_{\rm si}$) [54]. Note that the effective length λ_N can be improved by increasing the number of gates, decreasing the gate dielectric thickness

(T_{ox}), decreasing the channel thickness (T_{si}), or decreasing the permittivity of the channel (ε_{Si}).

Double-gate (horizontally oriented; see Fig. 6) devices first appeared in the literature in the mid-1980s [44], [45], followed closely by vertically oriented double-gate (FinFET) devices [46]–[51], [55]–[57]. The improved short-channel effects resulting from more than two gates led to several important modifications including the TriGate architecture (gates on two sides and the top [58]–[60]), Pi-Gates (the side gates extend below the channel [61]), and Omega-FETs (the gate not only wraps around two sides and the top but underlaps part of the fourth [62]).

These multiple-gate devices have electrostatic advantages over conventional planar devices. In addition, the increased electrostatic confinement provided by multiple gates relaxes the manufacturing constraints in comparison to ETSOI (the critical width W_{si} of a double gate is approximately twice as wide as the critical thickness T_{si} of an FDSOI device with the same short-channel properties).

Multiple gate devices have an additional critical benefit over FDSOI devices in that the total electrical area may be significantly larger than the total footprint area. For example, if the height of a TriGate is 50 nm, the width is 10 nm, and the pitch is 40 nm, then the device has $(2 * 50 + 10) = 110$ nm of electrical channel width in a 40-nm pitch, for enhancement of 2.75× in drive current over a 40-nm channel width FDSOI device. In addition to providing a potential layout density benefit, modern products will also see a performance benefit from the increased drive current (in spite of the increased effective channel width) as products are typically more heavily loaded by parasitic capacitances (70%) than gate-originated capacitances (30%).

Since fully depleted devices [ETSOI and multiple gate field-effect transistors (MuGFETs)] control I_{off} through architecture rather than doping profiles, the channel can remain undoped (V_T targeting can be done through altering the workfunction of the gate [37]). Undoped channels have the potential for low random variation due to minimization of random dopant fluctuations. Undoped devices display the lowest measured random V_T variation values in the literature (Fig. 9, [63]).

Manufacturing and design complexity continue to be the most significant challenges for future MuGFET devices. Horizontally oriented MuGFET devices (double-gate devices) face the difficult challenges of a release etch to access the lower gate, as well as the requirements for highly conformal atomic layer deposition (ALD) gate dielectric and metal electrode processes. Vertically oriented MuGFET devices (FinFET/TriGate devices) face significant fin and gate patterning challenges associated with the nonplanar architecture. The high aspect ratios at tight fin pitches introduce new challenges for S/D and extension doping, likely requiring creation of new doping and annealing techniques. The granularity of the FinFET/TriGate architectures (a transistor can only have an integral number of fins) introduces significant new complexity into the circuit design process, particularly for low power geometries where single-fin devices may be common. Register files and memory circuits also face significant challenges due to the quantization of fins and the limited flexibility to tune single-fin solutions for optimal circuit stability [52], [53].

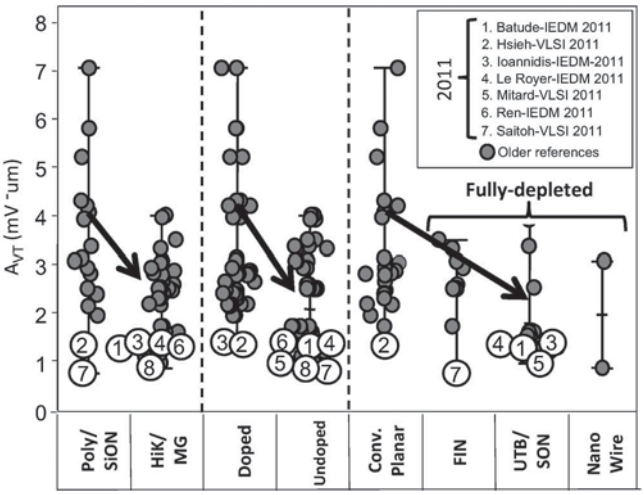

Fig. 9. Comparison of recent random variation (A_{VT}) values from the literature, illustrating improvement with high-*k*/metal gate and undoped structures, and the relative equivalence of all fully depleted technologies [63].

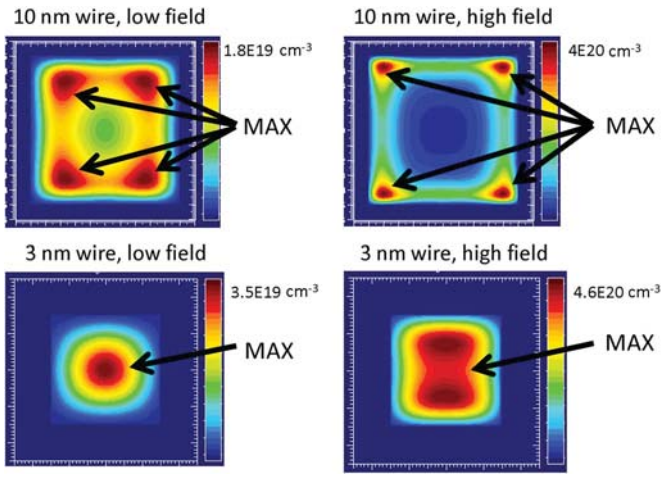

Fig. 10. Small diameter nanowire devices may operate in a regime where conduction moves from the surface of the device to the center [63].

Overall, in spite of the challenges of the nonplanar architecture, recent MuGFET devices have achieved higher drive currents than comparable generation FDSOI devices while retaining equivalent short-channel control (Fig. 6, [64]–[66]). In spite of the significant manufacturing issues, TriGate devices have been implemented successfully into manufacturing on the 22-nm node [2].

3) GAA Devices: GAA devices were first reported in the late 1990s [67]–[70]. GAA devices differ from Omega-FETs in that the gate wraps entirely around the device. Note that both lateral [67], [68] and vertical [69], [70] devices are possible with a GAA architecture. Both types provide optimal electrostatic confinement with the associated short-channel effect benefits.

Nanowires are an extreme case of GAA devices, having height and width dimensions roughly the same (or even cylindrical) and atomically small (< 10 nm) dimensions [71]–[76]. These devices operate in a size and field regime where carrier conduction moves from the surface of the device (as in conventional planar and finned devices) to the center of the device (see Fig. 10).

Nanowires represent the extreme limit of MuGFET scaling as they operate in the regime of fully depleted and quantum confined with associated changes in the transport physics [77]–[81]. Theoretical low field mobility studies for NMOS nanowires [78], [79] suggest flat or improved mobility down to a certain size (6–8 nm) and then rapid degradation in mobility at smaller sizes due to phonon and surface roughness scattering [80]. Theoretical mobility studies for PMOS are more complex (due to strain and band nonparabolicity) but also more optimistic, suggesting that ⟨110⟩ channel direction hole mobility down to 5-nm wire sizes remains competitive to planar mobility for high field and stress [81].

B. Decreasing the Electrical Gate Dielectric Thickness

Prior to ∼2005, the silicon industry aggressively scaled the silicon oxy-nitride gate dielectric thickness each generation. However, after the 90-nm generation, gate dielectric scaling slowed as lower power products became more important in the marketplace and gate leakage power limited further thickness scaling. Implementation of hafnium-based high-k gate dielectrics in 2007 at the 45-nm node enabled a return to electrical gate oxide thickness scaling while retaining low gate leakage power [82].

There are two different high-k gate stack fabrication techniques presently in use. The first of these is the gate-last or replacement gate technique [82]–[88]. This flow deposits the metal gate after transistor formation through removal of a dummy poly gate and replacement with the metal gate electrode. Gate-last processes typically incorporate one gate dielectric but two different metal gate electrodes (one for N and one for P). The second technique is the gate-first flow where the metal gate is fabricated at the historic gate oxide step in the process flow [89], [90]. Gate-first processes typically incorporate only one metal gate electrode and tune the N and P effective workfunctions with gate dielectric capping layers and channel material changes.

A significant benefit of the gate-last flow is that it deposits the metal gate materials after the high-temperature S/D formation steps are completed, thus offering a wider set of material options for tuning NMOS and PMOS gate work functions. The gate-last flow has the additional benefit of enhancing channel strain during the removal of the sacrificial polysilicon gate, one of the few strain enhancement techniques that simultaneously improves both N and P [83].

Gate-first flows are deceptively simple because they form the entire gate stack at the historical gate module location in the process flow. However, these flows require complex engineering of dipole-creating capping layers and multiple channel materials for effective workfunction control [89], [91].

Whether gate-first or gate-last, modern high-k gate dielectric stacks are actually multilayers, with a thin silicon oxy-nitride IL with $k \sim 4$, followed by a thicker high-k layer (with $k \sim 20$) and followed (in the case of gate-first) by a capping layer for effective workfunction control. In broad terms, reducing gate leakage due to tunneling is best controlled by thickening or increasing the k of the high-k region (the IL is too thin to do much good). In contrast, reducing the electrical oxide thickness T_{oxE} (and improving the electrostatic confinement) is best accomplished by thinning or increasing the k of the IL.

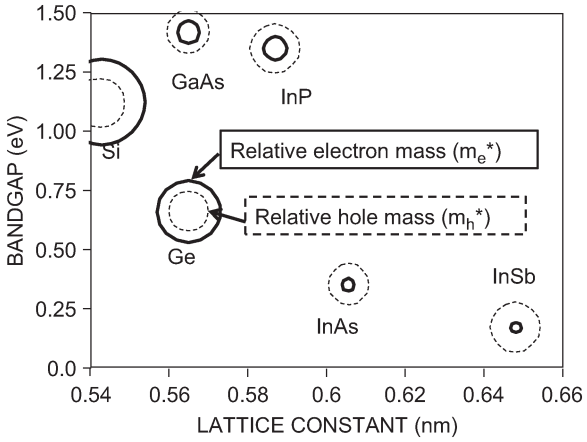

Fig. 11. III–V materials as a function of lattice constant and bandgap. The bubble size depicts the relative transport effective mass (m^*), with solid bubbles indicating electron m_e^* and dotted bubbles indicating hole m_h^*. Note InSb with the lowest m_e^* and Ge with the lowest m_h^*.

Two distinct strategies exist for reducing the thickness of the IL. The first approach is to simply not grow it in the first place (for example, with temperature optimization). The second approach is to use transition metals (such as Hf, Zr, and Ti) to decompose the SiO_2-like IL upon annealing, an effect called scavenging [92]. With either path, there is some concern that a thinner IL may degrade the mobility due to remote phonon carrier scattering [93].

Increasing the k of the IL is another path for reducing T_{oxE} without degrading mobility. A variety of materials have been explored for this, including combinations of La, Sr, Lu, and Al. The challenge with this approach is maintaining well-behaved work-function control [94].

IV. Channel Mobility

The on current at the virtual source of a MOS device can be simply expressed as $I = Qv$, where v is the velocity of the carriers and Q is the charge. Assuming Q is held constant, then improving the drive current requires improving carrier velocity, either in the mobility limit (where velocity $v = \mu E$) or in the ballistic limit (where the velocity $v = v_{\mathrm{inj}}$), As the most critical component in improving carrier velocity (in either case) is improving the effective mass (m^*) [95], then research and development efforts have primarily focused on intrinsically low m^* materials (see Fig. 11) and improving m^* (for example, through strain).

Note that, since effective mass is a critical part of channel mobility, then measured channel mobility is generally used as a proxy for carrier velocity. Therefore, the historical challenge of improving channel mobility continues to be a valuable goal towards achieving the optimal CMOS device.

Given the advanced state of silicon manufacturing technology, it is very unlikely that any material other than silicon will be used for the overall substrate in mainstream manufacturing. Thus, potential new channel materials must be integrated (with high yield) on conventional silicon substrates. Note that the

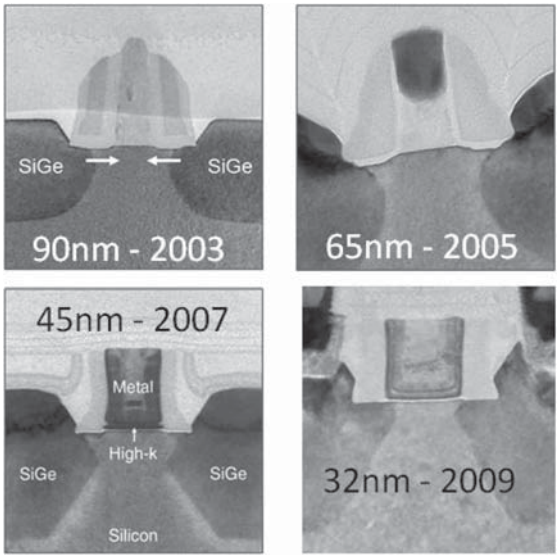

Fig. 12. Evolution of high-k and e-SiGe PMOS transistors between 90 and 32 nm [82]–[86], [96]–[99] illustrating the evolution of the S/D etch profile.

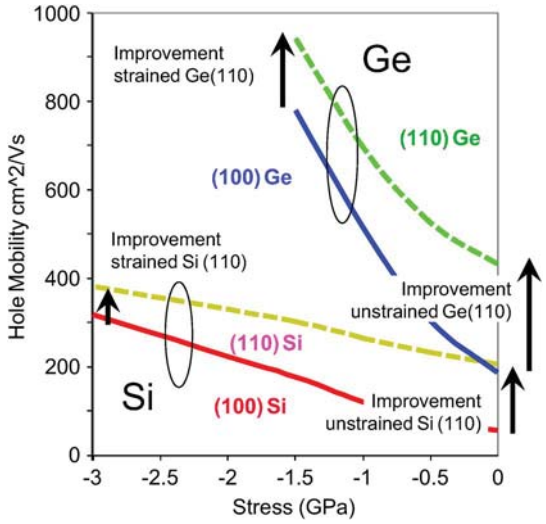

Fig. 13. Mobility and strain in Si and Ge as a function of stress and wafer orientation illustrating the reduction in improvement between (100) and (110) material (with a ⟨110⟩ channel direction) as a function of stress [100].

optimal n-material (perhaps a III–V) may be radically different than the optimal p-material (perhaps Ge-based), which means that novel new integration techniques will also be required. Finally, these new materials must demonstrate clear improvements over highly strained silicon, which is a steadily improving moving target.

A. Strain Advancements for PMOS

Generating uniaxial compressive strain with embedded SiGe (e-SiGe) has proven especially beneficial for silicon PMOS devices [96]–[99]. Multigenerational improvements have been achieved in e-SiGe through S/D etch profile optimization (see Fig. 12) and increased Ge percentage [100].

In e-SiGe, uniaxial strain is produced by growing pseudomorphic SiGe inside recessed Si S/D regions. Because the SiGe lattice is larger than the Si lattice, the SiGe S/D region expands, which compresses the adjacent Si channel. This results in a uniaxial stress along the channel (⟨110⟩) current flow direction. Furthermore, it is possible to enhance this uniaxial strain by combining the e-SiGe process with a replacement gate flow [83], [101].

The compression along the current flow direction from the e-SiGe S/D both warps and splits the valence band structure of silicon. The bandwarping produces improved effective transport mass for the heavy hole band (which is the ground state in the confined hole channel). In addition, the uniaxial stress increases the light-hole to heavy-hole band separation, reducing the interband scattering.

Since bandwarping effects depend only weakly on confinement, uniaxial strain gains show a minimal dependence on vertical field (in contrast to tensile biaxial strain where the gains are significantly reduced at a higher vertical field [98], [99], [102], [103]). Furthermore, uniaxial strain along the ⟨110⟩ channel direction has a significant advantage over biaxial strain due to the presence of shear strain components which are responsible for strong anisotropic warping of the bands, leading to repopulation of carriers to the bandstructure regions with the lighter transport mass [95], [104], [105].

Historically, there has been much interest in exploring nonstandard wafer and channel orientations. While significant improvements can result from combining strain and wafer/channel orientation changes, the performance results may not be additive. An excellent example is given by comparing (110) surface and ⟨110⟩ channel direction ((110)/⟨110⟩) material with (100)/⟨110⟩ orientation for PMOS under uniaxial compressive strain (see Fig. 13). PMOS in the (100) ⟨110⟩ orientation is not strongly affected by vertical confinement in a MOS device. However, it is strongly affected by compressive uniaxial strain. Thus, PMOS (100) ⟨110⟩ devices experience a large enhancement in mobility with increasing strain. In contrast, PMOS in the (110) ⟨110⟩ orientation is strongly affected by confinement but not as significantly affected by strain. Thus, PMOS (110) ⟨110⟩ devices have larger mobility at lower strain but improve less with increasing strain and may be surpassed by (100) ⟨110⟩ devices at high strain [100], [106], [107].

B. Ge-Based Systems for PMOS

Of the various advanced channel materials, Ge-based systems remain the most interesting for integration in a PMOS channel. Ge has the highest hole mobility of the major elemental semiconductors (note the possibility that GeSn alloys may have higher mobility than Ge [108]). SiGe manufacturing technology is well developed in the silicon industry due to the widespread use of e-SiGe S/D technology. In addition, the valence band structure of SiGe/Ge is not only similar to Si but behaves similarly to Si under both unixial stress and combined unixial/biaxial stress [100], [109].

Recall that Ge was the primary transistor material from the invention of the transistor in 1947 until the 1960s. The most critical reasons for switching from Ge to Si for early MOS technology remain the most critical issues today, namely: 1) the poor quality of the native GeO_x oxides compared to SiO_2; 2) the difficulty in controlling various surface and

interface states in Ge; and 3) the smaller bandgap of Ge compared to Si [110]. The primary changes between 1960 and 2012 leading to reconsideration of Ge channels are the advent of manufacturable high-k technologies using deposited dielectrics, deeper understanding of IL physics, and lower product voltages.

The key challenge with Ge (and SiGe) channels is rapid degradation in mobility with decreasing electrical oxide thickness [111]. The primary model for this degradation is poor quality germanium oxide at the Ge/dielectric interface. Thus, the goal is to create a high-quality low trap density IL between the gate dielectric and the Ge (SiGe). Note that this issue exists even if a high-k dielectric is used because an IL between the Ge and the high-k may still be formed (in fact, use of a high-k material may further complicate the issue by altering the chemistry of the GeO-GeO_2 film).

There are two major strategies being researched for resolving the gate dielectric challenges: one is the use of an ultrathin Si cap, and the second is creation of a higher quality dielectric IL than GeO (for example, GeO_2). The use of a thin Si-cap [112]–[114] is the most mature of the technologies under investigation with significant progress over the last decade [115]–[118] and particularly recently [109], [119], [120]. While, historically, GeO_2 was considered a poor passivation material, recent studies have reawakened interest in this path and its variants [121]–[127]. There has also been some success with direct thermal growth of GeON [128], [129]. In addition, transistors have been formed with Ge condensation [130], by oxidizing Ge through an ALD Al_2O_3 film [131], [132] using $SrGe_x$ interlayers [133], and through sulfur passivation treatments (which have also shown promise with InGaAs) [134], [135].

Another key challenge with Ge (and SiGe) is the significant reduction in energy bandgap with increasing Ge percentage, which results in high OFF-state leakage $(I_{\rm off})$ due to band-to-band tunneling (BTBT) (note that straining germanium, for additional mobility improvement, has the unfortunate side effect of further degrading the bandgap [136]). There are two major strategies for resolving the energy bandgap challenges with Ge (and with III–V NMOS materials as well). The first is to selectively apply Ge (SiGe) devices to low-voltage products where $V_{\rm nom} < E_g$. The second strategy is to fabricate these devices in a quantum-confined system (for example, an ultrathin body or nanowire) where the quantum confinement generates strong quantization of the energy levels and a larger effective bandgap [136], [137].

While significant research work has focused on the purely Ge channel [107], [111], [119], there is increasing effort on integrating SiGe (rather than pure Ge) channels. Although an early driver for SiGe channel implementation was to compensate for V_T targeting issues in a gate-first process [89], [138], there is increasing success in implementing SiGe channels for performance improvement [109], [120], [139], [140].

Although the vast majority of research work in Ge-based systems has focused on the Ge/SiGe channel, there has been some recent innovative work with GeSn materials [141], [142]. These materials are of interest both as S/D stressors for Ge channels (by analogy with SiGe being a S/D stressor for an Si channel) and as channel materials themselves.

C. Strain Advancements for NMOS

Early work on NMOS strain was done in biaxial strained NMOS Si on relaxed SiGe [143]–[148]. Biaxial strain can be introduced by pseudomorphic growth of Si channel material on relaxed SiGe. Because the Si lattice is smaller than the SiGe (or Ge) lattice, the Si layer will be stretched in two directions (biaxially). When the channel is in biaxial tension, the symmetry of the sixfold conduction band valleys is broken. The out-of-plane valleys (lower transport mass) drop in energy, and electrons move to populate these lower mass valleys. Additionally, the energy separation between valleys is increased, reducing scattering between bands and valleys.

For NMOS, once the carriers repopulate in to the twofold valleys due to the confinement valley splitting at high vertical field, little additional effective mass improvement is possible with biaxial stress. Additionally, reduction of scattering due to valley splitting with biaxial stress saturates at high vertical field. This results in reduced gains at high vertical field. Note, however, that uniaxial stress can warp the bands and result in improved gains at high field [81], [103], [104], [149].

Due to the challenges in manufacturing biaxially strained Si channel material on relaxed SiGe, other NMOS strain techniques began to appear in manufacturing processes. For example, the SiN layers commonly used for contact etch stops can impart useful stress to the NMOS devices [150], [151] even in a replacement gate flow [152].

As another approach, implanting the gate, capping and annealing the gate, and removing the cap can generate stress gains [153]. This method, termed the stress memorization technique (SMT), was shown to deliver significant improvement [154], to be repeatable multiple times in the same process [155], and to be compatible with high-k/metal gate [156].

More recently, a modification of the SMT technique, emphasizing creation of an S/D dislocation, has shown significant NMOS stress gains. Extremely deep preamorphization implants create multiple mask-edge dislocations in the S/D region, which significantly enhance the short-channel mobility [157], [158].

However, the "holy grail" of NMOS stress engineering has been to find an analogous NMOS system to the PMOS e-SiGe. The most popular candidate has been e-SiC [159]. The challenge with e-SiC is the low solid solubility of carbon, which makes it difficult to retain sufficient substitutional carbon in the lattice (particularly after anneals and implants) to impart useful strain. In spite of significant engineering effort, only modest gains have been achieved with NMOS e-SiC [160], [161].

D. III–V for NMOS

Of the various III–V materials, those with lattice constants less than $\sim$6 Å and bandgaps greater than $\sim$0.4 eV have received the most attention (see Fig. 11). With regard to lattice constant, while the wide range of lattice constants in these materials permits strain engineering, the larger lattice constants also pose challenges for fabrication due to lattice mismatch defects [162]–[165]. With regard to bandgap, while the lower bandgap materials have smaller electron effective masses, they are also susceptible to BTBT, limiting their maximum operating

voltages. Although it is desirable to operate at lower voltages to improve active power ($C_{\rm dyn}V^2f$), many products also require a high-voltage maximum-performance burst operating mode for short-term peak performance. Therefore, the most interesting materials are GaAs, InP, InAs, and their various ternary and quaternary alloys. These materials are widely used in opto-electronics and communications and are supported by a mature manufacturing industry.

Research on III-V materials is typically justified by citing the low effective mass and associated high carrier velocities and electron mobilities of these materials (see Fig. 11). However, low effective mass is only part of the picture. Recall that the on current of a MOS device can be simply expressed as $I = Qv = C\,(V_g - V_T)\,v$, where C is the total device capacitance. C can be expressed as the series combination of the dielectric capacitance ($C_{\rm ox}$), a quantum capacitance associated with the penetration of the Fermi level inside the 2D subbands of a quantum well due to the finite DOS (C_Q), and a centroid capacitance associated with the offset of the charge profile from the channel interface ($C_{\rm cent}$) [166]. In a conventional planar silicon MOS device, $C_{\rm cent}$ and C_Q are relatively large, and thus, the capacitance is dominated by $C_{\rm ox}$. However, in a low m^* device (such as a III-V device with high electron mobility) or in a highly quantum-confined device (such as a small silicon nanowire [167], [168]), both $C_{\rm cent}$ and C_Q can be relatively small, and the device can enter a charge-choked regime. This issue is sometimes called the "DOS bottleneck" or the "dark-space" issue [169].

The "DOS bottleneck" has two solution paths. The first approach is to operate the device at an intermediate effective mass, low enough to achieve velocity improvement over strained silicon while still high enough to mitigate DOS issues. Mobility measurements showing effective masses greater than the bulk value (attributed to nonparabolicity of the conduction band in conjunction with the quantization and strain effects) suggest operation is possible in this intermediate regime [166]. Recent experimental evidence showing device $I_{\rm on}$ improvement compared to strained scaled silicon at low $V_{\rm DS}$ for InGaAs MOSFETs [170], [171] and InAs HEMTs [172] further supports this approach. The second approach is to change the substrate orientation (for example, using the (111) surface [173]) in order to retain the low effective transport mass and to solve the DOS problem by including more conduction band valleys. While this can be quite complex (as the results change with both $T_{\rm oxE}$ and $T_{\rm si}$), theoretical results suggest that improvement over strained silicon is possible for several III-V materials [174].

As with Ge, one of the most critical challenges in III-V materials is the poor quality of the native oxide(s) compared to SiO_2. In addition, when a III-V surface is oxidized, a high density of interface states can be generated, which may cause Fermi-level pinning, increase the subthreshold swing, degrade the mobility, and create reliability issues.

There are a variety of strategies being researched for resolving the gate dielectric challenges in III–V materials, including the use of ILs, alternative dielectrics, indium-based compounds, and buried-channel approaches.

ILs are a rich area of research due to the complexity of the III-V IL surface physics. As an example, when a GaAs surface is oxidized, interface states appear generated by As–As dimers, Ga and As dangling bonds, and Ga vacancies [175]–[177]. Interestingly enough, Ga-O passivated surfaces appear to be free of interface states with energies inside the bandgap, which may simplify creation of N and P channel GaAs MOSFETs using Ga_2O_3 ILs [178]–[180]. A potential drawback of this approach is the lack of a manufacturable ALD process.

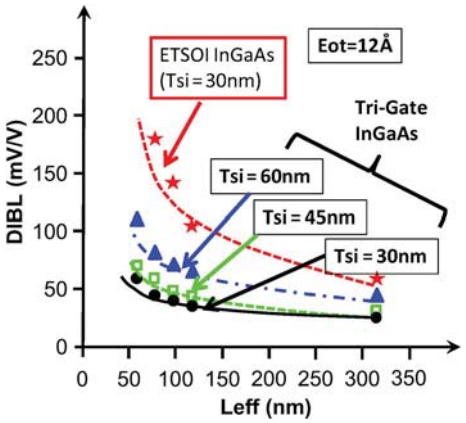

Fig. 14. TriGate InGaAs device illustrating DIBL improvement as a function of $L_{\rm eff}$ and $W_{\rm si}$ compared to an ETSOI InGaAs device [188].

Alternative dielectrics are also an active area of research, including Al_2O_3 with GaAs [181], InGaAs [182], InAs [183], and InP [184], as well as $TaSiO_x$ [170] and various rare earth dielectrics [185], [186]. Note that the states generated by group V dimers of In-containing compounds are predicted to lie inside the conduction band [176], which may explain the improvement in device characteristics when the In percentage is increased [187] and the success of InAs and InGaAs systems with a variety of dielectrics.

The difficulty in completely mitigating the various interface states in III-V systems has led to the idea of burying the channel underneath a high-bandgap material to reduce Coulomb scattering from the charged interface and bulk oxide states, as well as remote phonon scattering from oxide phonons. The best III–V devices have exploited many of these techniques, for example, in using InGaAs buried-channel structures equipped with an InP barrier layer using ALD $TaSiO_x$ as the dielectric [170].

The majority of the early research device work in III-V MOSFETs was done using MBE systems, often at universities. As a consequence, these designs have not attempted to optimize for state-of-the-art electrostatic confinement (short-channel control). However, there is no intrinsic reason why the advanced electrostatic control structures discussed in Section III cannot be applied to III-V devices. Recent examples of this are shown in Fig. 14 [188], where an InGaAs device has been fabricated in a TriGate configuration, and in [189], where an InGaAs HEMT has been fabricated in a vertical nanowire configuration.

V. Conclusion

As we look forward to the ultimate CMOS device (see Fig 15), we need to address both the familiar challenges of historical scaling (channel mobility, short-channel control, parasitic resistance, and capacitance) and the new challenges

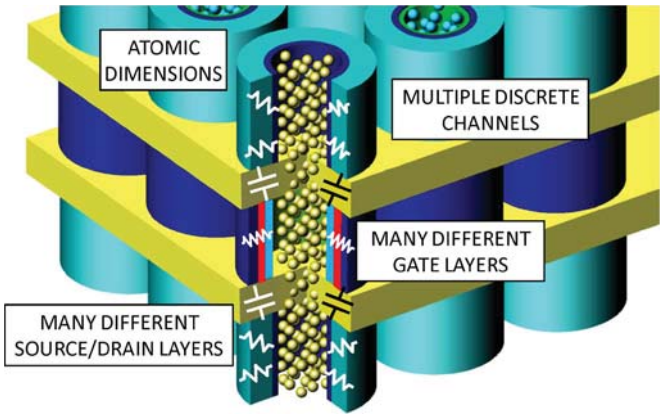

Fig. 15. Looking forward to the ultimate CMOS device.

associated with length scales on the order of atomic dimensions (atomic spacing limiting critical dimensions, interface and support layers dominating the physical structures, and a myriad of quantum effects including leakage, confinement, and scattering). Better atomic-scale materials (with higher mobility, higher conductivity, lower dielectric constant, and reduced scattering) are needed, as well as better atomic-scale process techniques (atomic layer processes, structured materials, and self-assembled materials). New physics effects will also appear at these length scales, requiring new experimental and theoretical research activities to resolve.

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Kelin J. Kuhn (F'11) received the Ph.D. degree in electrical engineering from Stanford University, Palo Alto, CA.

She is currently an Intel Fellow and a Director of Advanced Device Technology with the Components Research Group, Intel Corporation, Hillsboro, OR.