Fact Sheet

Intel at the 2012 IEEE International Solid-State Circuits Conference (ISSCC), Feb. 19-23, 2012

SAN FRANCISCO, Feb. 19, 2012 – Intel is delivering myriad presentations, panel discussions and demonstrations at this year's IEEE International Solid-State Circuits Conference (ISSCC). Topics include fundamental leaps in energy-efficient computing, integrated digital radio and SoC technology, efficient processor graphics and innovation with 22nm 3-D Tri-gate transistors. Below are highlights covering Intel's scheduled presence at the event.

Sunday, Feb. 19

- Forum F2: **"Robust VLSI Circuit Design and Systems for Sustainable Society,"** 8 a.m. Technology scaling brings new challenges to the design of reliable and robust VLSI circuits and systems – challenges that arise at the system, circuit and device levels. This forum provides an overview of such challenges, as well as recent advances in the domain of reliable and robust VLSI systems. Yih Wang, Intel principal engineer, will speak in this forum about robust SRAM Design in nanoscale CMOS circuit and technology.

- Tutorial T6: **"Power Management Using Integrated Voltage Regulators,"** 12:30 p.m. Aggressive technology scaling has enabled very high levels of transistor integration. Managing total power consumption has emerged as the most challenging task in today's highly complex microprocessor systems. This tutorial will review power management techniques implemented in recent designs. Tanay Karnik, principal engineer and program director, Intel Labs' Academic Research Office, will present this 90-minute tutorial.

Monday, Feb. 20

- Plenary Session 1.4: **"Sustainability in Silicon and Systems Development,"** 11:10 a.m. Moore's Law predicts that transistor integration capacity will continue to double every 2 years, providing the abundance of transistors needed to realize novel architectures for future platforms, enabling ever more intelligent electronic gadgets and devices. The major challenge we now face is energy efficiency. This talk by David Perlmutter**,** Intel executive vice president and chief product officer, addresses energy efficiency, and outlines challenges, solutions, and opportunities over the next decade for the compute continuum.

Session 3: Processors

- Session 3.1 **– "A 22nm IA Multi-CPU and GPU System-on-Chip,"** 1:30 p.m. This paper describes some of the circuit innovations in the upcoming Intel processor (codename "Ivy Bridge"), the first processor to utilize Intel's innovative new 3-D Tri-Gate 22nm transistor technology. See a real-life demonstration of the applications discussed in this paper at the "Industry Demonstration Session;" 4-7 p.m., Golden Gate Hall.

- Session 3.4 – **"32nm x86 OS-Compliant PC On-Chip with Dual-Core Atom® Processor and RF WiFi Transceiver,"** 3:15 p.m.
  This paper demonstrates Intel's future ability to integrate communications on the same silicon as processors to drive down cost and size for future mobile devices with a research test chip that for the first time integrates an RF transceiver for WiFi into an Atom-based SoC.

- Session 3.6 **– "A 280mV-to-1.2V Wide-Operating-Range IA-32 Processor in 32nm CMOS,"** 4:15 p.m.
  This paper describes Intel's Near Threshold Voltage (NTV) Processor, previewed by Intel President and CEO Paul Otellini and company CTO Justin Rattner at the Intel Developer Forum in San Francisco in September 2011. NTV technology is a breakthrough concept that could allow processors from mobile to HPC to operate in modes that are 5-10x more energy efficient than today. The paper provides details of the IA-32 concept processor, fabricated in 32nm CMOS technology and demonstrating reliable ultra-low voltage operation, power consumption as low as 2mW, and energy-efficient performance across the wide voltage range of 280mV (3MHz) to 1.2V (915MHz). See a real-life demonstration of the applications discussed in this paper at the "Industry Demonstration Session;" 4-7 p.m., Golden Gate Hall.

- Session 3.8 **– "A Reconfigurable Distributed All-Digital Clock Generator Core with SSC and Skew Correction in 22nm High-k Tri-Gate LP CMOS,"** 5 p.m.
  This paper describes a digital clock generator that can be reconfigured for microprocessors, SoCs and wireless transceivers. Traditionally, such clocks have been made with analog circuits, but transistor speedup and scaling from Moore's Law enables the clock generator to be built digitally. This has numerous advantages such as lower power, which leads to longer battery life, and less silicon area, reducing cost. It also allows for the integration of other features that were previously implemented off-chip, further reducing system cost.

Industry Demonstration Session, 4-7 p.m.
ISSCC 2012 will hold industry demonstration sessions (IDS), intended to demonstrate real-life applications made possible by new ICs presented this year, where Intel will show applications discussed in these papers:

- Session 3.1 **"A 22nm IA Multi-CPU and GPU System-on-Chip"**
- Session 3.6 **"A 280mV-to-1.2V Wide-Operating-Range IA-32 Processor in 32nm CMOS" –** (Intel's Near-Threshold Voltage Processor)

Evening Session:

- ES4: **"Optical PCB Interconnects, Niche or Mainstream?"** 8 p.m.
  This session reviews the latest in optical interconnect-related circuit design, prospects for optics use in mainstream I/O applications, and provides comparison to copper-based solutions and associated roadmaps. Mario Paniccia, Intel Fellow and director, Photonics Technology Lab, will discuss Integrated Silicon Photonics and applications in and around PC/Servers as part of this session.

Tuesday, Feb. 21

Session 10: "High-Performance Digital"

- Session 10.1 – **"A 280mV-to-1.1V 256b Reconfigurable SIMD Vector Permutation Engine With 2-Dimensional Shuffle in 22nm CMOS,"** 8:30 a.m.
  Winner of the 2012 ISSCC Distinguished Technical Paper award, this paper describes Intel Labs' research to extend Near Threshold Voltage technology (see Session 3.6 above) to circuits aimed at processor graphics applications. As future personal and professional computing applications become more visual, it is important to ensure that Intel's SIMD (single instruction, multiple data) graphics engines can benefit from the frugal computing modes enabled by NTV technology.

- Session 10.3 – **"A 1.45GHz 52-to-162GFLOPS/W Variable-Precision Floating-Point Fused Multiply-Add Unit with Certainty Tracking in 32nm CMOS,"** 9:30 a.m.
  This paper describes a test chip to make floating point calculations more efficient, particularly for visual applications computed by Intel's future processor graphics engines. The paper proposes a first of its kind variable-precision scheme that enables 24-, 12- and even 6-bit precisions, and tracks the amount of certainty that is needed so that only the required amount of digits are used. This has the potential to cut power in half for these applications. In addition, the research incorporated NTV technology (see Session 3.6 above) to attain low-voltage modes with an additional 7x efficiency gain.

- Session 10.4 – **"A 2.05GVertices/s 151mW Lighting Accelerator for 3-D Graphics Vertex and Pixel Shading in 32nm CMOS,"** 9:45 a.m.
  Intel's future processor graphics engines aim to optimize the processing of 3-D scenes, specifically, the lighting calculations that determine the colors of the pixels on your screen. This paper describes an experimental accelerator that transforms complex floating point calculations from linear to logarithmic, and describes a test chip implementing this technique with 5x acceleration in throughput and latency for lighting calculations.

Session 9: Wireless Transceiver Techniques

- Session 9.4 – **"A 20dBm 2.4GHz Digital Outphasing Transmitter for WLAN Application in 32nm CMOS,"** 10:15 a.m.
  This paper is about a WiFi-compliant (802.11g/n) transmitter using Intel's 32nm process and techniques leveraging Intel transistors to achieve record performance (power consumption per transmitted data better than state-of-the art). These techniques are expected to yield even better results when moved to Intel's 22nm process and beyond.

Session 11: Sensors & MEMs

- Session 11.8 **– "Ratiometric BJT-Based Thermal Sensor in 32nm and 22nm Technologies,"** 11:45 a.m.
  The paper is about a new thermal sensor circuit used in microprocessors. It is one of the first analog circuits reported in Intel's upcoming 22nm process node. Intel shrunk the circuit by 10x as compared to the previous Intel sensor, a exceptional achievement in analog design.

Session 13: High-Performance Embedded SRAM

- Session 13.1 – **"A 4.6GHz 162Mb SRAM Design in 22nm Tri-Gate CMOS Technology with Integrated Active V_{MIN}-Enhancing Assist Circuitry,"** 1:30 p.m.
  This paper describes a 162Mb, 22nm SRAM array with special circuits to enable unprecedented performance at low voltage. On-die memory caches implemented with SRAM arrays are critical for speeding up access to instructions and data, and are widely used in microprocessors and SoCs. Hence, improving their performance, their bit density – to enable larger arrays and/or reduce die size – and reducing power per bitcell are of utmost importance. Intel describes a design that provides 85 percent greater density than comparable 32nm array designs, while achieving a 70 percent improvement in performance relative to 32nm at voltages below 0.8V.

- Session 13.3 – **"Capacitive-Coupling Wordline Boosting with Self-Induced V_{CC} Collapse for Write V_{MIN} Reduction in 22-nm 8T SRAM,"** 2:30 p.m.
  One of the major challenges for microprocessor designs in advanced process technologies is scaling of minimum operating voltage. Write failures in 8T SRAM cache and register file arrays often limit the minimum operating voltage. This paper demonstrates a new capacitive-coupling wordline boosting technique with self-induced voltage collapse in a 22nm test chip, which promises significant reduction in minimum write voltage with minimal area overhead, and thereby helps widen the dynamic operating range of the design.

Session 14: Digital Clocking & PLLs

- Session 14.4 – **"A TDC-Less ADPLL With 200-to-3200MHz Range and 3mW Power Dissipation for Mobile SoC Clocking in 22nm CMOS,"** 4:30 p.m.
  All modern SoCs require a special on-chip circuit called a Phase Locked Loop (PLL) that generates the clock pulses. Intel has designed a digitally controlled PLL in its 22nm process featuring tri-gate transistors, that meets the low power and low area requirements of mobile SoC applications such as tablets and cellular phones as described in this paper.

Industry Demonstration Session, 4-7 p.m.
ISSCC 2012 will hold IDSes intended to demonstrate real-life applications made possible by new ICs presented this year, where Intel will show applications discussed in these papers:

- Session 3.1 **"A 22nm IA Multi-CPU and GPU System-on-Chip"**
- Session 3.6 **"A 280mV-to-1.2V Wide-Operating-Range IA-32 Processor in 32nm CMOS" –** (Intel's Near-Threshold Voltage Processor, codename "Claremont")

Evening Session, 8 p.m.

- ES5: **"Vision for Future Television"**
  In this session, representatives from Intel, LG Electronics, Toshiba and Nagoya University will discuss future technologies that could close the gap between current TV capabilities and customer demand. Brendan Traw, Intel Fellow, will talk about television's future.

Wednesday, Feb. 22

Session 20 – RF Frequency Generation

- Session 20.6 – **"A 32nm CMOS All-Digital Reconfigurable Fractional Frequency Divider for LO Generation in Multistandard SoC Radios with On-the-Fly Interference Management,"** 11:15 a.m.
  This paper describes circuit technologies designed to facilitate the integration of WiFi, WiMax, and other wireless technologies directly into SoCs for mobile devices. This could lead to thinner, lighter, cheaper and more capable tablets, phones and embedded devices. The research tackles three key challenges: 1) having one integrated radio to generate a wide range of signals across the WiFi and WiMax communications bands; 2) ensuring these radios play well with other often unknown components of an SoC; and 3) replacing tricky analog RF components with digital ones to facilitate Moore's law scaling to future process nodes. Specifically, this paper describes a new, reconfigurable "fractional frequency divider" that achieves all of the above.

Thursday, Feb. 23

Forum F3: **"10-40 Gb/s I/O Design for Data Communications,"** 8 a.m.
The importance of I/O data rates beyond 10Gb/s is growing rapidly. Supporting these data rates introduces new challenges beyond those faced at lower data rates. This forum will present both electrical and optical I/O approaches to meeting these challenges at the architecture and circuit levels. Intel will talk about techniques to improve power efficiency.

Forum F6: **"Power/Performance Optimization of Many-Core Processor SoCs,"** 8 a.m.
As performance scaling per-core continues to slow down, designers are faced with myriad challenges in efficiently using transistors offered by modern processes. This forum will address next-generation computing challenges in the context of highly parallel manycore processors. Mark Anders, an Intel research scientist, will talk about high-performance, energy-efficient NoC fabrics.

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