Intel Architecture Press Briefing

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(intel®)

Today's News
Intel Technology: Delivering on the Promise

Mission Critical

Tick-Tock

Expandable Server

Nehalem

Larrabee

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Tukwila: Delivering Performance to World's Most Powerful Computers

- Quad-core with 30 MB cache
- 2 billion transistors
- Multi-Threading Technology
- Intel QuickPath interconnect
- Dual Integrated Memory Controllers
- Estimate >2x* performance
- Mainframe-class RAS

"With Intel's upcoming quad-core Tukwila processor, Windows Server solutions running on Itanium-based systems will provide an even more scalable, reliable, agile and dynamic datacenter foundation for our customers."

—Bill Laing, GM Windows Server & Solutions Division, Microsoft
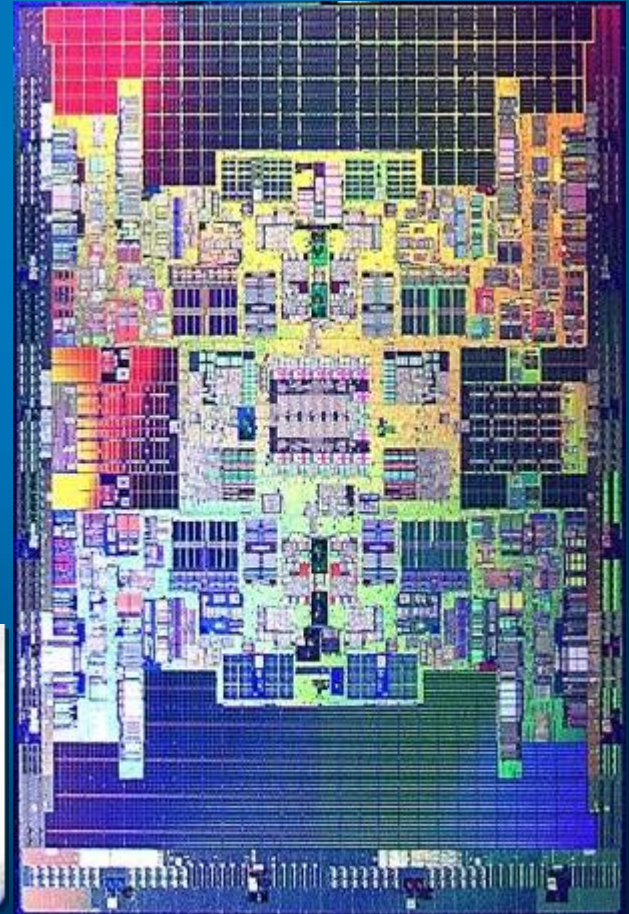
* Compared to Dual-core Itanium® Processor 9100 series

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Product Cadence for Sustained Leadership

2007-08

Penryn
Processors
45nm

TICK

TOCK

Delivering Products on Schedule and Moore's Law

(intel)

Expandable and Scalable:
Quad-Core Intel® Xeon® processor 7300

- Caneland platform built for virtualization and consolidation
- Energy Efficient performance: Leading in benchmarks
- Scalable
- Enterprise proven reliability and investment protection
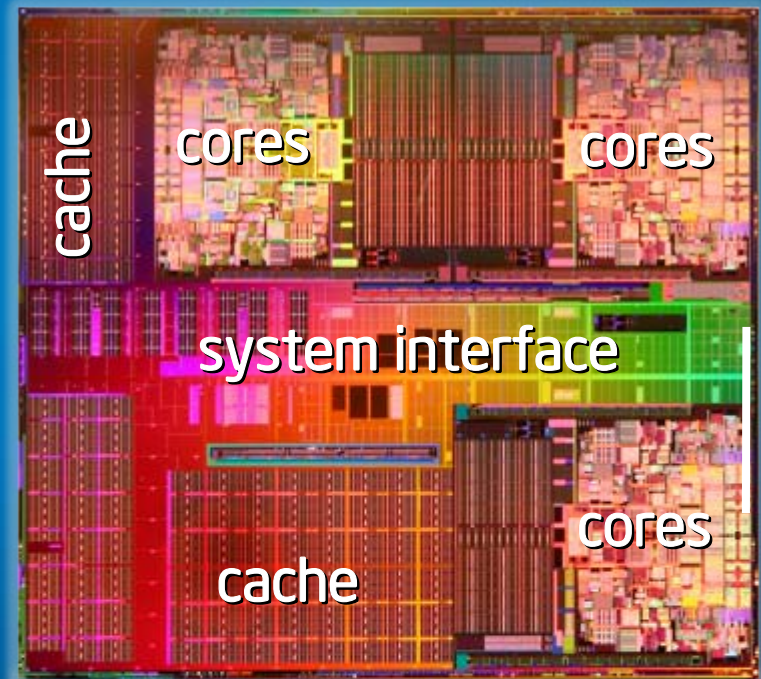- Great customer acceptance

Industry's Virtualization Platform of Choice

Expandable and Scalable: Gets Better with Dunnington

- 6 core Processor
- 1.9 billion transistors
- 45nm Hi-K technology
- 16 MB L3 cache
- Latest Intel virtualization capabilities
- Socket compatible with Caneland platform
- Available 2H'08

cache

cores

cores

system interface

cores

cache

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Energy Efficiency: Top SPECpower* Results
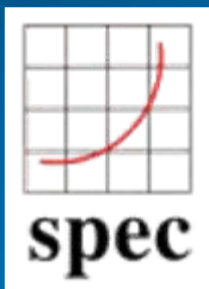
spec

Rank	Sponsor	SPECPower_ ssj2008 result	Platform	Processors
1	HP	778	DL180 G5	2x Intel® Xeon® E5450
2	Dell	719	PE 2950 III	2x Intel® Xeon® E5440
3	Dell	712	PE 1950 III	2x Intel® Xeon® E5440
4	HP	698	DL160 G5	2x Intel® Xeon® E5450
5	FSC	690	RX300 S4	2x Intel® Xeon® E5440
6	Dell	682	PE 2950	2x Intel® Xeon® E5440
7	FSC	667	TX150 S6	1x Intel® Xeon® X3220
8	HP	662	DL360 G5	2x Intel® Xeon® E5450
9	HP	546	DL580 G5	4x Intel® Xeon® L7345
10	Intel	468	SM 6025B	2x Intel® Xeon® L5335

First industry standard Energy Efficiency benchmark

Public SPECpower results from http://www.spec.org/power_ssj2008/results/power_ssj2008.html as of Feb 28, 2008

SPECPower_ssj2008 results measured as ssj_ops/watt

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Product Cadence for Sustained Leadership

2007-08

Penryn
Processors
45nm

Nehalem
Processors
45nm

TICK

TOCK

Driving Products to Deliver on Moore's Law

Nehalem Micro-architecture: Dynamically Scalable and Innovative New Design

Scalable from 2 to 8 cores

Micro-architecture enhancements (4 –wide)

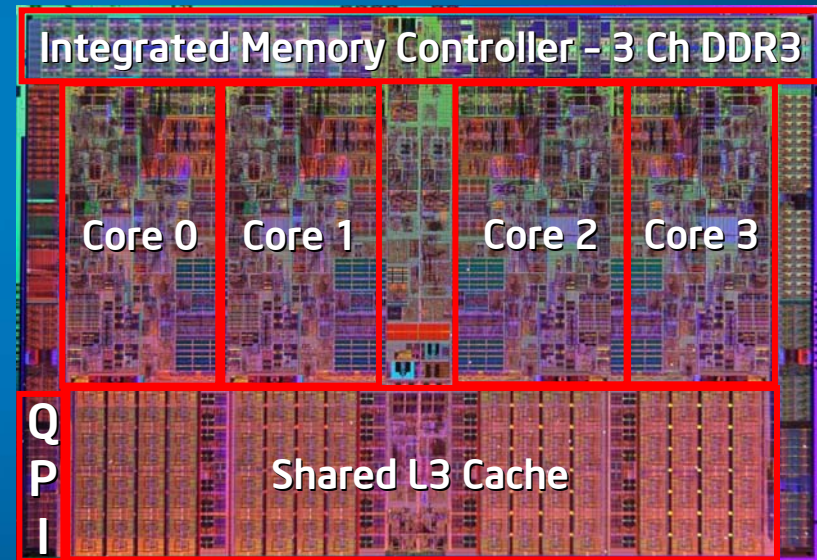2-way simultaneous multi-threading

Integrated memory controller

QuickPath interconnect

Shared and Inclusive Level-3 cache
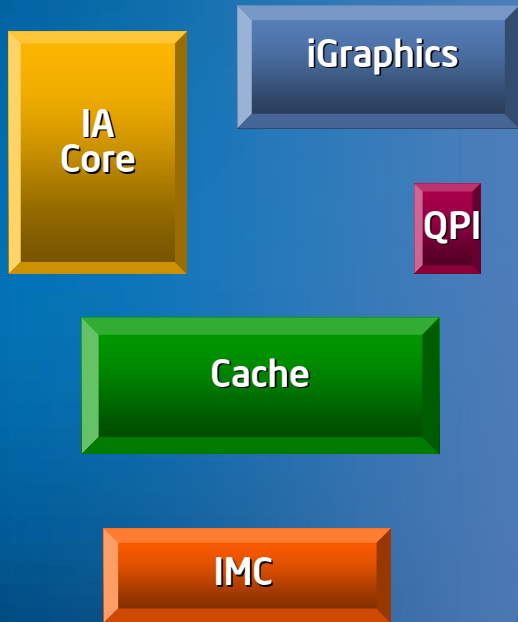
Dynamic power management
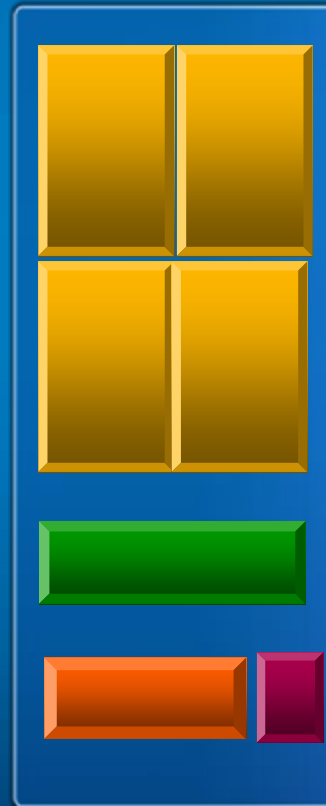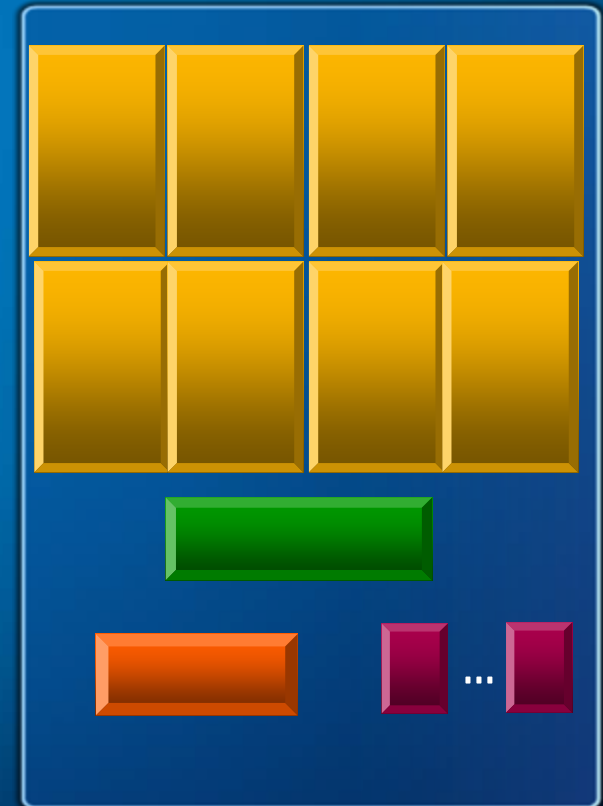
SSE 4.2

Production: Q4'08

Integrated Memory Controller – 3 Ch DDR3

Core 0   Core 1   Core 2   Core 3

QPI

Shared L3 Cache

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Nehalem Design Scalable Via Modularity

Nehalem Building Block Library

iGraphics

IA Core

QPI

Cache

IMC

Ex: 4 Core

...

Ex: 8 Core

...

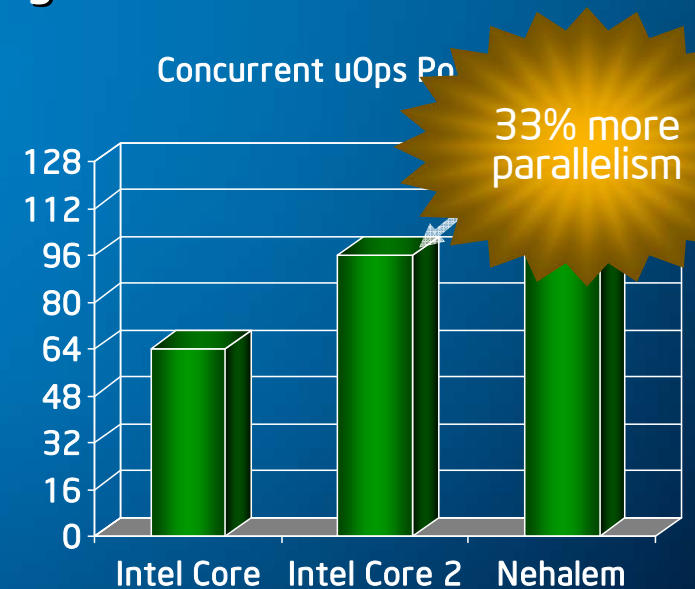**Sample Range of Product Options**

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Nehalem: Core uArch Enhancements

Foundation: Intel® Core™ Microarchitecture

Significant Performance and Efficiency Enhancements

- **Increased parallelism**
  - ➤ **33% more micro-ops in flight possible**
- **Enhanced algorithms**
  - ➤ **Faster "unaligned" cache accesses**
  - ➤ **Faster synchronization primitives**
- **Further branch prediction enhancements**
  - ➤ **New 2nd level branch predictor**
  - ➤ **Renamed Return Stack Buffer**

Concurrent uOps Po...

33% more parallelism

	128
	112
	96
	80
	64
	48
	32
	16
	0

Intel Core   Intel Core 2   Nehalem

Builds upon Industry Leading 4 Instruction issue Intel® Core micro-architecture
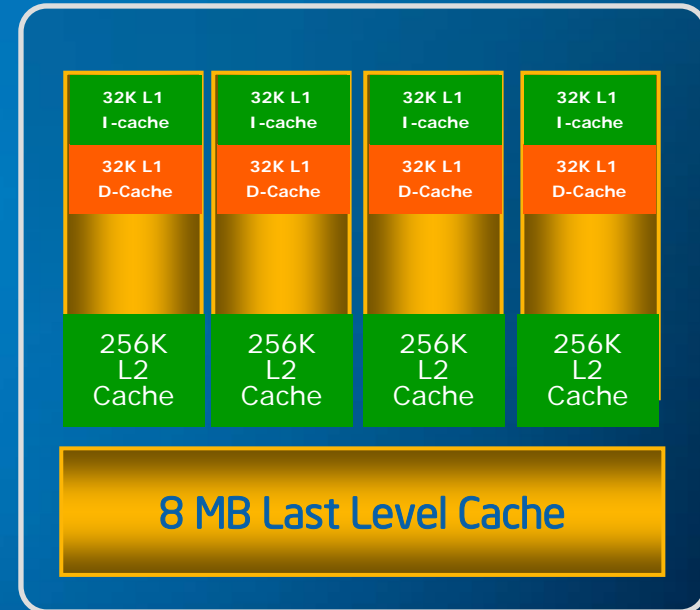
Simultaneous Multi-Threading (SMT)

- Each core able to execute two software threads simultaneously

- Extremely power efficient

- Enhanced with larger caches and more memory bandwidth

- Benefits

  - Highly threaded workloads (eg, multi-media apps, databases, search engines)

  - Multi-Tasking scenarios
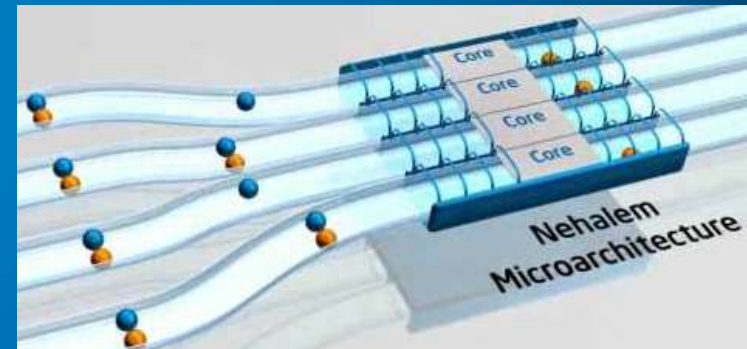
Simultaneous Multi-threading Enhances Performance and Energy Efficiency
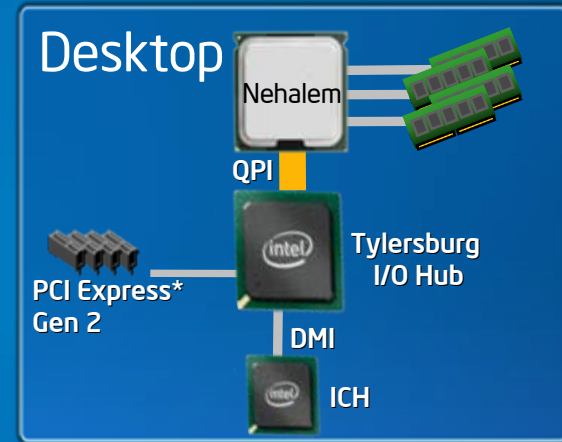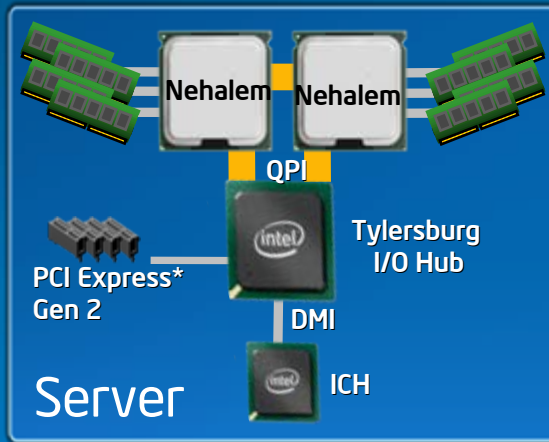
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Enhanced Cache Subsystem

- **New 3-level Cache Hierarchy**
  - L1 cache same as Intel Core™ uArch
    - 32 KB Instruction/32 KB Data
  - New 256 KB/core, low latency L2 cache
  - New Large 8MB fully-shared L3 cache
    - Inclusive Cache Policy - minimize snoop traffic
- **New 2-level TLB hierarchy**
  - Adds 2nd level 512 entry Translation Look-aside Buffer

32K L1 I-cache	32K L1 I-cache	32K L1 I-cache	32K L1 I-cache
32K L1 D-Cache	32K L1 D-Cache	32K L1 D-Cache	32K L1 D-Cache
256K L2 Cache	256K L2 Cache	256K L2 Cache	256K L2 Cache

8 MB Last Level Cache

Superior multi-level shared cache extends Intel® Smart Cache technology

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Nehalem/Tylersburg Platforms
(High End Desktop and Server/Workstation)

- **Intel® QuickPath Interconnect**
  - **New point to point interconnect**
  - **2 links per CPU socket**
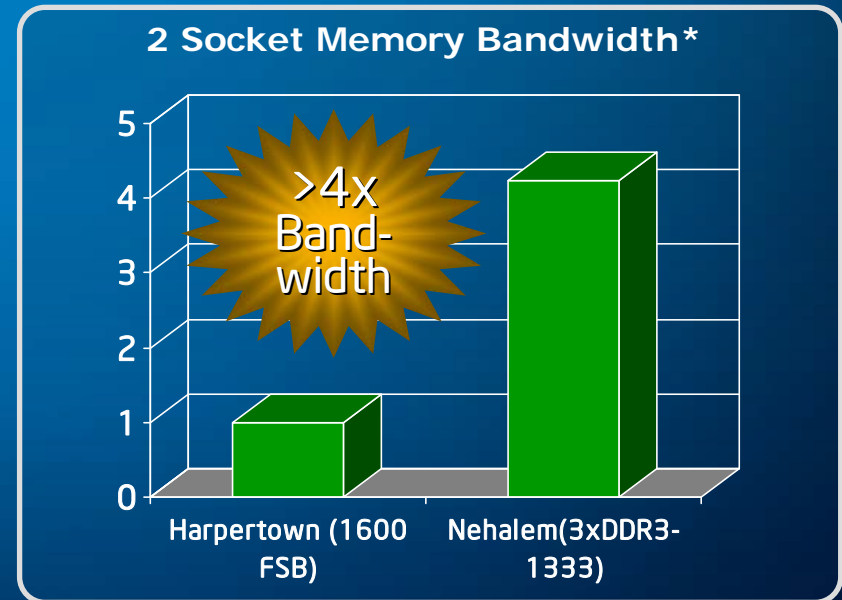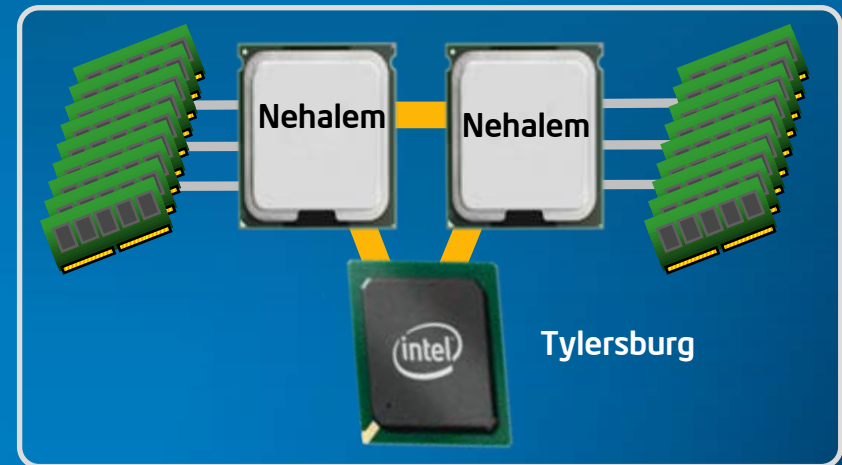 - **Up to 25.6 Gb/sec total bandwidth/link**

- **Integrated DDR3 Memory Controller**
  - **3 channels per processor**
  - **Massive amounts of Bandwidth**
  - **Significant Memory Latency Reduction**

Huge Latency Decrease and Bandwidth Increase over Prior Generation

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Nehalem High End Desktop/Server IMC

- **3 channels per socket**

- **Up to 3 DIMMs/channel**

- **DDR3-800, 1066, 1333**
  - ➢ **Future scalability**

- **Supports RDIMM and UDIMM**

- **Very low latency**

- **Very high bandwidth**

- **Built-In RAS Features**

Nehalem Nehalem

Tylersburg

2 Socket Memory Bandwidth*

>4x Band-width

5
4
3
2
1
0

Harpertown (1600 FSB)   Nehalem(3xDDR3-1333)

Leadership Memory Bandwidth

Product Cadence for Sustained Leadership

2009-10

Westmere
Processors
32 nm

Sandy Bridge
Processors
32 nm

TICK

TOCK

Continuing the Pace of Innovation

Intel® Advanced Vector Extension (AVX)

256-bit vector extension to SSE for FP intensive applications

| KEY FEATURES	BENEFITS
Wider Vectors Increased from 128 bit to 256 bit	Up to 2x peak FLOPs output
Enhanced Data Rearrangement Use the new 256 bit primitives to broadcast, mask loads and do data permutes	Organize, access and pull only necessary data more quickly and efficiently
Three Operand, Non Destructive Syntax Designed for efficiency and future extensibility	Fewer register copies, better register use, more opportunities for parallel loads and compute operations, smaller code size

Visual Computing: Graphics Re-defined

Mainstream Graphics

- Triangle / Rasterization

- Rigid pipeline architecture

- Tools constrained by architecture

- Inefficient for non-graphics computing
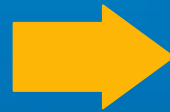
Visual Computing

- New life-like Rendering e.g. Global illumination

- Programmable, ubiquitous architecture

- High definition audio and video processing

- Combines with model based computing (e.g. Physics)

Visual Computing

Acquiring, Analyzing, Modeling and Synthesizing Visual Workloads

Photorealistic 3D Rendering

Computational Modeling

Interactive User Interface

High Definition Audio, Video

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Visual Computing: What Does it Take?

Intel Leadership

- Platforms: Client, Workstation, Server
- CPU, Graphics, Media Architecture
- Process and Technology Leadership
- Software, Tools & Developer Support

Photorealistic 3D Rendering

Computational Modeling

Interactive User Interface

High Definition Audio, Video

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Larrabee: Visual Computing Architecture

- **Many IA cores**
  - ➢ **Scalable to TeraFLOPS**

- **New cache architecture**

- **New vector instruction set**
  - ➢ **Vector memory operations**
  - ➢ **Conditionals**
  - ➢ **Integer and FP arithmetic**

- **New vector processing unit / wide SIMD**

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Intel Software: Unleashes Developer Freedom

Industry Leading Intel® Software Tools

Addresses development and performance tuning needs

Intel® MPI Library
Intel® Thread Checker
Intel® Thread Profiler
Intel® VTune™ Performance Analyzers
Intel® Performance Libraries
Intel® Threading Building Blocks
Intel® Compilers

Intel Software Products

Visual Computing Tools & Resources

Extending Intel® Software for Larrabee Architecture

Supports industry standard APIs (DirectX* & OpenGL*)

Risk Factors

This presentation contains forward-looking statements. All statements made that are not historical facts are subject to a number of risks and uncertainties, and actual results may differ materially. Please refer to our most recent Earnings Release and our most recent Form 10-Q or 10-K filing available on our website for more information on the risk factors that could cause actual results to differ.

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(intel) Rev. 2/26/08

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