



Moorestown Platform: Based on Lincroft SoC Designed for Next Generation Smartphones

HOT CHIPS 2009

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Agenda

- Moorestown Platform Overview
- Moorestown Platform Re-Partitioning
- Lincroft SoC: Designed for
 - High Performance
 - Low Power
- Summary

Major Reductions in Power and Form Factor



2008



Menlow

Board Size 8,500 sq mm
Standby Power 1.6W

2009/2010



Moorestown

Board Size – Reduced 2x
Standby Power Up to 50x*

Forecast

2011



Medfield

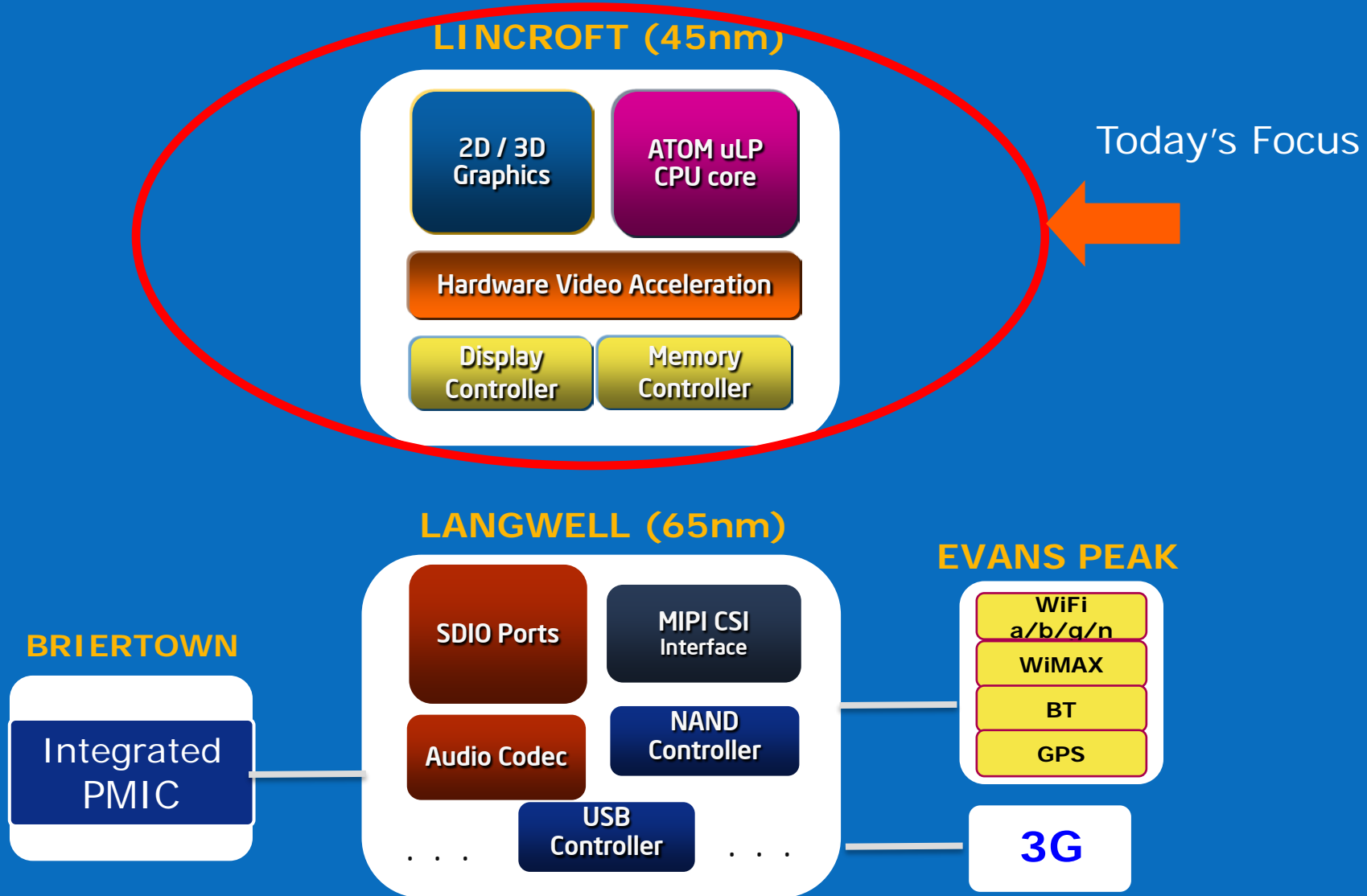
Board Size - Reduced
Standby Power - Lower

Forecast

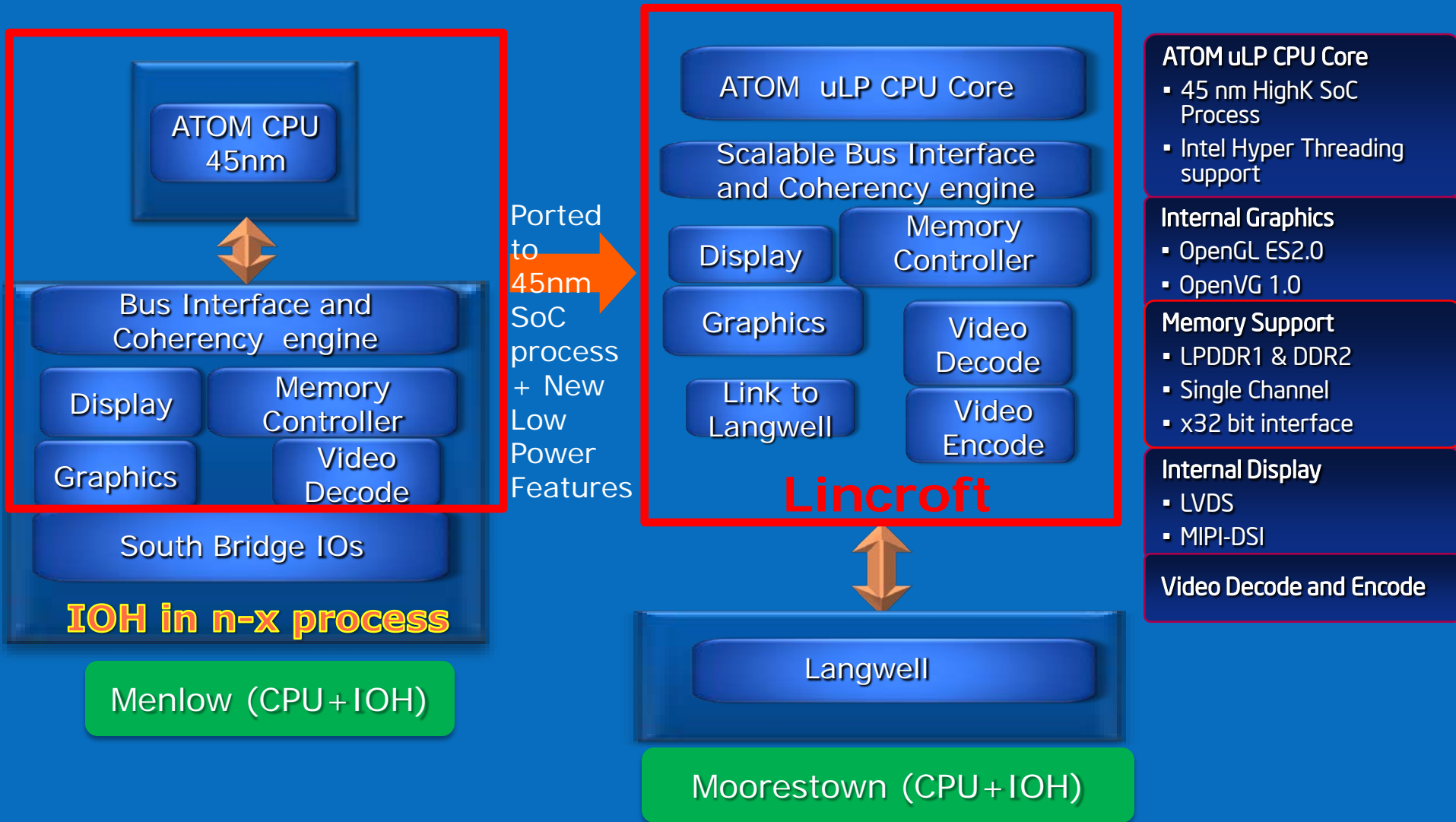
*Power and Form Factor Reductions On Track
Moorestown Idle Is Similar To Phone Level Power*

•Moorestown Platform Idle power reduction (based on current platform features) compared to Menlow Platform
•Drawings are not to scale

Moorestown Platform Overview



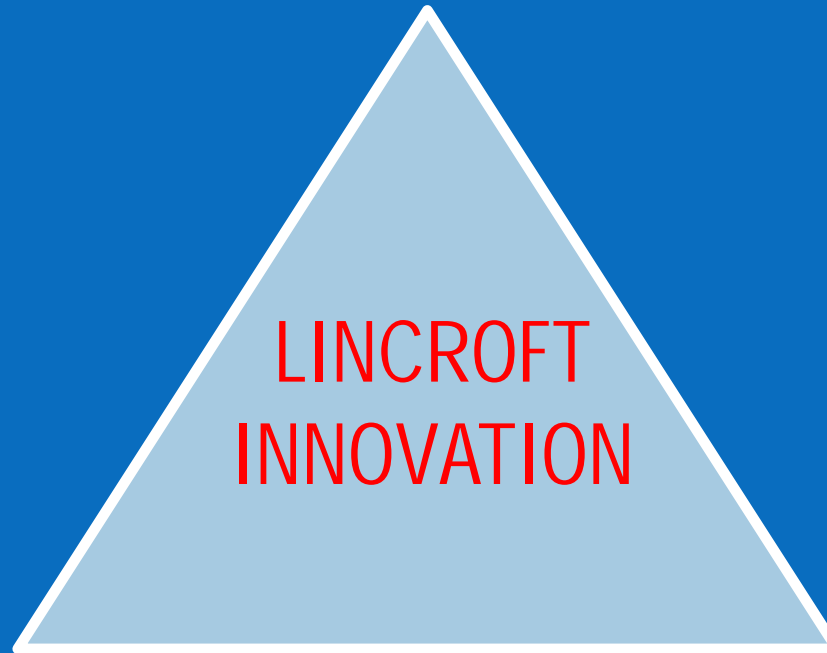
Moorestown Platform Re-Partitioning



Re-Partitioning using 45nm SoC process → Higher Performance and Ultra Low Power

Lincroft Innovation Vectors

High Performance
for amazing Internet Experience



Dramatically Lower Power
Upto 50x platform idle power*

Small Size
For Smartphone Form Factor

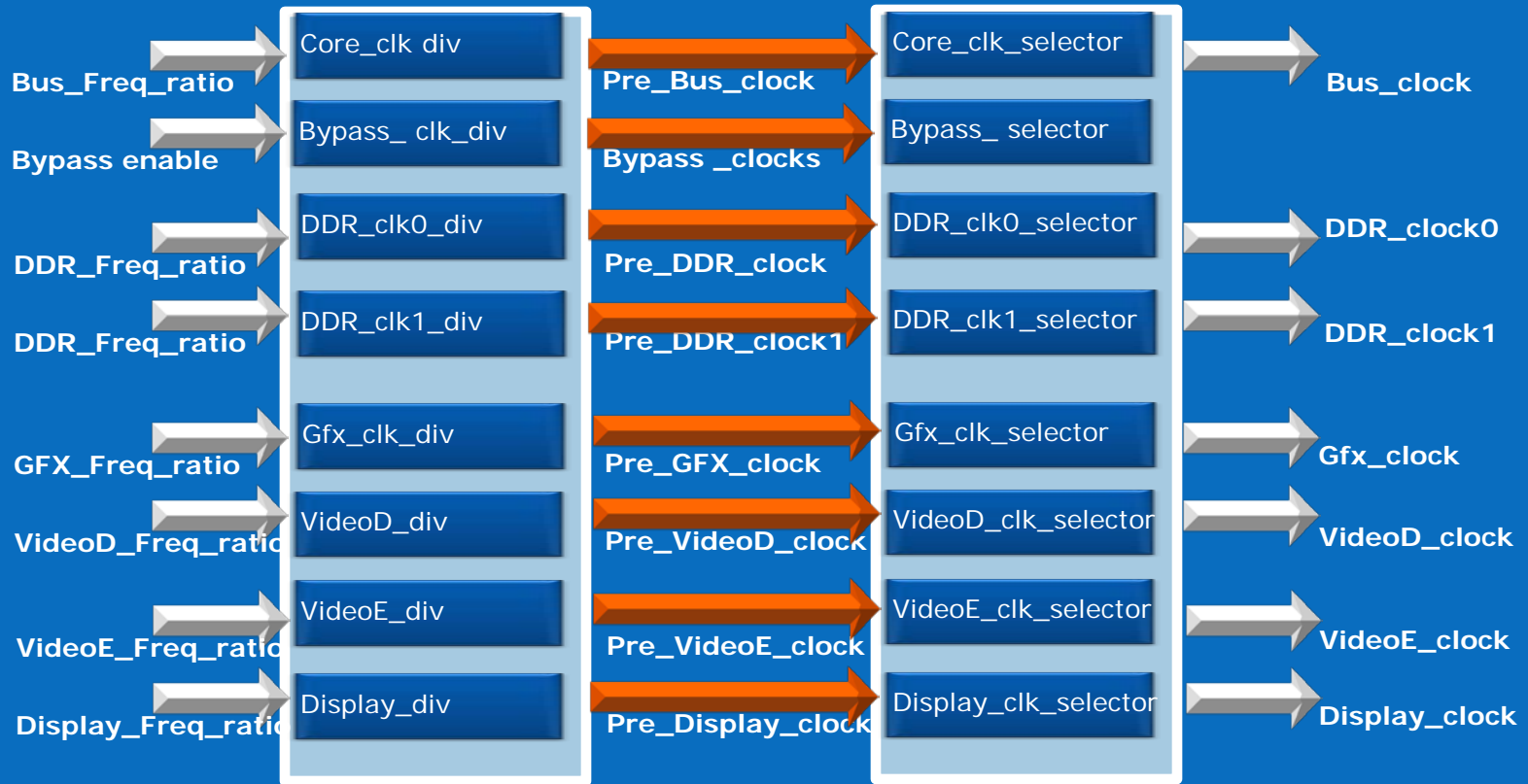
Significant Advancement on all Key Vectors

* Moorestown Platform Idle power reduction (based on current platform features) compared to Menlow Platform

Lincroft High Performance Innovation

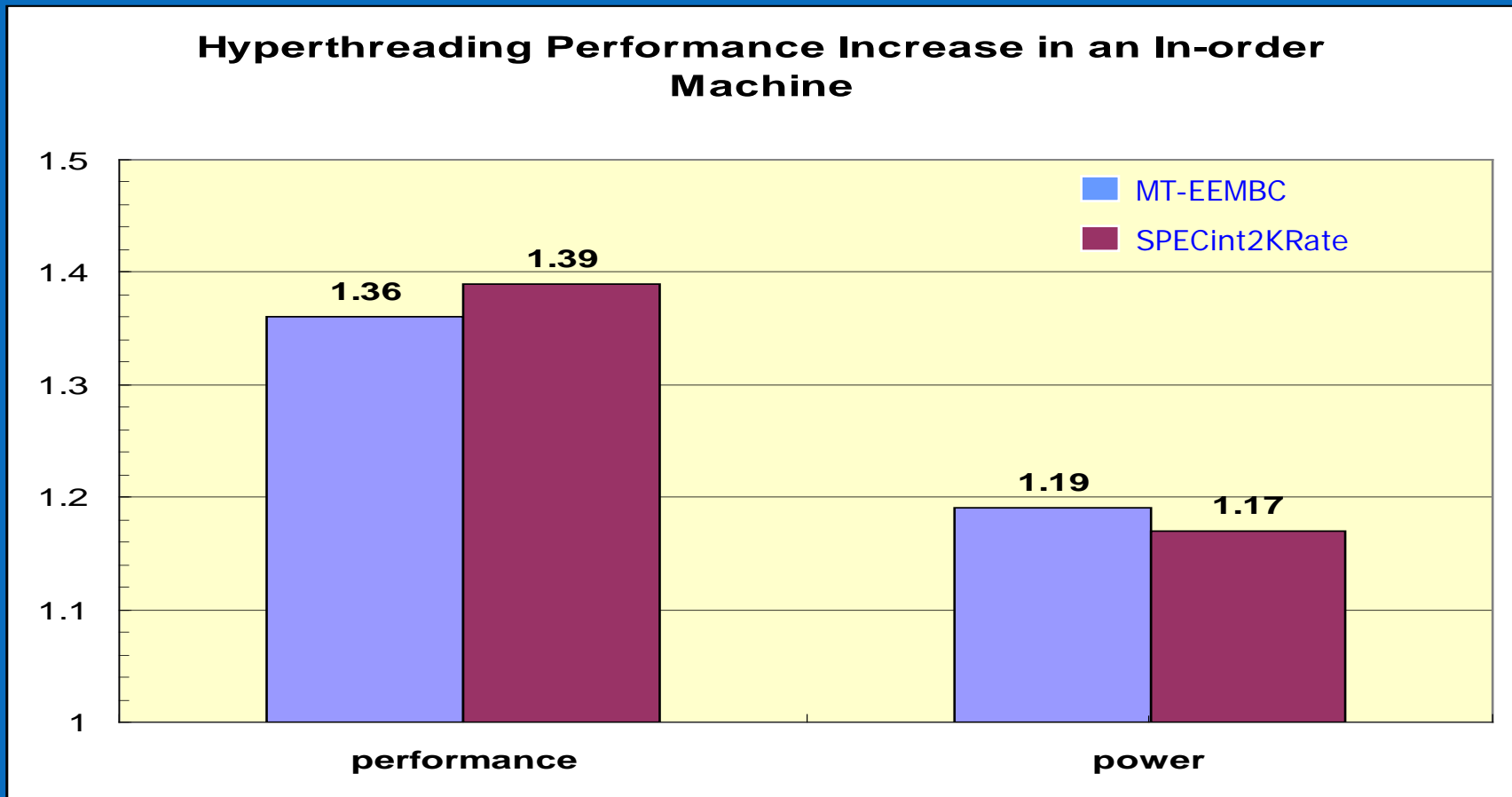
- Wide range of scalable frequencies for multimedia blocks
- Intel Hyper threading technology
- Bus Turbo Technology
- Burst Mode technology

Large Range of Scalable Frequencies for Multimedia Engines



Scalability enables Lincroft SoC into wide spectrum of FFs

Intel Hyper-threading Technology



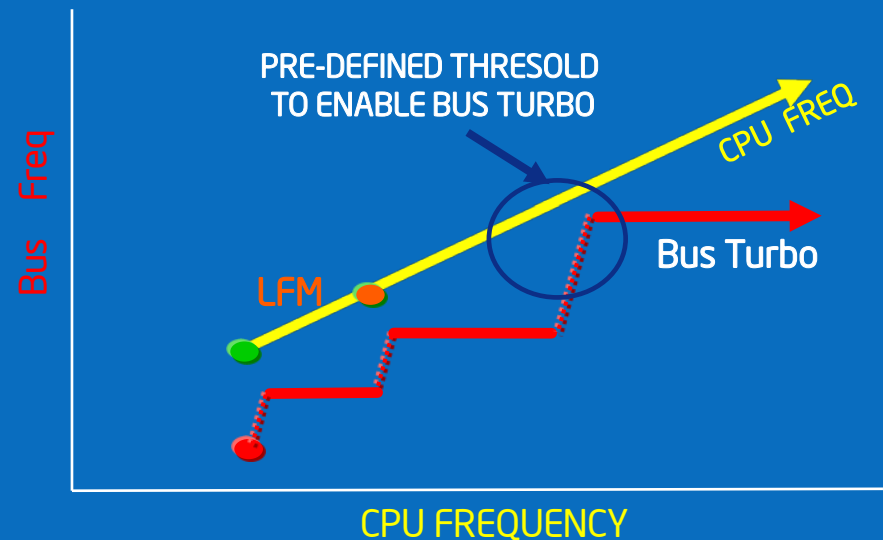
Hyper-threading technology provides excellent Performance/Power efficiency

Source* : Intel Testing, Specint2k and EEMBC run in Single Threaded / Hyper Threaded Mode on Linux. For Performance the score for each binary is calculated based on the runtimes; For Power, the effective capacitance or C-dyn is measured per binary on each of the benchmark while running in ST and HT modes. The difference in C-dyn and thus total power difference is calculated for ST and HT modes. Performance tests and ratings are measured using specific computer systems and/or components and reflect the approximate performance of Intel products as measured by those tests. Any difference in system hardware or software design or configuration may affect actual performance. Buyers should consult other sources of information to evaluate the performance of systems or components they are considering purchasing. For more information on performance tests and on the performance of Intel products, visit Intel Performance Benchmark Limitations

“Bus Turbo Mode” -- Further Performance Boost

- Motivation
 - To reduce memory latency and increase bus BW when CPU bursting at higher frequencies

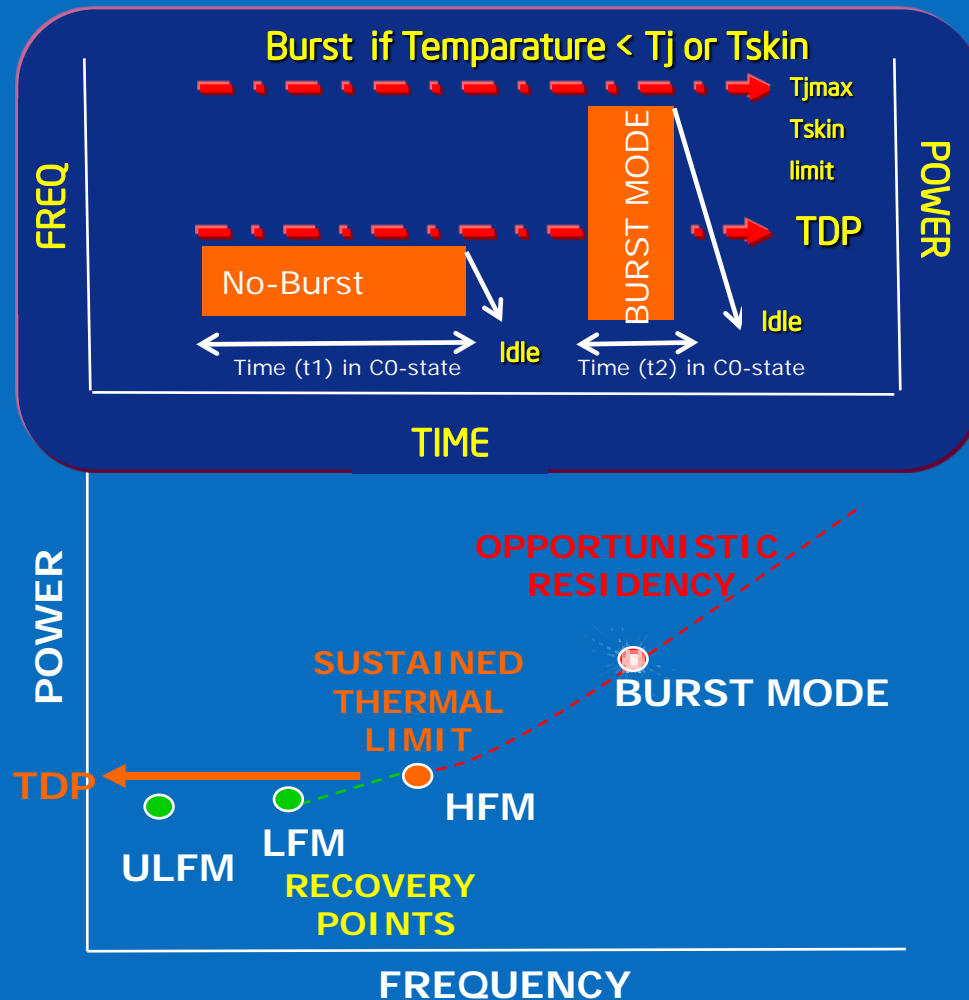
- Implementation
 - HW dynamically increases BUS frequency at pre-set CPU frequency
 - No need to re-lock PLL that provides clock to bus
 - Uses clock divider



“Bus Turbo Mode” substantially reduces memory latency and provides higher bus BW

Burst Mode -- Addl Performance Headroom

- Taking advantage of Thermal headroom on T_j and T_{skin} by increasing CPU frequency for short duration
- When T_j and T_{skin} limits are violated, System throttles to Recovery points
- Optimizes consumed energy
 - Energy(WHr) = Power x time
 - Race to idle
 - Saves energy if
 - $t_2/t_1 < p_1/p_2$



Burst mode provides on-demand performance without impacting thermal design

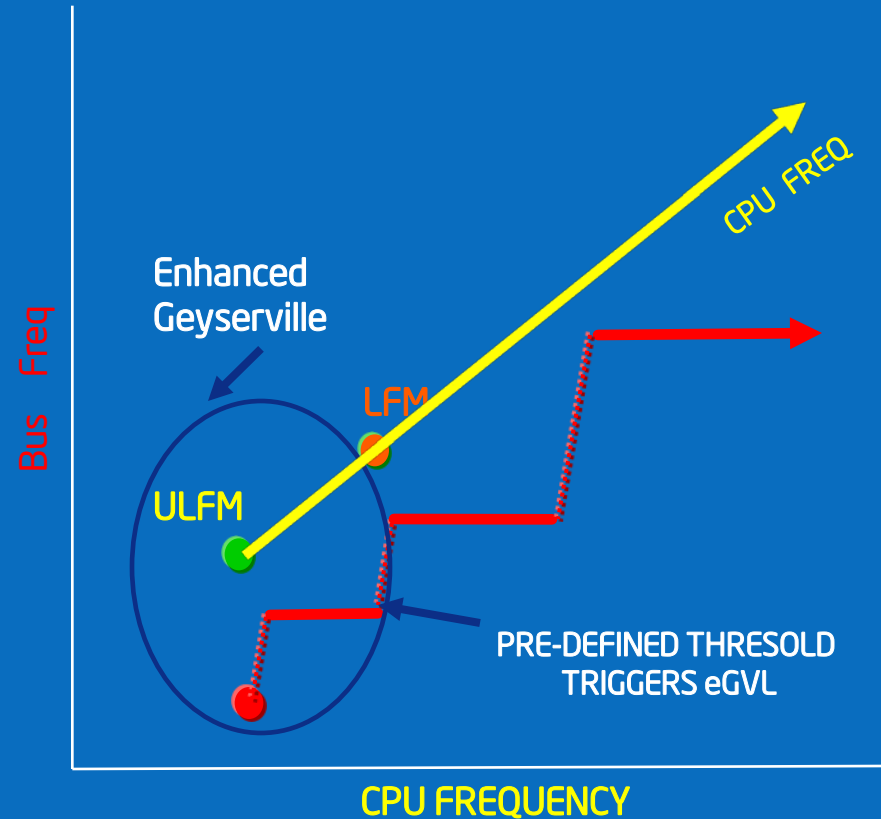
Lincroft Low Power Innovations

- Low power architecture features
 - MIPI-DSI
 - LP-DDR1
 - HW accelerators for Video Decode/Encode
- Enhanced Geyserville to support ULFM
- Lincroft CPU Power C-states
- Lincroft Distributed Power Gating

Enhanced Geyserville (eGVL)

- Motivation
 - To provide lowest possible CPU frequency
 - To enable “As many P-states as possible” below LFM at V_{min}
 - Linear savings of average power when CPU is not doing anything useful while in C0 state (cV^2F)

- Implementation
 - Added P-states below LFM at V_{min}
 - OS can now request CPU to transition to these new P-states



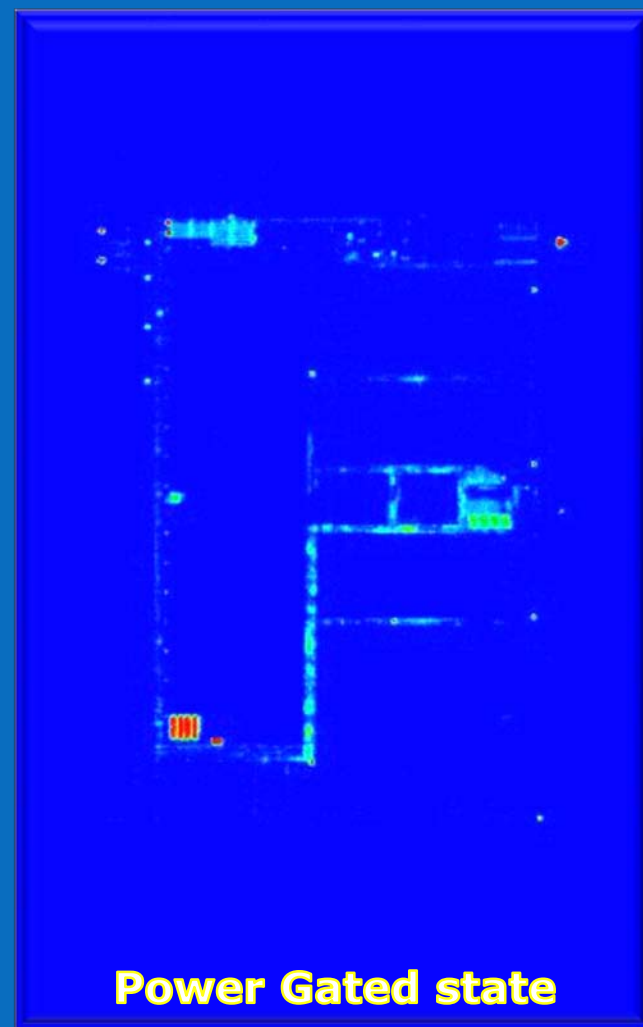
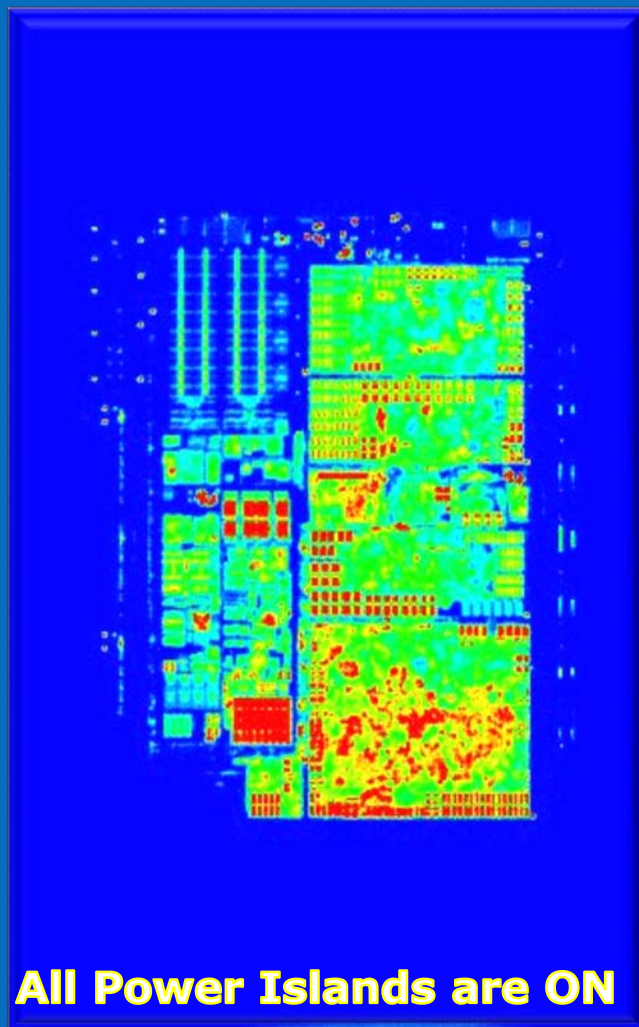
eGVL mode provides additional range of low power operating point

Lincroft CPU Power C-states

| | C0 HFM | C0 LFM | C0 ULFM | C1/C2 | C4 | C6 |
|--------------|--------|--------|---------|-------|-----|-----|
| Core voltage | | | | | | |
| Core clock | | | | OFF | OFF | OFF |
| PLL | | | | | OFF | OFF |
| L1 caches | | | | | | |
| L2 caches | | | | | | |
| Wakeup time | active | active | active | | | |
| Power | | | | | | |

Lincroft SoC: IREM image of Full ON vs. Power Gated

- Multiple Physical power Islands
- Distributed power gating to enable fine grain power management
- SW interface for Active Island power management
- HW managed sequencing of power ON and OFF



Aggressive Distributed Power Gating enables up-to 50x reduction in idle power*

* Moorestown Platform Idle power reduction (based on current platform features) compared to Menlow Platform

Summary

- Moorestown: Based on Lincroft SoC, Designed for
 - High Performance for amazing Internet Experience
 - Dramatically Lower Power – Upto 50x lower idle power
 - Small Size for Next Generation Smartphones

- Lincroft High Performance Innovation
 - Wide range of scalable frequencies for multimedia blocks
 - Intel Hyper threading technology
 - Bus Turbo Technology
 - Burst Mode technology
 - Intel 45nm SoC High-K process technology

- Lincroft Low Power Innovation
 - Low power architecture features
 - Enhanced Geyserville to support ULFM
 - CPU C-states
 - Lincroft Distributed Power Gating

Thank you

**Lincroft SoC, Langwell
and Moorestown
platform team**