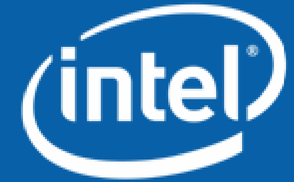


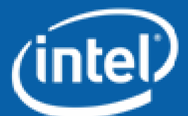
Getting the Lead Out

December, 2007

Tom DeBonis
Assembly & Test Technology Development
Technology and Manufacturing Group

Summary

- Intel has removed the lead (Pb) from its manufacturing process across its entire portfolio of packages in its 45nm family of microprocessors*
  - … 65nm chipsets will transition to lead-free manufacturing process in 2008
- Intel's 45nm Hi-k metal gate process technology represents a dramatic transition to new materials that enable energy efficient performance microprocessors
- Intel's family of 45nm microprocessors will begin production in second half of 2007
- Intel's effort to eliminate lead in our products is part of broader strategy to support an environmentally sustainable future



*45nm product is manufactured on a Lead Free process. Lead-free per EU RoHS directive July, 2006 (2002/95/EC, Annex A). Some EU RoHS exemptions may apply to other components used in the product package.

Agenda

- Background
  - Intel's Commitment to the Environment
  - Intel's Progression toward Lead-free
  - Where is the lead and where it's being removed
- Transition to Lead-free Flip Chip Process
- Summary
- Questions

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Intel's Commitment to the Environment

- Intel has a long history of commitment to the environment
- This philosophy guides our product design, our manufacturing operations, our innovative technology, and our public policies
- It makes good business sense
  - We have a philosophy of doing what's right
  - Often exceeding regulatory requirements

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Reduced Environmental Footprint

Recent Successes

- Launched Intel® Core™2 Duo processors: for desktops up to 40% faster and 40% more energy efficient
- Transitioned Intel® StrataFlash® Cellular Memory packages to halogen-free technology.
- Saved over 9 billion gallons of fresh water through our water reuse and recycling practices
- Recycled more than 70% of our chemical and solid wastes
- Reduced our global warming gas emissions the equivalent of removing 50,000 cars from the road
- Named Technology Super Sector Leader by Dow Jones Sustainability Index for the 6th year running

Intel 2006 Corporate Social Responsibility report recently posted online
http://www.intel.com/intel/cr/gcr06/overview.htm

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Intel Lead-free Technology Progression

Packages and Complexity

Done!

Done!

Done!

180nm wire bond Chip-scale

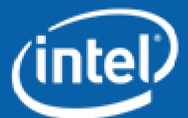
130nm Wire bond Lead-frame & BGA

90nm Flip-Chip 95% Lead-Free

45nm Flip-Chip Lead-Free Process*

2001 / 2002 | 2003 | 2004 | 2005 | 2006 | 2007

Intel has been reducing lead in its products for several years… 45nm is the final milestone



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The Long Road to Lead-Free

- Lead has been used in electronics for several decades to form the electrical and mechanical connections between chip, package, and system circuitry

- Finding suitable replacements has been a technical challenge for the entire industry

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Eliminating the Pb in Intel Components

Flip-Chip Pin Grid Array (FC-PGA)

Flip-Chip Bump
Lead
^RoHS Exempt

Caps/Resistors**
Lead

Pin Grid
Lead

socket

Printed Circuit Board

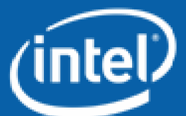
Flip-Chip Ball Grid Array (FC-BGA)

Flip-Chip Bump
Lead
^RoHS Exempt

Caps/Resistors**
Lead

Solder Balls
Lead

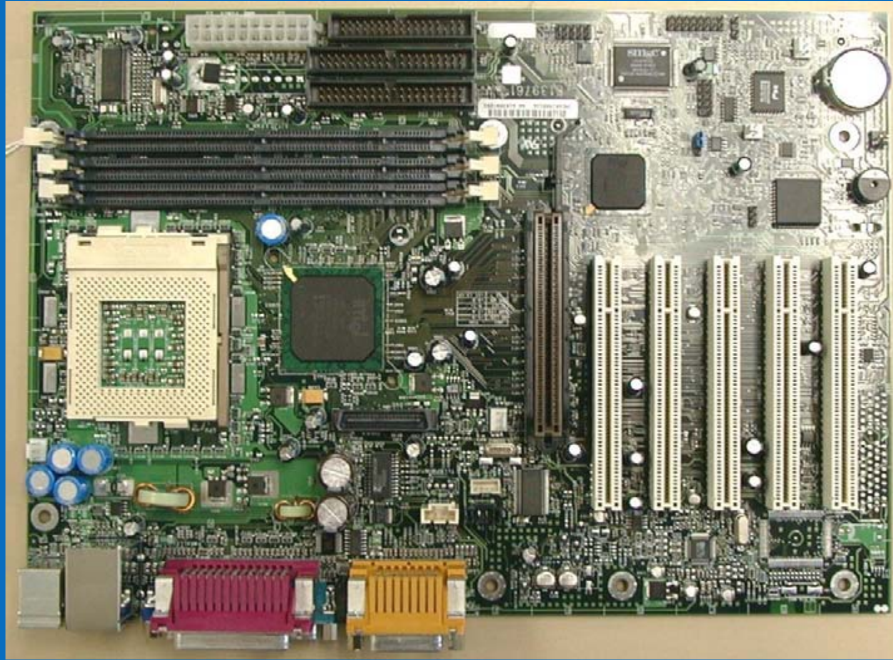
***95% of the Lead Content Removed from Flip-chip Packages in 2004**



*Percentage based on weight ** Some RoHS exemptions may apply to other components used in the product package

Preparing the Industry for the Lead-free Transition

PC Platform Example



Industry Complexity:

- Huge number of components (chipsets, sockets, passives, connectors, & many more)
- Simultaneous availability of Lead-free components
- Compatibility/Reliability of Lead-free components at higher temperatures
- Board process manufacturability at higher temperatures

- **In 2004 Intel developed an enabling program to prepare industry**
  - **Industry consortia, suppliers, and manufacturing service providers to develop manufacturing processes, set standards and educate the industry**

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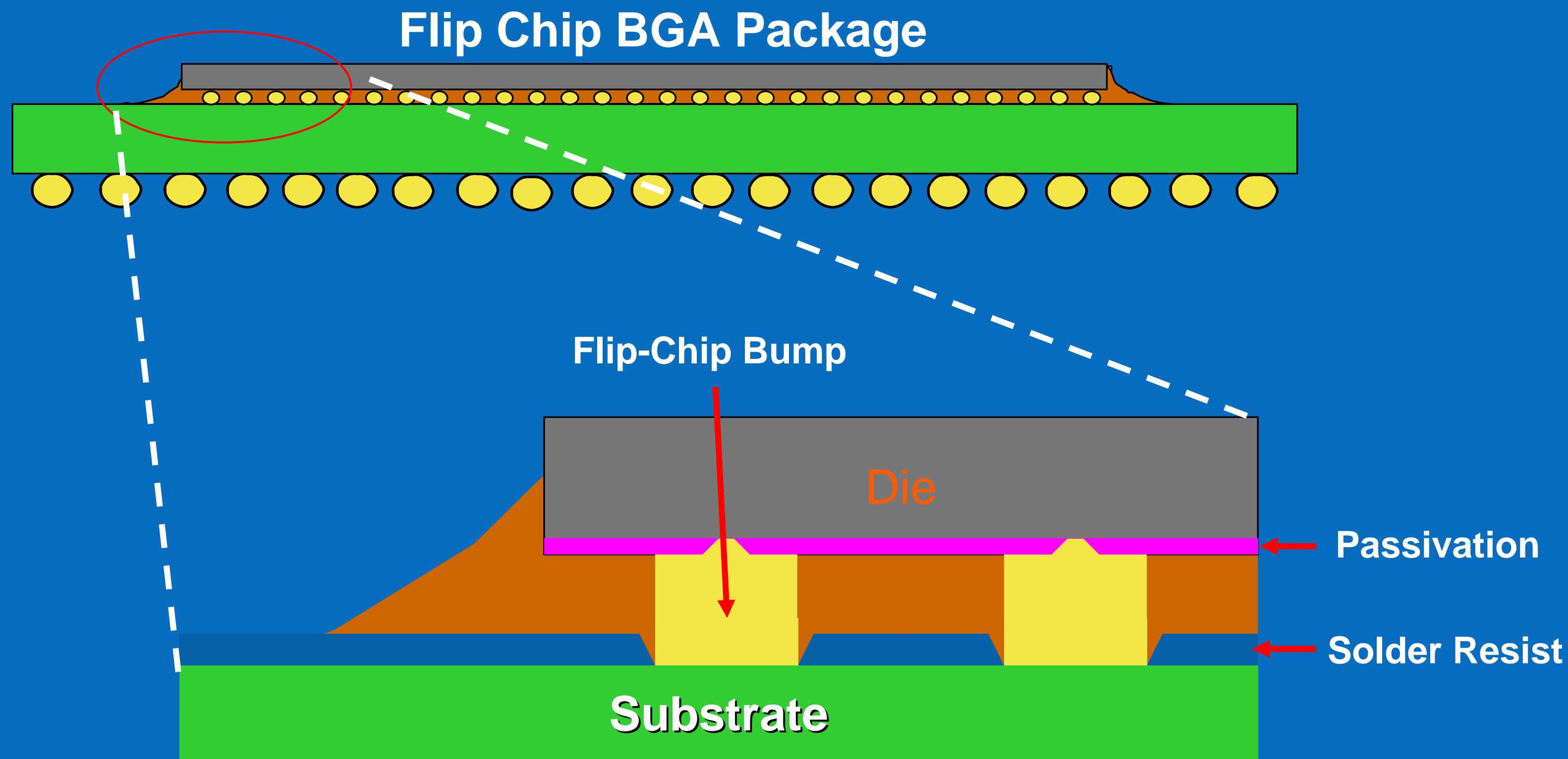
Lead-Free Flip-Chip Package Technology Challenges



Many challenges had to be overcome to remove the remaining 5% of Lead (Pb) in the First Level Interconnect

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Lead-Free Solder Properties Affect Low-K Inter Layer Dielectric

At reflow temperature

Silicon Die
CTE* 2.8 ppm/ºC

Flip Chip Bump

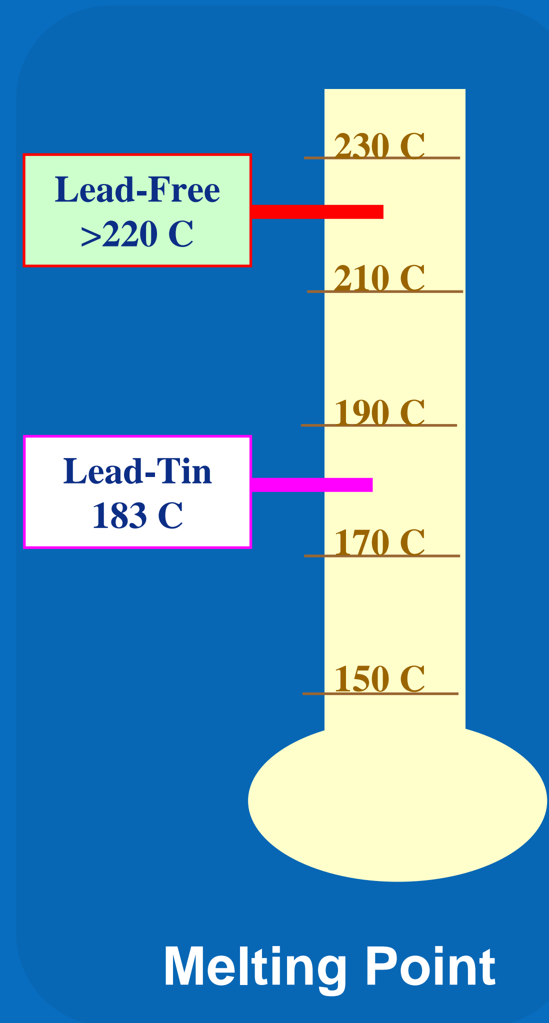
Package
CTE* 17 ppm/ºC
(Copper Laminate)

Cooling

Heating

At room temperature

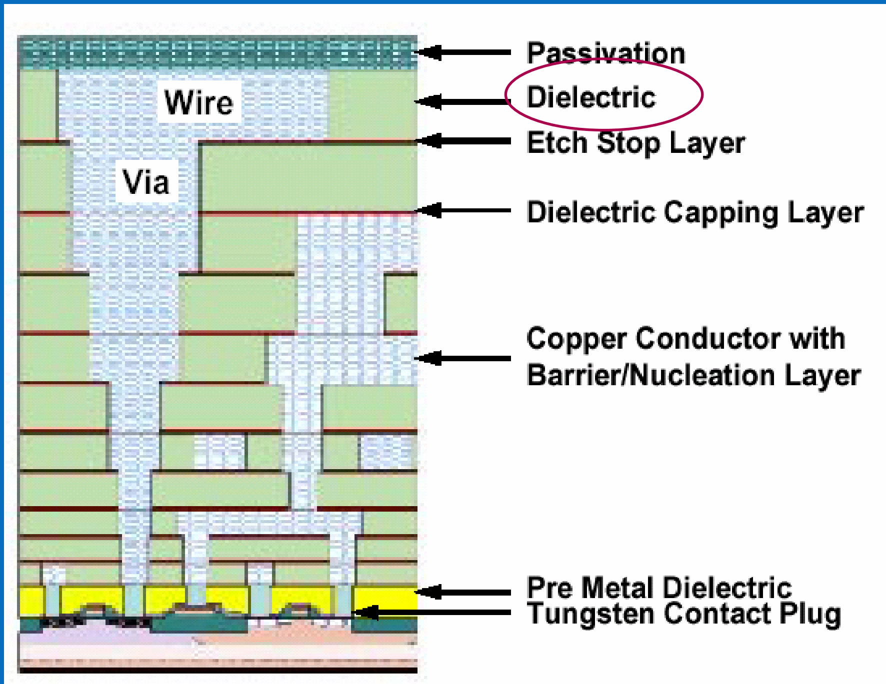
The Package shrinks more than the chip



Lead-free solder increases stress

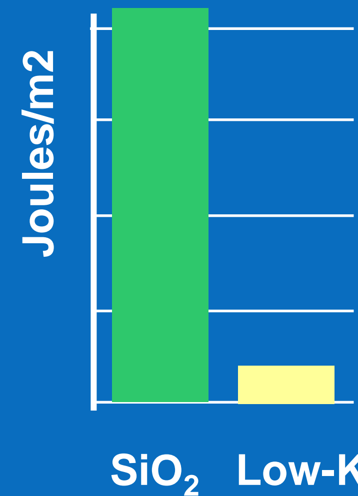
* CTE = Coefficient of Thermal Expansion *PPM= Parts Per Million

Low-K Silicon & Lead-free Package Integration Challenge



example silicon cross-section

ILD Strength

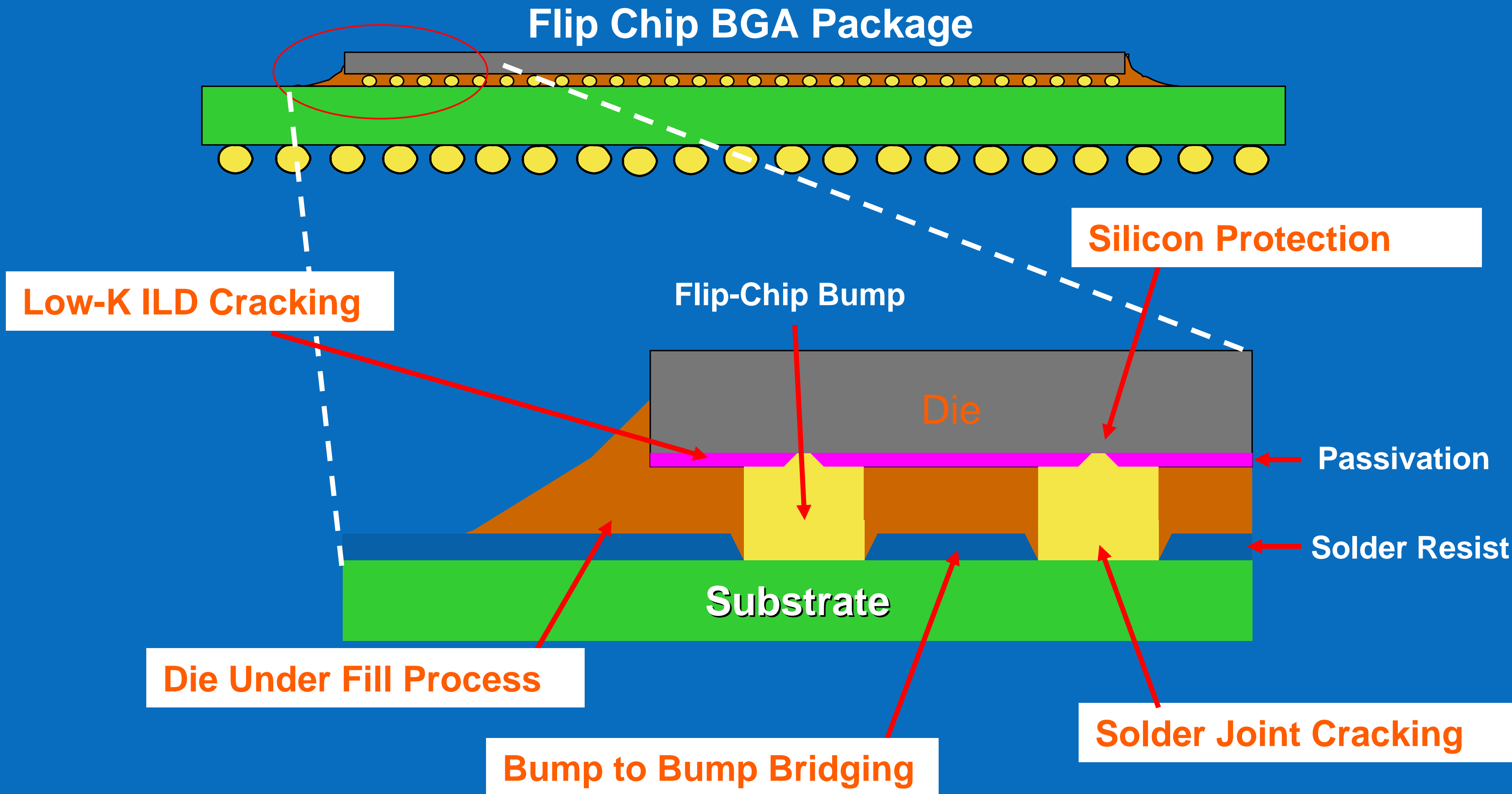


Successful Integration of Silicon & Lead-Free Flip Chip Package Technologies requires a significant reduction in Inter Layer Dielectric (ILD) Stress

SiO_2= Silicon Dioxide

K = “dielectric constant” which measures the relative permittivity of a material.

Pb-free Flip-Chip Package Technology Challenges



Many Challenges had to be overcome to remove the remaining 5% of Lead (Pb) in the First Level Interconnect

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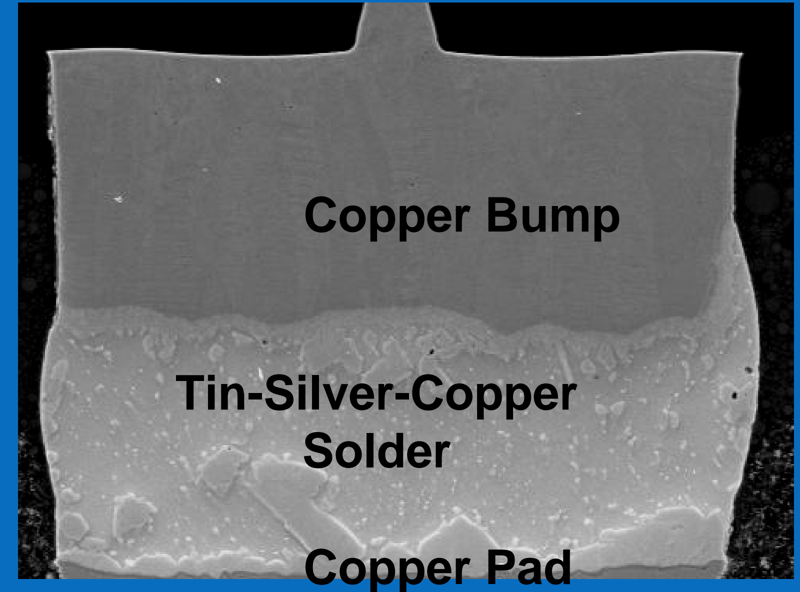
Introducing Intel's 45nm Lead-Free Flip Chip Technology

Traditional High-Lead Bumps

Lead-free Advanced Bump Metallurgy



Solders containing lead have been replaced with a copper column and lead-free solder

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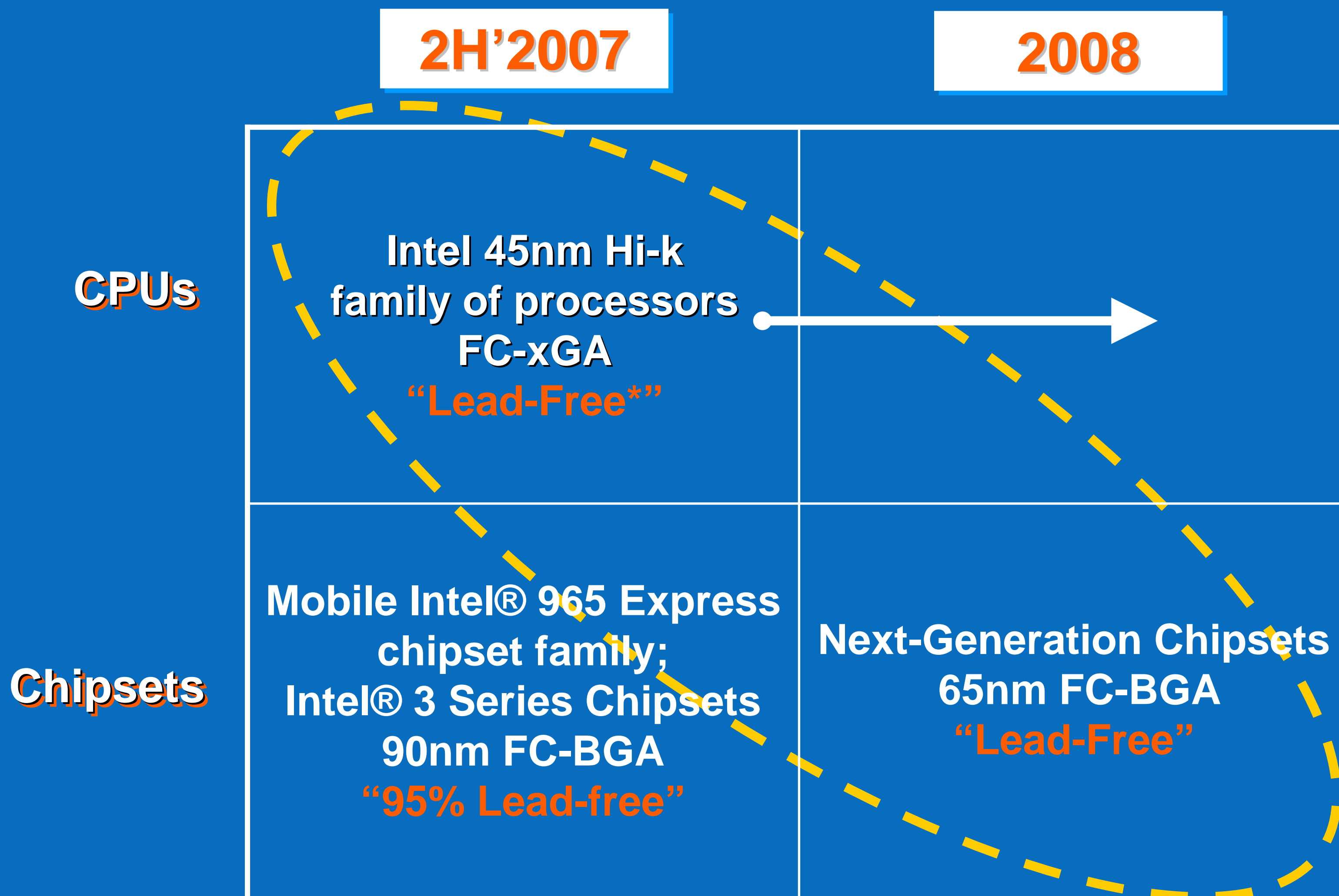
Transition to Lead-Free Flip-Chip Technology



Note: All products, dates, and figures are preliminary, for planning purposes only, and subject to change without notice

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For further information on Intel's lead free technology, please visit

www.intel.com/technology/silicon

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Definitions

- Lead Free / Pb Free:
  - Lead free 45nm manufacturing process. Lead free per EU RoHS directive (2002/95/EC, Annex A)
  - Does not require exemption for Lead (Pb) in die/package First Level Interconnect (FLI)
  - Some RoHS exemptions may apply to other components used in the product package

- RoHS Compliant: Complies with the RoHS directive because either:
  1) its Lead Free and meets the RoHS material content thresholds or
  2) a RoHS exemption applies (e.g. flip chip exemption)

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45 nm Technology Benefits

45 nm benefits compared to 65 nm

~2x improvement in transistor density, for either smaller chip size or increased transistor count

~30% reduction in transistor switching power

>20% improvement in transistor switching speed or
>5x reduction in source-drain leakage power

>10x reduction in gate oxide leakage power

These performance and leakage improvements would not be possible without high-k + metal gate