Reducing Variation in Advanced Logic Technologies:

Approaches to Process and Design for Manufacturability of Nanoscale CMOS

Kelin J. Kuhn
Intel Fellow
Director of Logic Device Technology
Portland Technology Development
Intel Corporation

Key messages

- Process variation is not a new problem
- A variety of process, design and layout techniques can be applied to mitigate the impact of random and systematic variation
- Improvements in variation in 45nm illustrate that variation does not pose an insurmountable barrier to Moore's Law, but is simply another challenge to be overcome

History

Process variation

Not a new problem

THRESHOLD-VOLTAGE SENSITIVITY OF ION-IMPLANTED M.O.S. TRANSISTORS DUE TO PROCESS VARIATIONS

Indexing terms: Field-effect transistors, Ion implantation

Adjustment of the threshold voltage V_T by ion implantation yields a certain distribution of threshold voltages determined by different process parameters. A procedure is presented for minimising the threshold-voltage sensitivity of implanted m.o.s. transistors due to these parameters for a typical set of process parameters.

The threshold-voltage shift ΔV_T due to ion implantation depends, among other parameters, on the depth of penetration of the ions into the semiconductor.[1] The depth of penetration is related to the implantation energ
t_{ox}. The standard m.o.s. process n
deviation of $\pm 10\%$ for t_{ox}. Uncer
energy may be of interest, too.

To introduce the problem, consic
lower oxide thickness. This has tw

(*a*) For a given implantation ener
within the semiconductor, Q_{eff},
thickness decreases. This tends to in

(*b*) Simultaneously, the oxide capa
has the opposite effect of decreasing

For a large oxide thickness, the fir
a small t_{ox}, when practically all t
into the semiconductor, i.e. variati
Q_{eff}, the second effect dominates
of a certain t_{ox}, the threshold shift Δ
of t_{ox}.

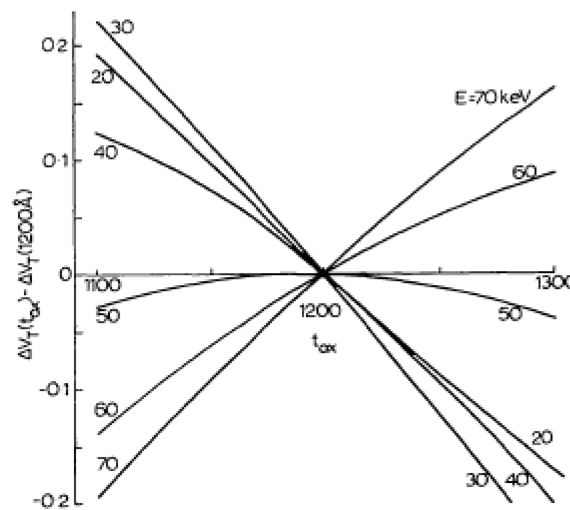


Fig. 1 *Threshold shift ΔV_T (t_{ox}) as function of oxide thickness t_{ox} for different implantation energies*
Dose = $1 \cdot 07 \times 10^{12}$ cm^{-2}

1974:

W. Schemmert, G. Zimmer, *Threshold-voltage sensitivity of ion-implanted m.o.s. transistors due to process variations,* Electronics Letters, Volume 10, Issue 9, May 2 1974 Page(s):151 - 152

Concerns about threshold voltage variation are not new!

Process variation

Not a new problem

CASTAM: A Process Variation Analysis Simulator for MOS LSI's

YUKIO AOKI, TORU TOYABE, MEMBER, IEEE, SHOJIRO ASAI, MEMBER, IEEE, AND TAKAAKI HAGIWARA

Abstract—A simulator named CASTAM, which includes both process and device models, has been developed to predict MOS process variations through the analysis of variations in electrical characteristics of fabricated MOS devices using the Monte Carlo method.

Analysis accuracy using the simulator is examined. Investigation shows that process parameter variations can be estimated with an error of less than 10 percent if an appropriate set of device characteristic items is chosen.

Wafer inspection data for a CMOS pilot line can be analyzed with this simulator, and the main cause of threshold voltage variation pinpointed. Predictions derived from the analyzed results have been confirmed using experimental data. This shows that analysis using CASTAM is sufficiently reliable.

the main cause of variation in device characteristics. It is, however, hard to directly measure variations in process parameters. In 1964, D. P. Kennedy *et al.* [1] proposed a method by which variations in process parameters could be estimated from measured variations in device characteristics, and they applied this method to bipolar transistors. Recently W. May *et al.* [2] have reported on almost the same method, and they also analyzed variations in bipolar transistors.

The purpose of the work being reported on here has been to develop CASTAM, a Computer Aided STAtistical Modeling simulator. This program was first applied to MOS devices [3], being different from the above literature.

Attempts to model variation are not new!

1984:

Y. Aoki, T. Toyabe, S. Asai, T. Hagiwara, *CASTAM: A process variation analysis simulator for MOS LSI's*, IEEE Transactions on Electron Devices, Volume 31, Issue 10, Oct 1984 Page(s):1462 - 1467

Process variation

Not a new problem

Circuit Sensitivity to Interconnect Variation

Zhihao Lin, *Member, IEEE,* Costas J. Spanos, *Senior Member, IEEE,* Linda S. Milor, *Member, IEEE,* and Y. T. Lin

***Abstract*—Deep submicron technology makes interconnect one of the main factors determining the circuit performance. Previous work shows that interconnect parameters exhibit a significant amount of spatial variation. In this work, we develop approaches to study the influence of the interconnect variation on circuit performance and to evaluate the circuit sensitivity to interconnect parameters. First, an accurate interconnect modeling technique is presented, and an interconnect model library is developed. Then, we explore an approach using parameterized interconnect models to study circuit sensitivity via a ring oscillator circuit. Finally, we present an alternative approach using statistical experimental design techniques to study the sensitivity of a large and complicated circuit to interconnect variations.**

***Index Terms*—Circuit analysis, interconnect, statistical analysis, worst case design.**

I. INTRODUCTION

THE CONTINUOUSLY increasing scale of integration used in the design and processing of integrated circuits has drawn special attention toward interconnect effects. As the minimum feature size in VLSI systems drops to 0.25 μm and below, interconnect characteristics are becoming limiting factors on performance, since the time constant associated with interconnect is scaled by a smaller factor compared to those of devices. Future chip complexity and speed advances will depend on the ability to model the electrical behavior of interconnect in an accurate and efficient fashion.

A modeling framework to study the sensitivity of circuit performance to interconnect parameter variations will allow circuit designers to meet timing targets while taking into account the random and systematic source of interconnect parameter variations. It will also help the process designers to design new technologies while taking the sensitivity information into consideration. Finally, the sensitivity study results will help make the circuit more robust against the variation.

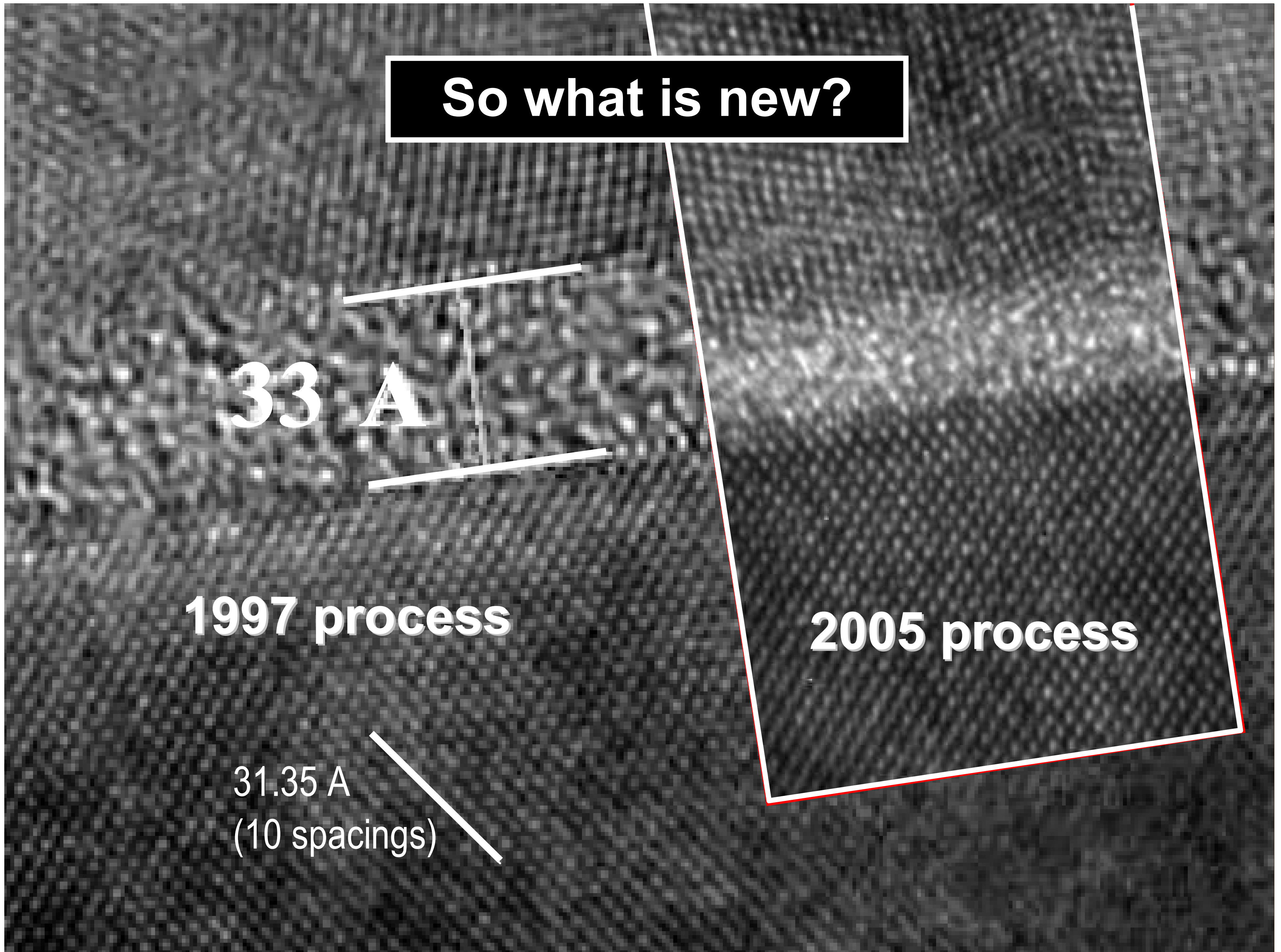
Overall, the goal of this paper is to address the problem of interconnect variations, look for a methodology to model interconnect wires, and develop approaches to quantify and investigate interconnect parameter variations on circuit performance under current and future technologies. The ultimate objective is to facilitate optimal circuit and process design, reduce time-to-yield, and improve the final yield.

Two approaches to study the circuit sensitivity to interconnect parameter variations are developed in this paper. The first approach is based on a parameterized interconnect model library. The parameterized interconnect models allow us to manipulate interconnect parameters, and to generate a circuit description that is suitable for performance sensitivity study. The second approach uses statistical experimental design techniques to analyze complicated circuits via simulation experiments. The first approach is illustrated with the help of a ring oscillator circuit, and the second approach is illustrated with a large multiplier circuit.

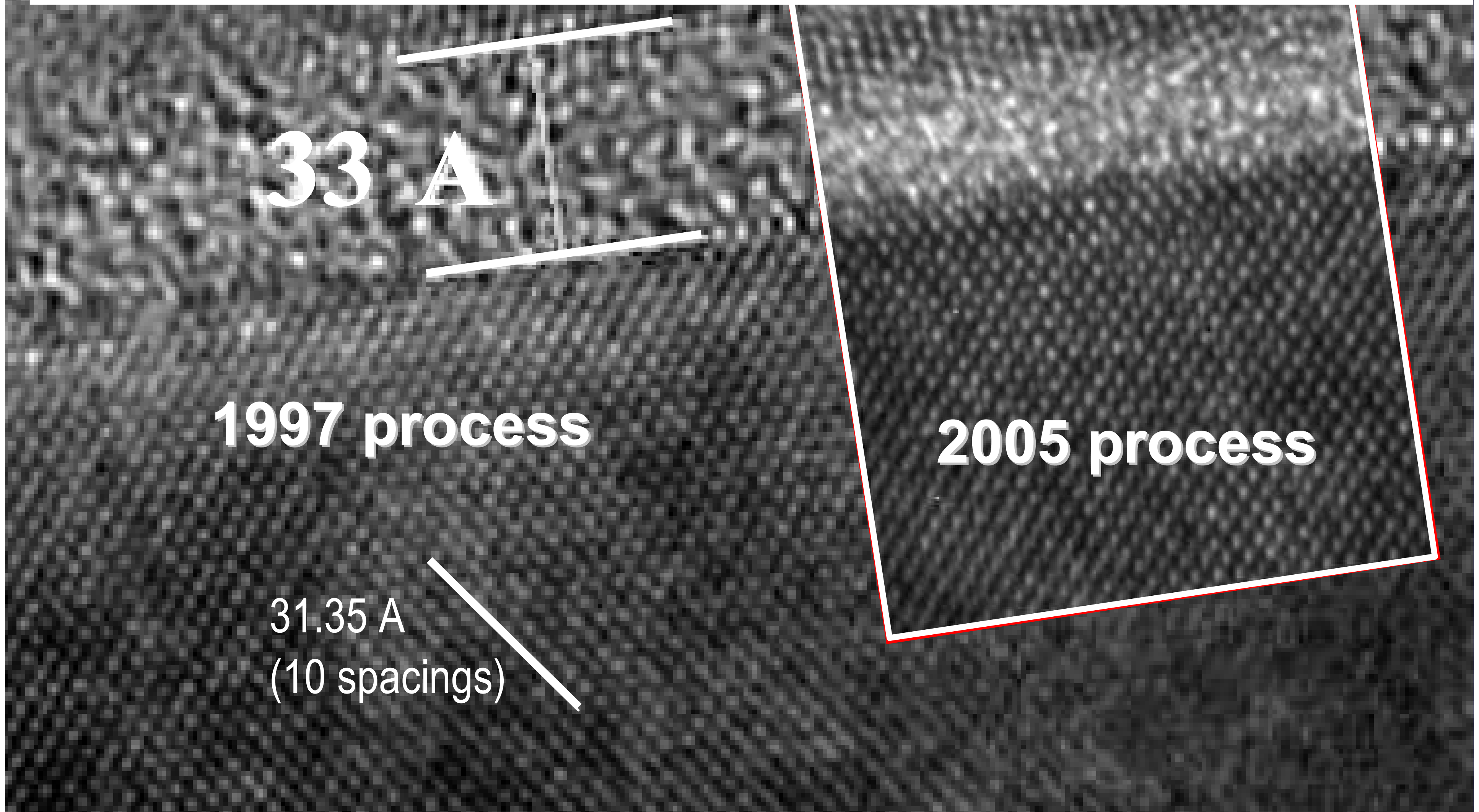
Concerns about interconnect variation are not new!

1998:

Z, Lin, C.J. Spanos, L.S. Milor, Y.T. Lin; *Circuit sensitivity to interconnect variation,* IEEE Transactions on Semiconductor Manufacturing, Volume 11, Issue 4, Nov. 1998 Page(s):557 - 568

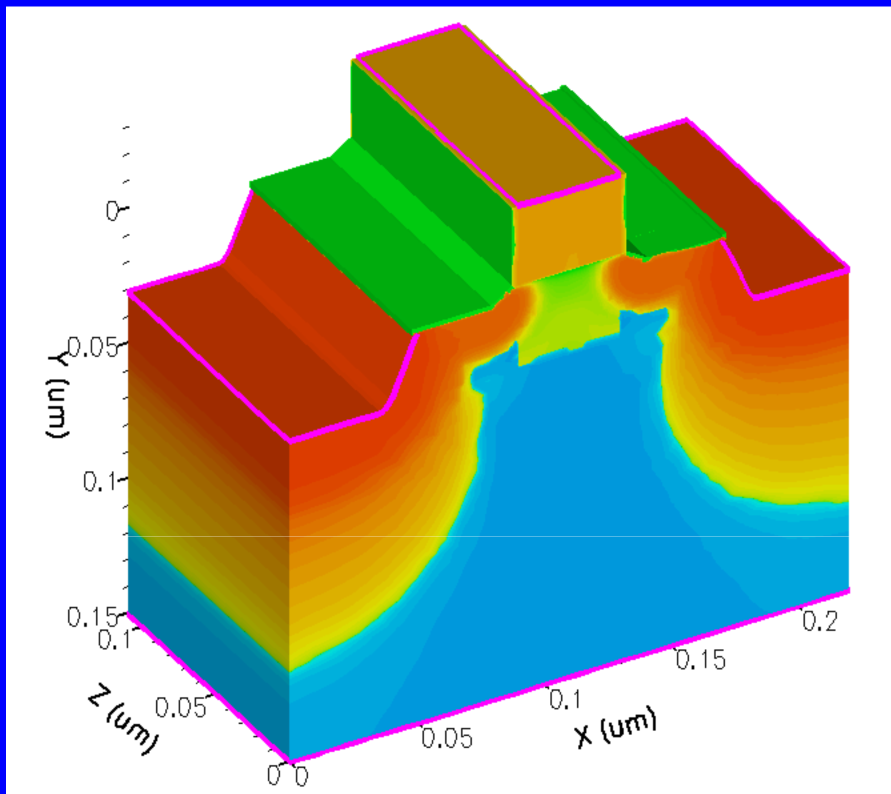

So what is new?
33 A
1997 process
2005 process
31.35 A
(10 spacings)

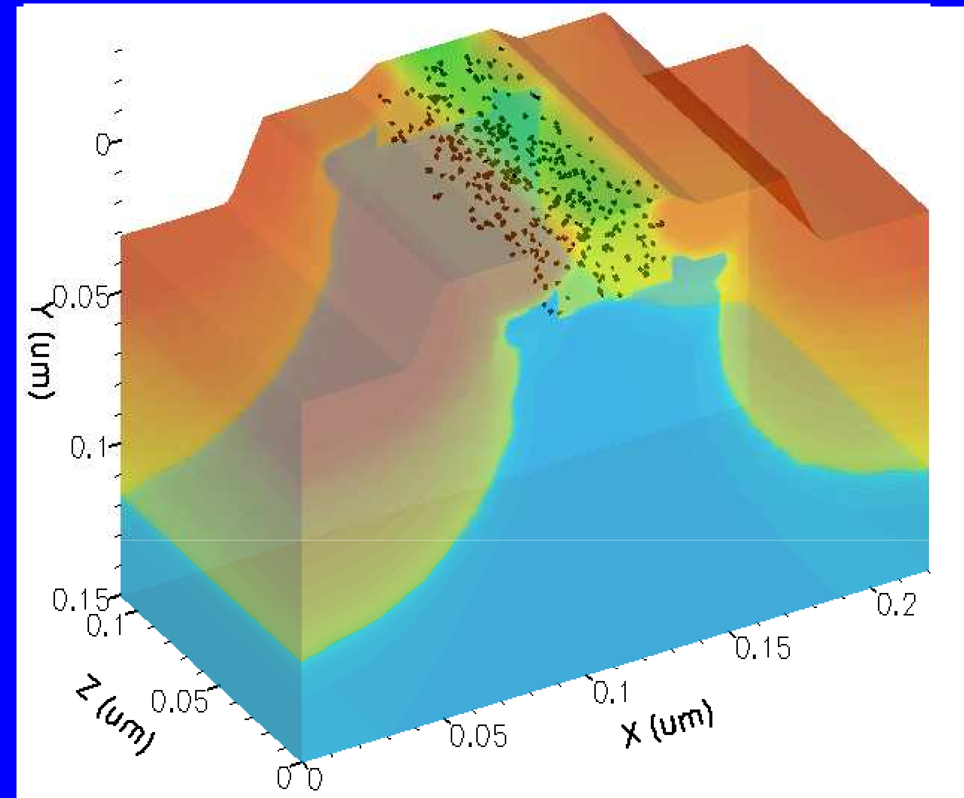
An increasing number of process elements possess feature sizes on the order of fundamental dimensions (such as atomic dimensions and light wavelengths)



Random Variation

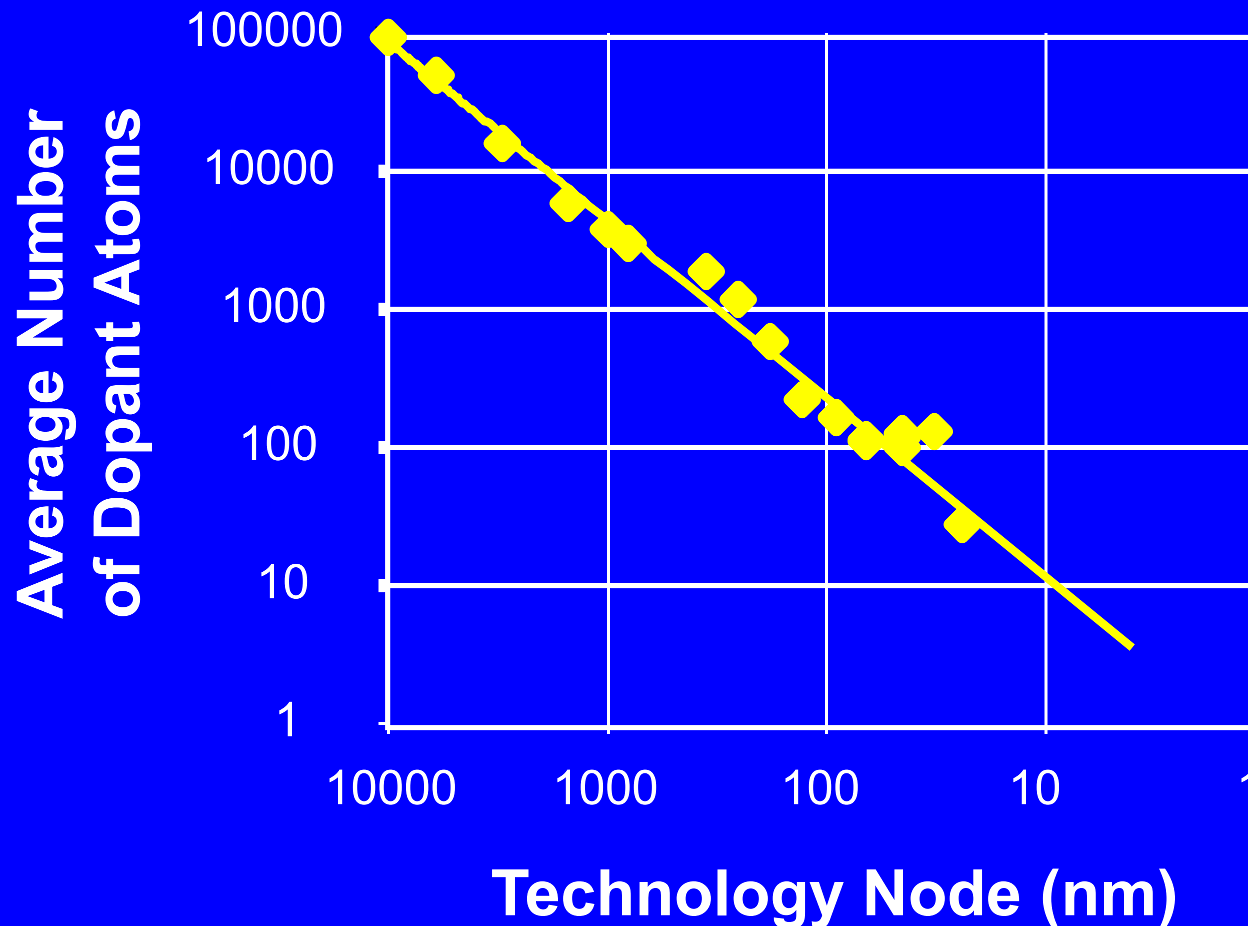
Random Dopant Fluctuations (RDF)

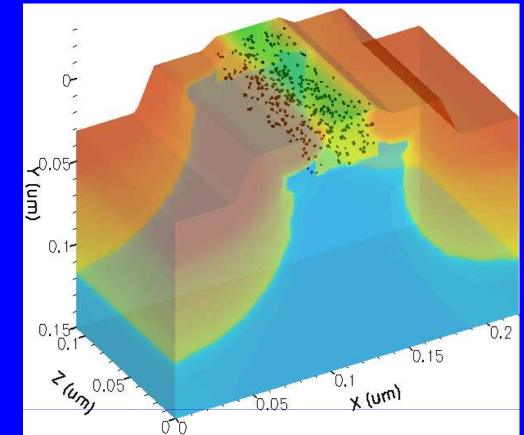




Decreased channel area means that
MOS threshold voltage variation due to random dopant fluctuations (RDF) is an increasingly significant effect

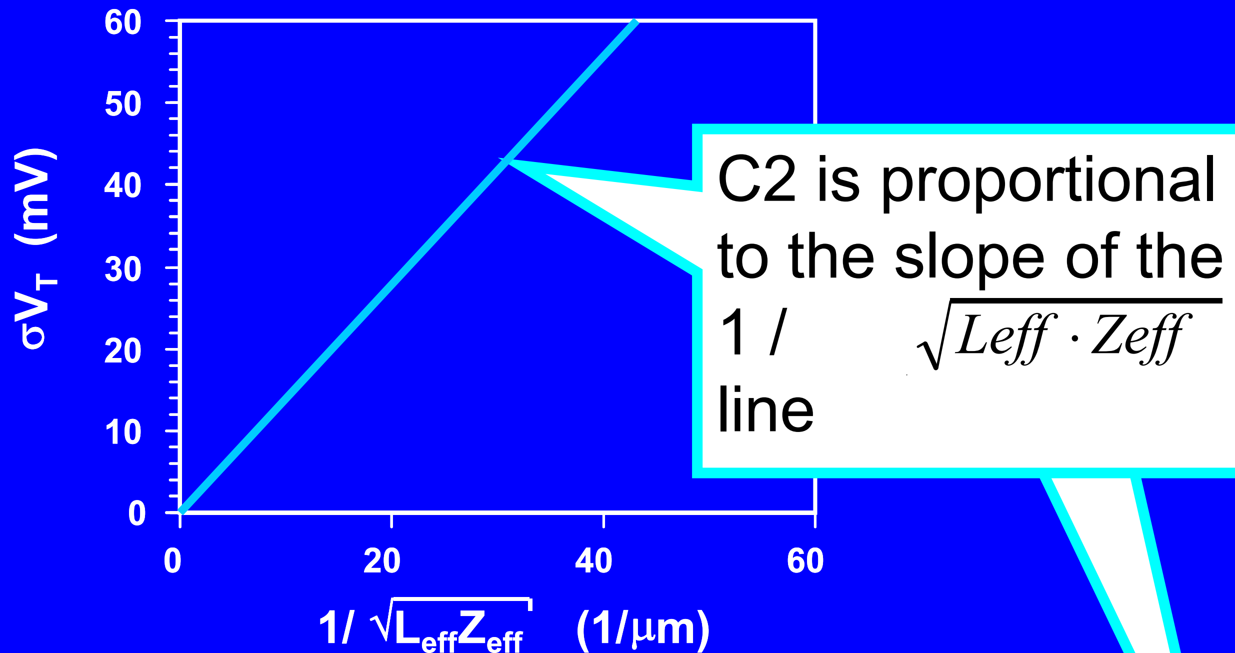
RDF: Driven by the decrease in the average number of dopant atoms/device per technology generation





[1] D. Frohman-Bentchkowsky et al., Fairchild, T-ED 1969
[2] F.H. Gaensslen et al., IBM, IEDM 1975
[3] J.J. Sanchez et al., Intel, T-ED 1989
[4] A.T. Wu et al., Intel, IEDM 1989

Characterizing RDF

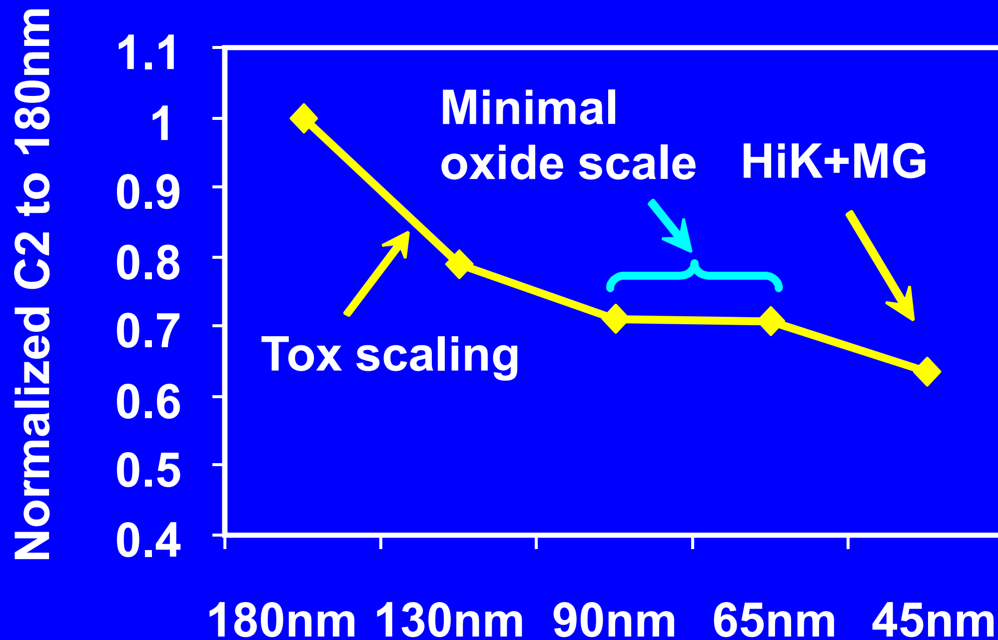


RDF is frequently described by (Stolk):

$$\sigma V_{Tran} = \left(\frac{\sqrt[4]{4q^3 \varepsilon_{si} \phi_B}}{2} \right) \cdot \frac{T_{ox}}{\varepsilon_{ox}} \cdot \left(\frac{\sqrt[4]{N}}{\sqrt{Leff \cdot Zeff}} \right) = \frac{1}{\sqrt{2}} \left(\frac{c_2}{\sqrt{Leff \cdot Zeff}} \right) \quad (1)$$

P. Stolk, F. Widdershoven, and D/ Klaassen, “Modeling statistical dopant fluctuations in MOS transistors” IEEE Trans. on Elec. Dev., 45:9, pp 1960-1971, Sept. 1998

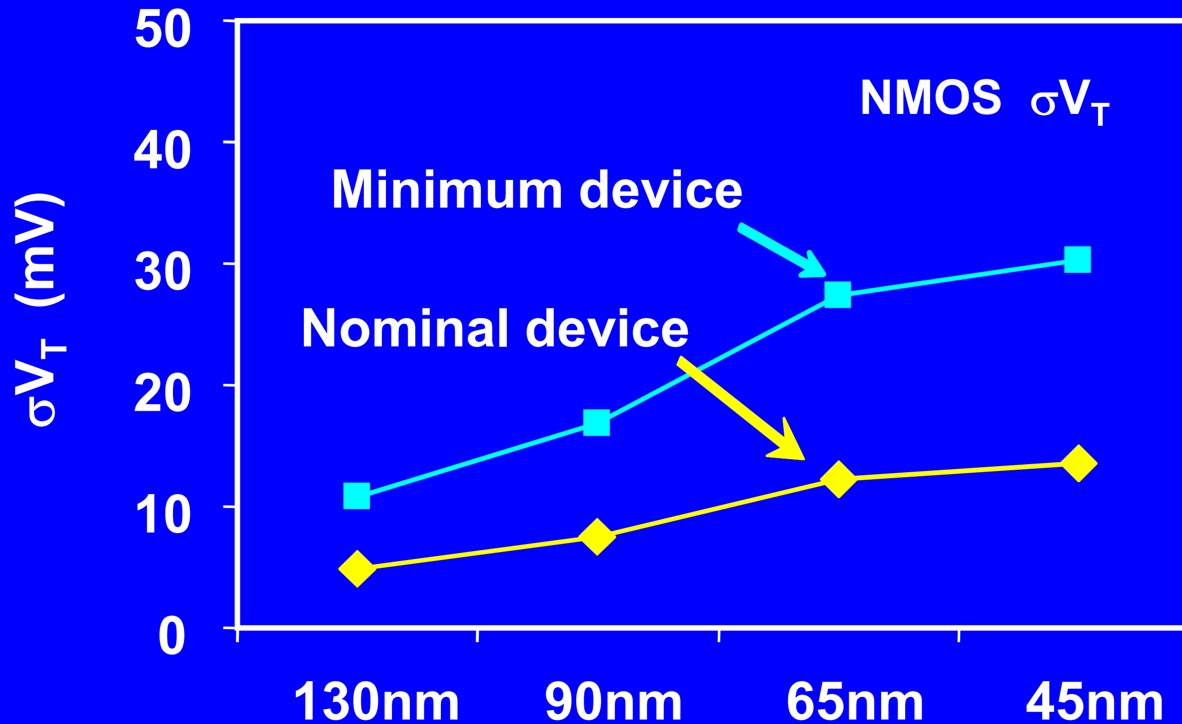
Scaling of C2



- **180nm to 90nm:** Improved with Tox scaling
- **90nm to 65nm:** No improvement, gate leakage concerns limited Tox scaling
- **65nm to 45nm:** Improved, HiK+MG enabled a return to a historical scaling trend

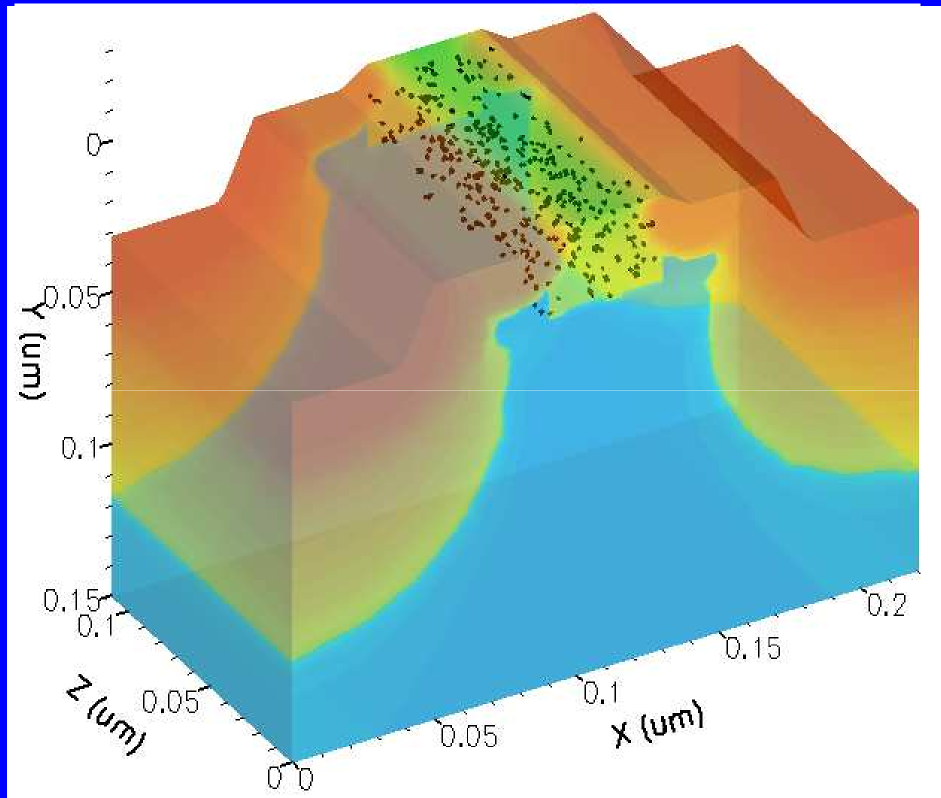
$$\sigma V_{Tran} = \left(\frac{\sqrt[4]{4q^3 \varepsilon_{si} \phi_B}}{2} \right) \cdot \frac{T_{ox}}{\varepsilon_{ox}} \cdot \left(\frac{\sqrt[4]{N}}{\sqrt{Leff \cdot Zeff}} \right) = \frac{1}{\sqrt{2}} \left(\frac{c_2}{\sqrt{Leff \cdot Zeff}} \right) \quad (1)$$

Scaling of σV_T



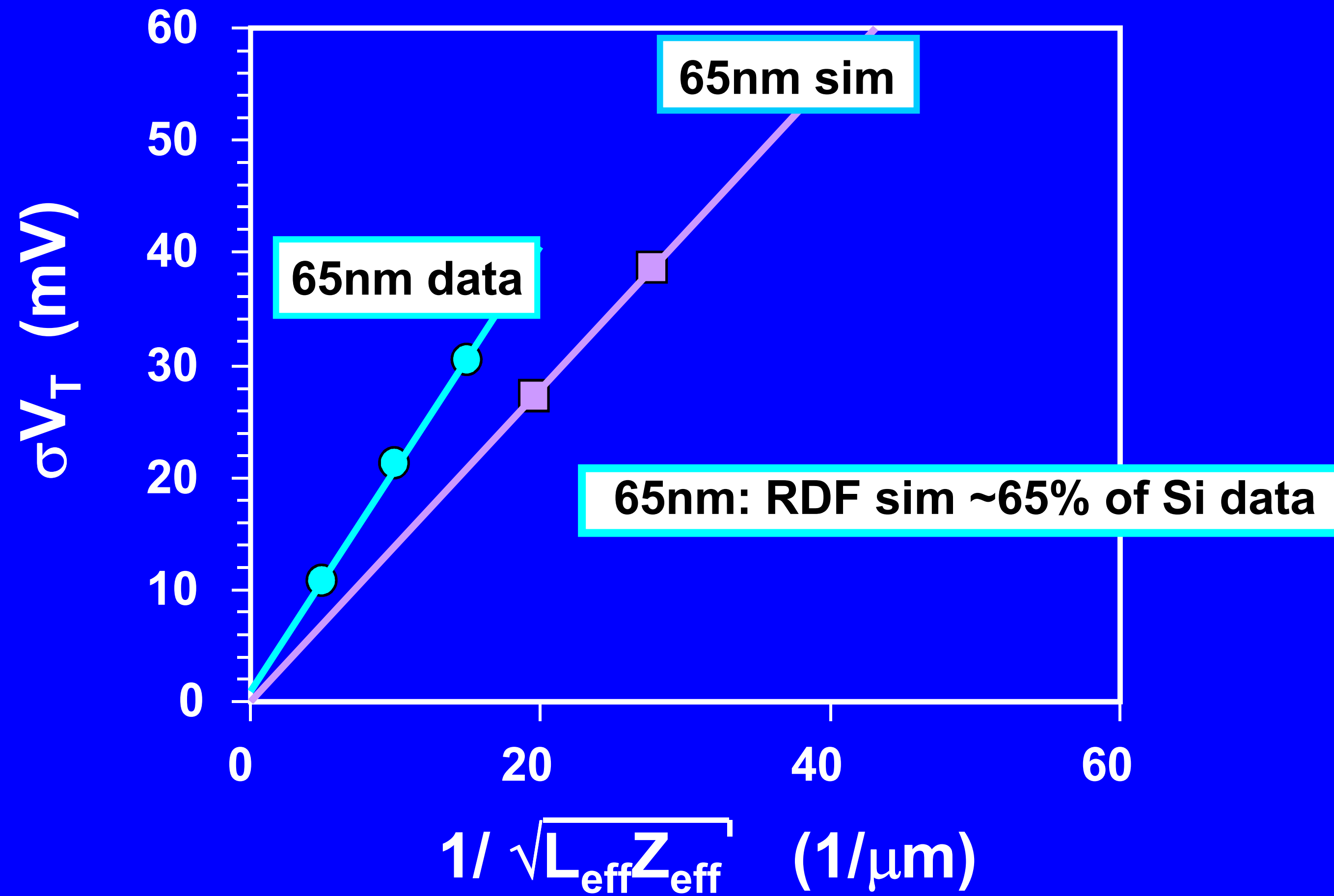
$$\sigma V_{Tran} = \left(\frac{\sqrt[4]{4q^3 \varepsilon_{si} \phi_B}}{2} \right) \cdot \frac{T_{ox}}{\varepsilon_{ox}} \cdot \left(\frac{\sqrt[4]{N}}{\sqrt{Leff \cdot Zeff}} \right) = \frac{1}{\sqrt{2}} \left(\frac{c_2}{\sqrt{Leff \cdot Zeff}} \right) \quad (1)$$

RDF – Silicon to Simulation

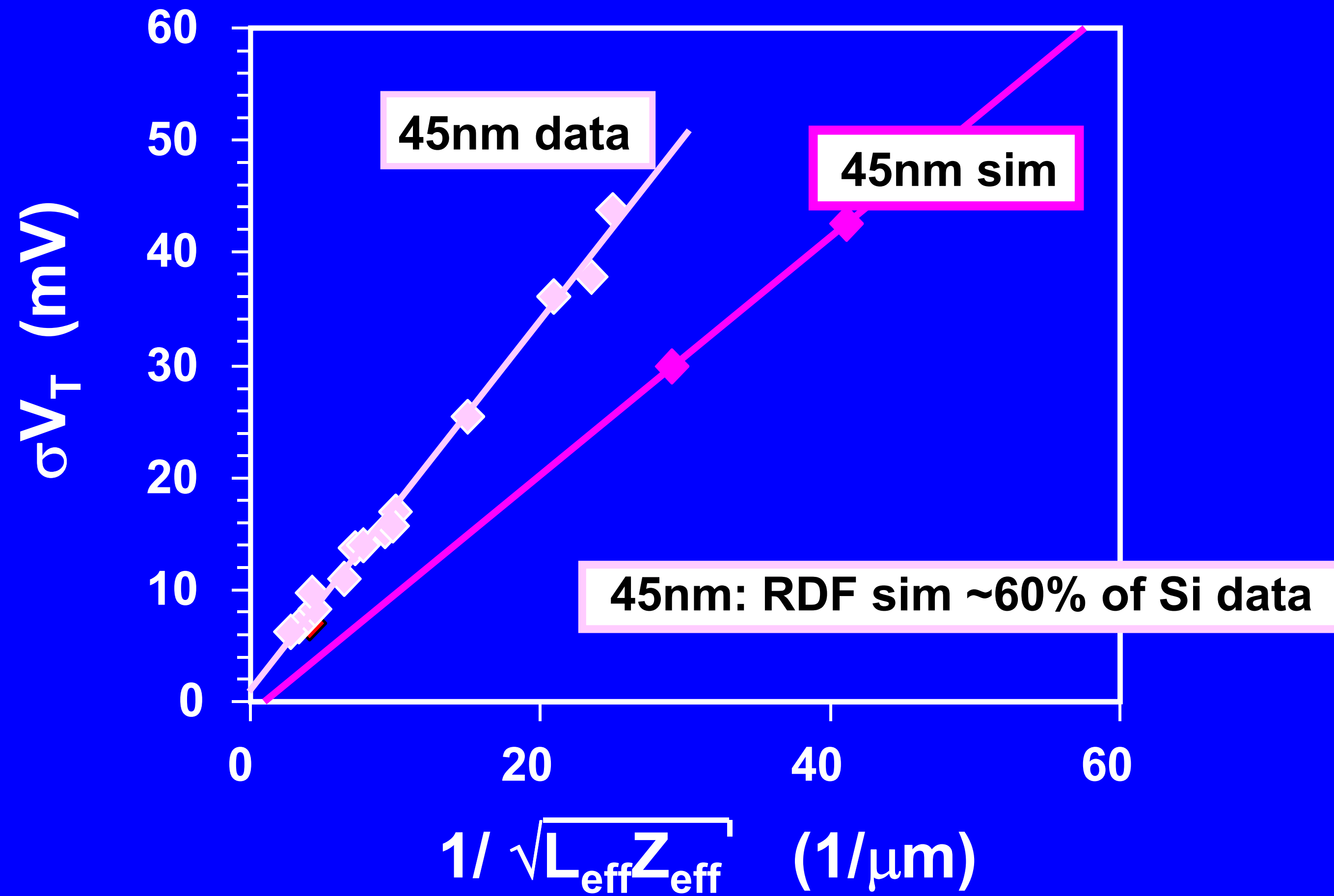


- **Correlation of theoretical RDF predictions against experimental data can provide insight into non-RDF variation sources.**
- **RDF simulations performed using a 3D numerical model with adaptive local meshing for arbitrary dopant profiles**

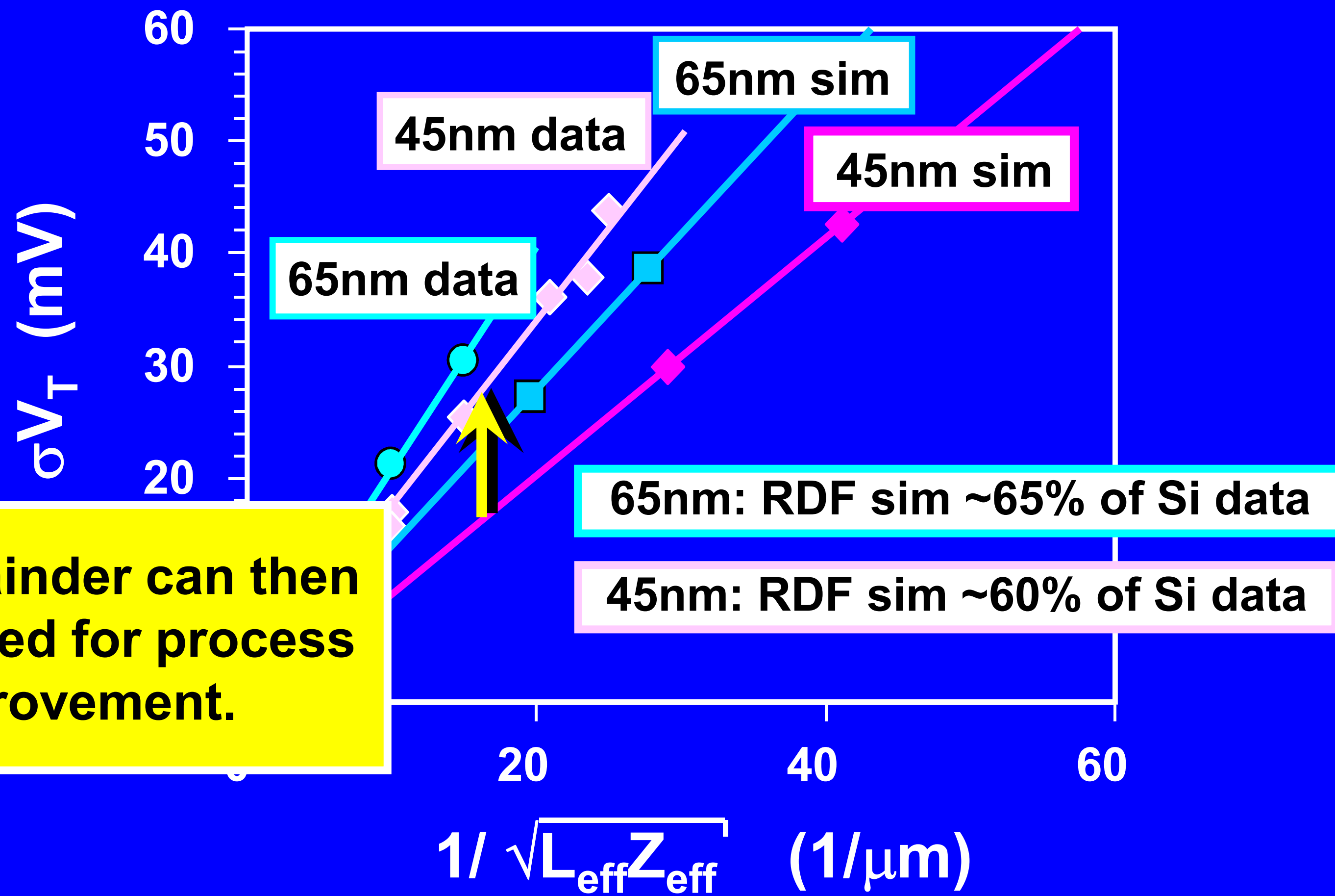
RDF – Silicon to Simulation



RDF – Silicon to Simulation

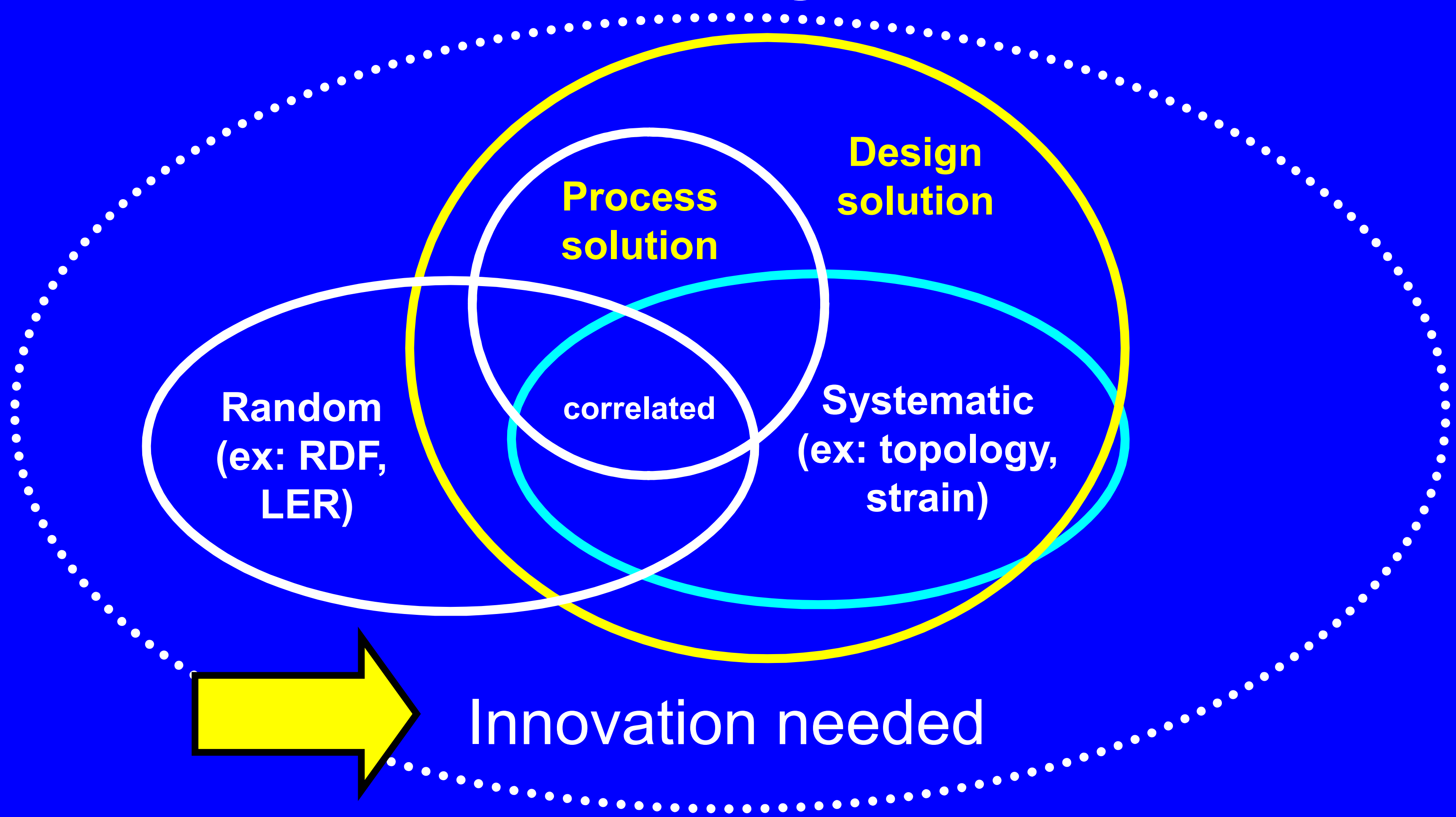


RDF – Silicon to Simulation



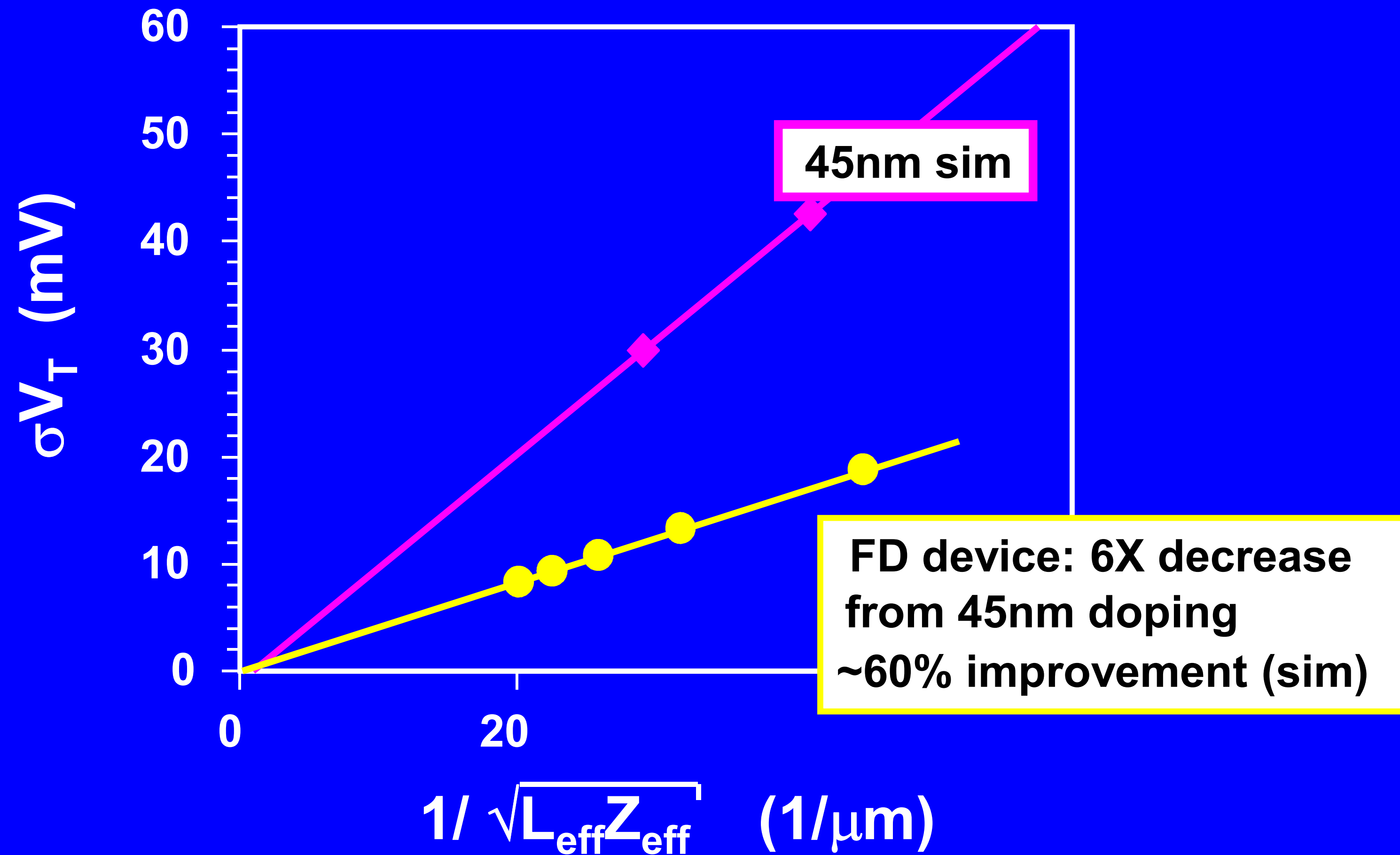
The remainder can then be targeted for process improvement.

But what happens next with RDF? Does scaling stop?



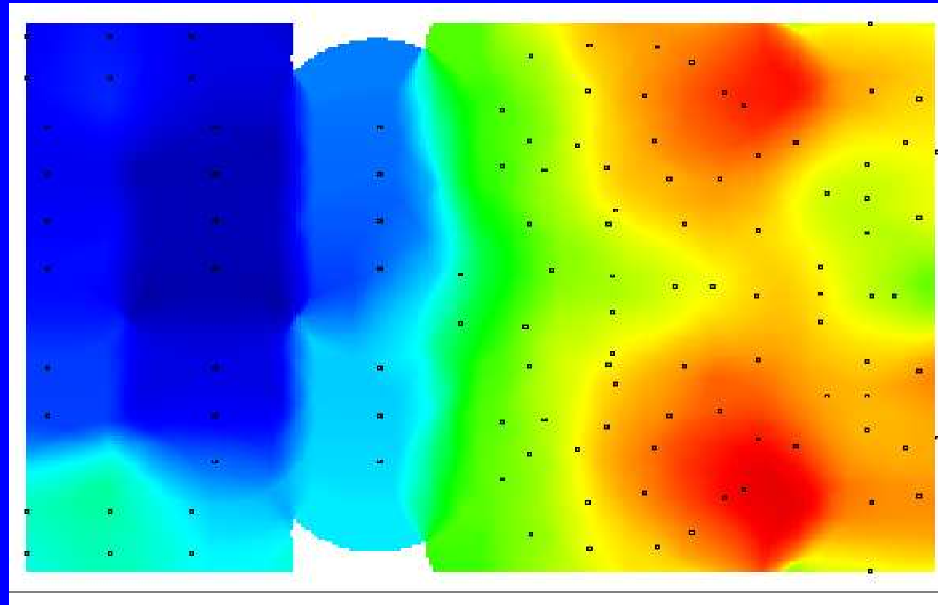
A variety of paths exist for variation improvement
RDF can be addressed through innovation

RDF: Improvement with fully depleted devices



Fully depleted devices (such as tri-gate or UTB devices) are examples of innovations which permit significant improvement in RDF due to the ability to maintain channel control at lower channel doping.

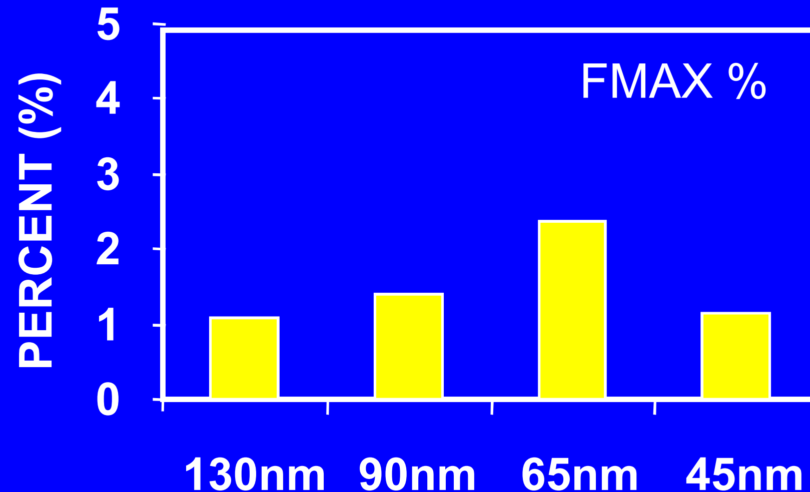
Measurement of Random Variation with Ring Oscillators



One powerful tool for assessment of variation is locating ring-oscillators (ROs) routinely in all product designs

The detailed RO data can be used to identify areas of concern for process teams to resolve

Scaling of Random WIW Variation

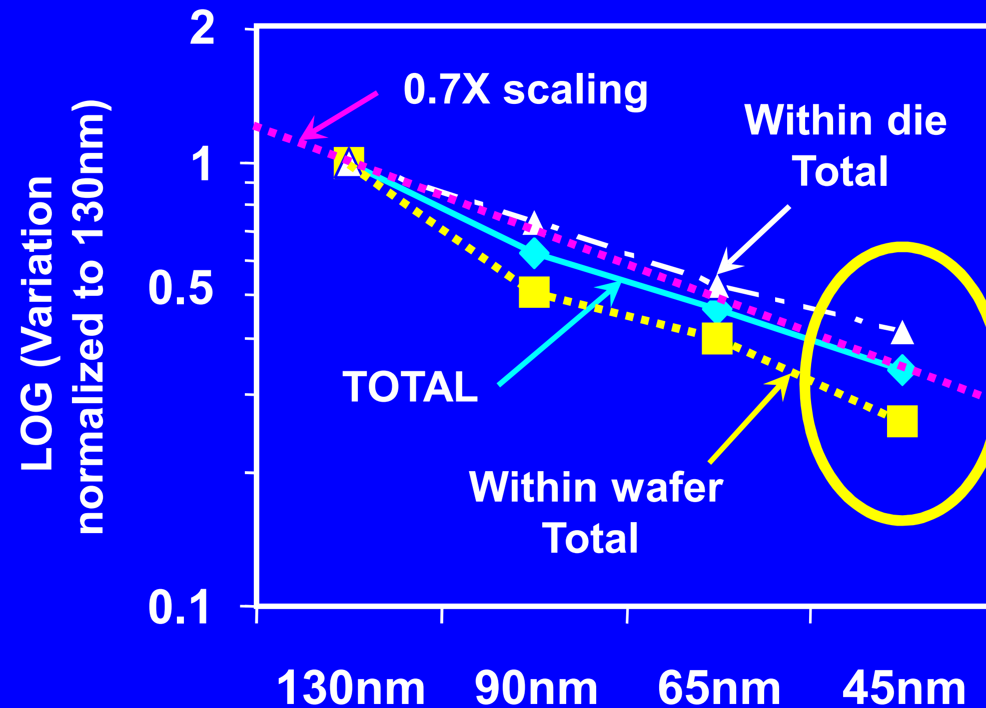


Comparisons from RO data show that random WIW variation has improved significantly between 65nm and 45nm due to HiK-MG

Random WIW variation in 45nm is comparable to prior generations

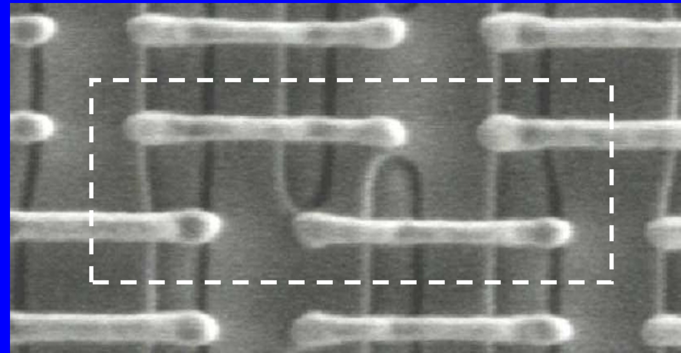
Systematic Variation

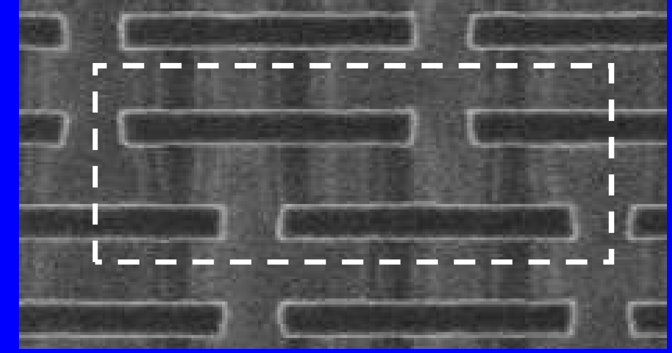
Scaling Systematic Poly CD (gate CD) Lithography Variation



Critical to management of variation is the ability to deliver a 0.7X poly CD variation improvement in each generation enabled by continuous process technology improvements

Process-Design Mitigation for Variation Management

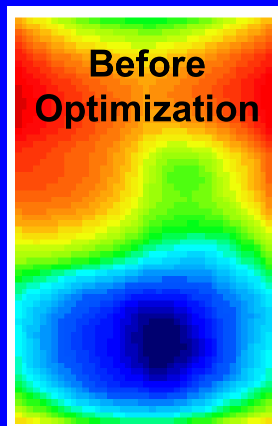


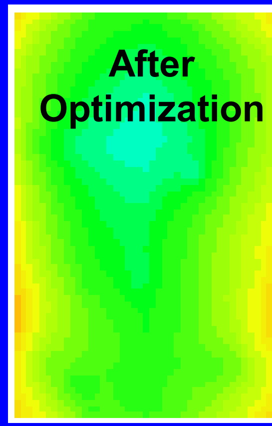


90nm – tall
1.0 μm²

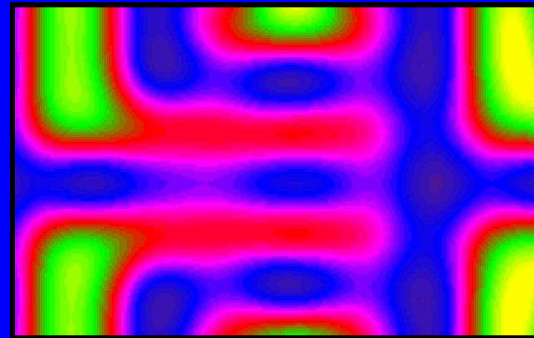
→ Design mitigation
65nm – wide - 0.57 μm²

→ Process mitigation - 45nm – wide
w/ patterning enhancement 0.346 μm²

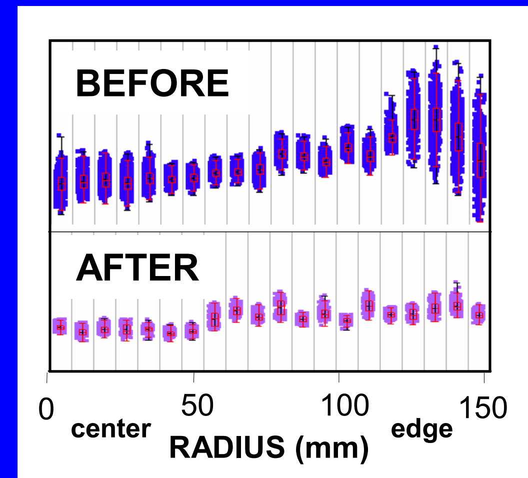




Design mitigation
w/ dummification

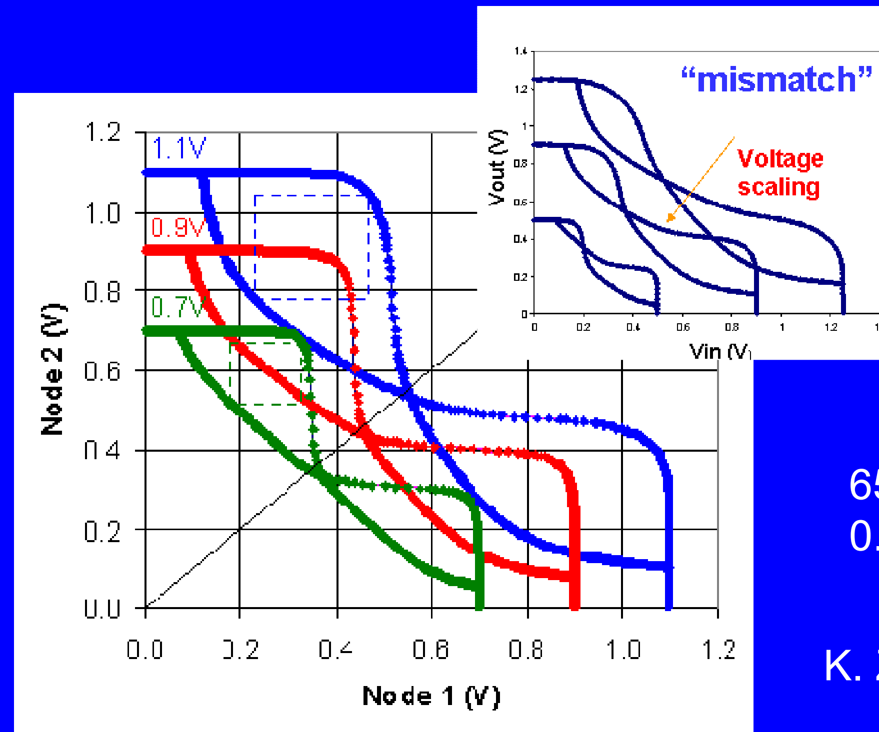


Process/design mitigation with
computational lithography



Process mitigation
w/ CMP improvements

Systematic Mismatch in the SRAM



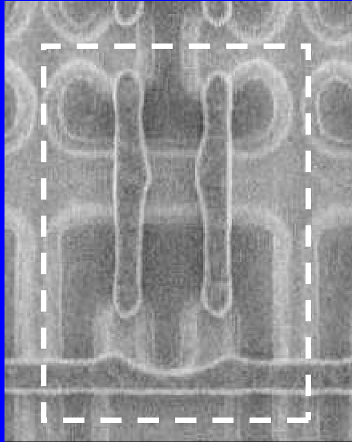
65nm – WIDE
0.57 μm^2

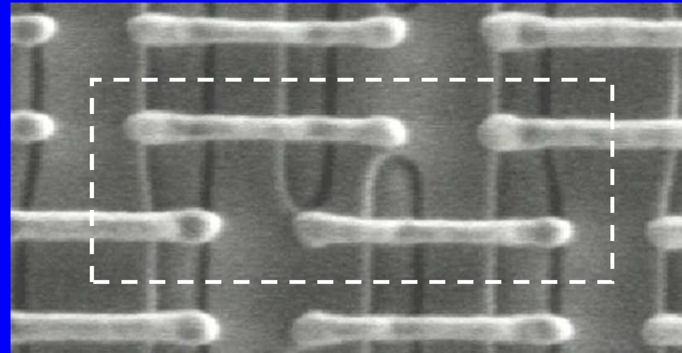
K. Zhang, VLSI 2004

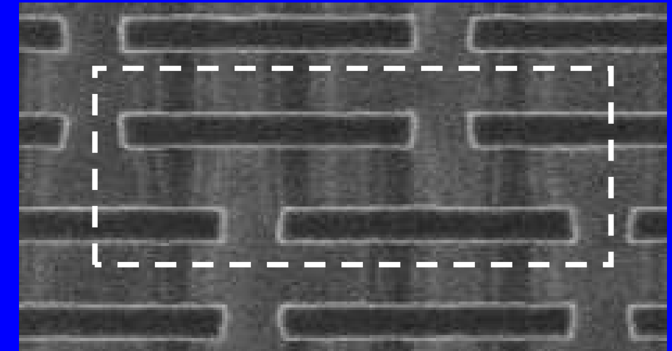
- SRAM circuits exercise the smallest area devices in the technology
- SRAM static noise margin (SNM) is sensitive to device mismatch
- Although RDF is the fundamental limit for mismatch in the SRAM
  a large variety of systematic issues also contribute to SRAM cell mismatch

→ **These systematic issues can be mitigated with design and process changes**

Systematic Variation Mitigation Strategies







90nm – TALL
1.0 μm^2

65nm – WIDE
0.57 μm^2

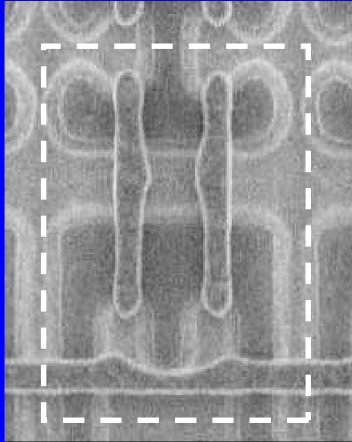
45nm – WIDE
w/ patterning enhancement 0.346 μm^2

DESIGN MITIGATION

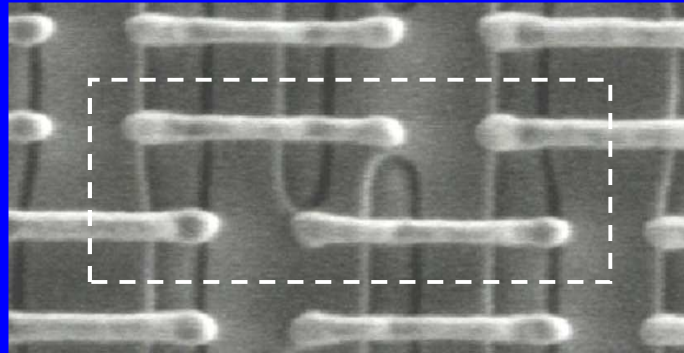
90nm to 65nm: "tall" design to a "wide" design.

- Single direction poly
- Elimination of diffusion corners
- Relaxation of patterning constraints on other critical layers

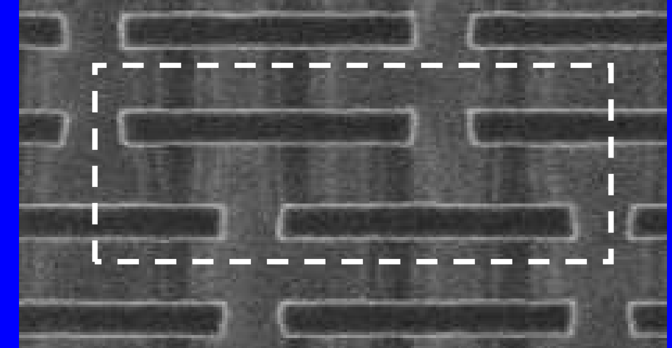
Systematic Variation Mitigation Strategies



90nm – TALL
1.0 μm²



65nm – WIDE
0.57 μm²



45nm – WIDE
w/ patterning enhancement 0.346 μm²

PROCESS MITIGATION

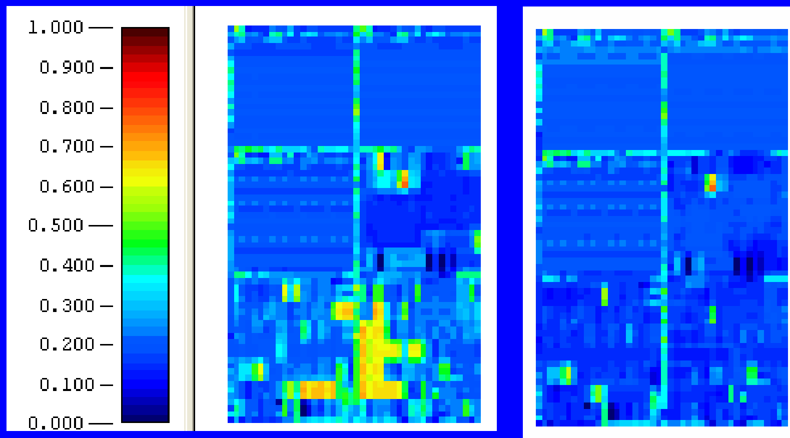
65nm to 45nm: Patterning enhancements

- Square corners (eliminate “dogbone” and “icicle” corners)
- Improved CD uniformity across STI boundaries

Systematic Front-End Variation

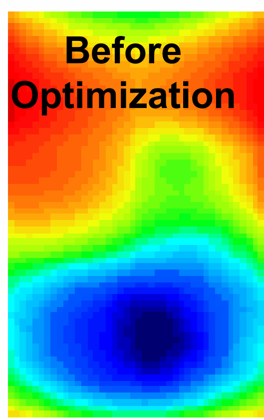
Before Optimization

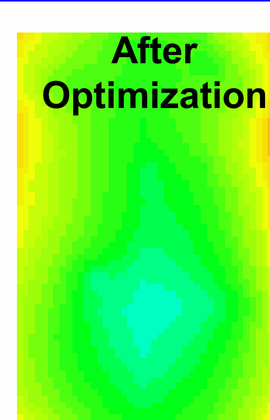
After Optimization



Poly Layout Extraction

10.00
8.00
6.00
4.00
2.00
0.00
-2.00
-4.00
-6.00
-8.00
-10.00

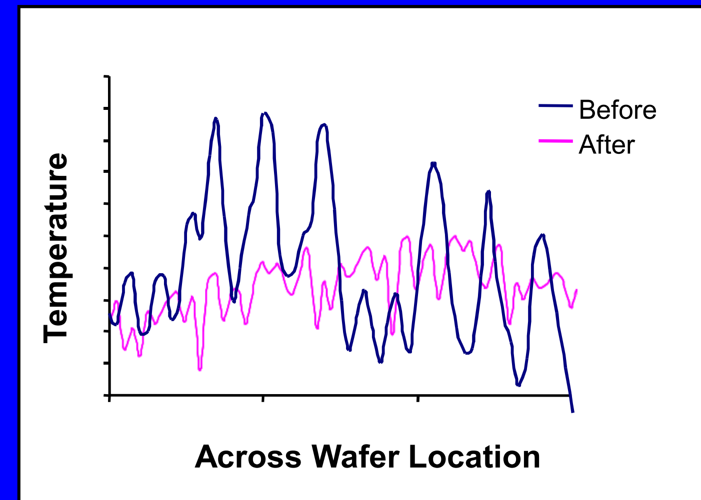




Temperature Simulation

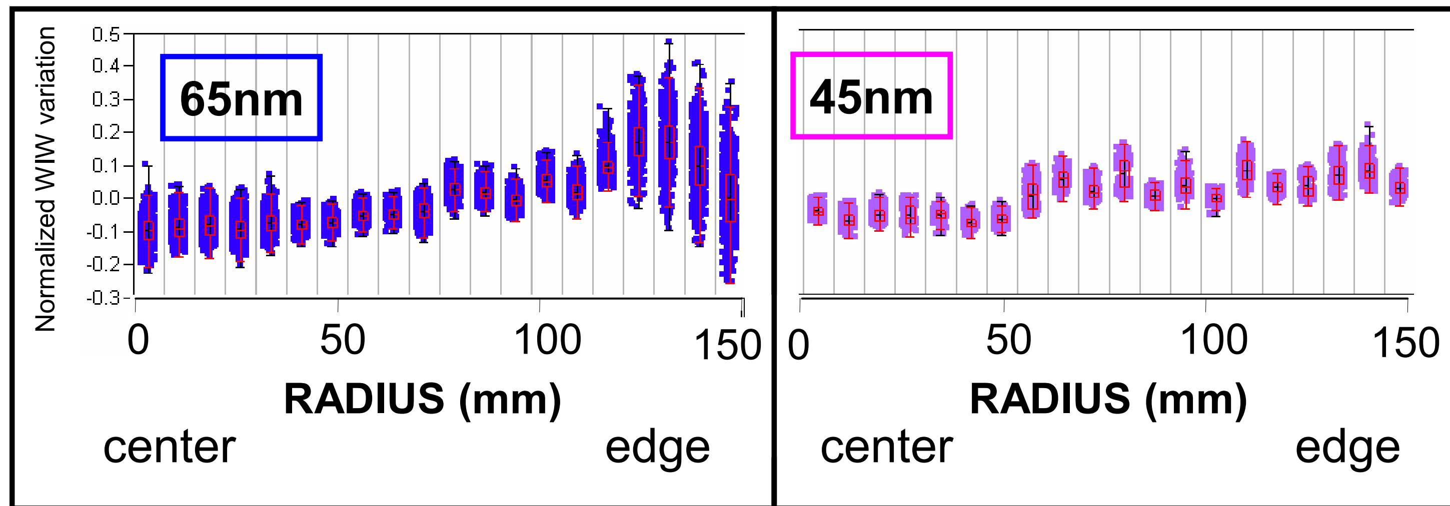
S. Rikhi, SEMI ISS 2007

In Fab Temperature Profile



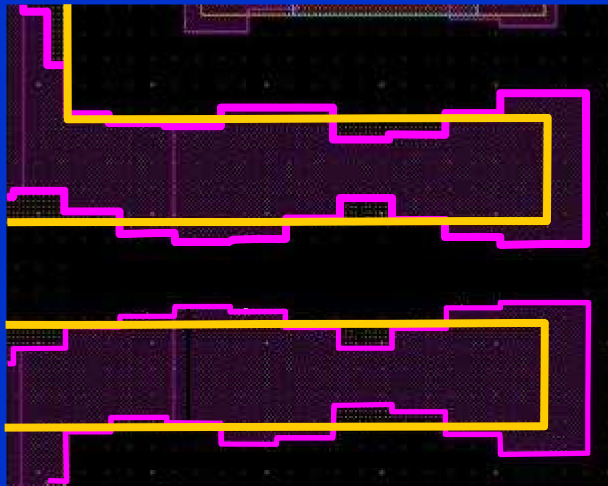
Addition of poly (gate) dummies to improve RTA temperature uniformity and reduce systematic transistor variation

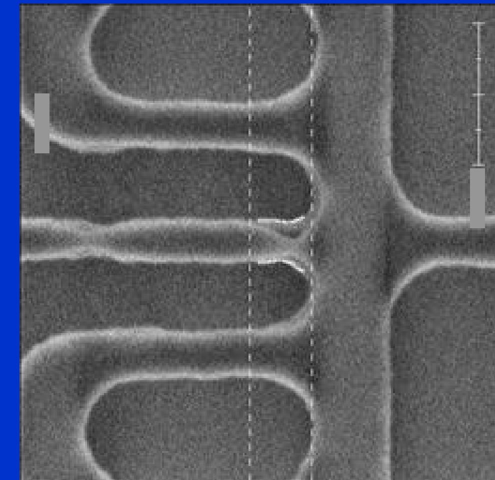
Systematic Interconnect Variation



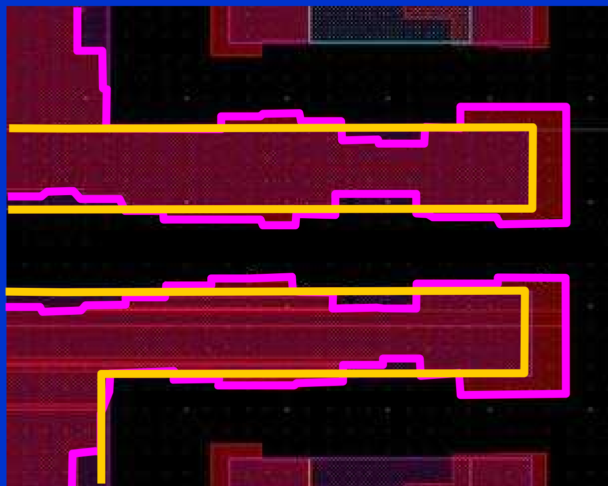
- Recent literature has devoted to modeling interconnect variation
- While improved modeling can be valuable, a better approach is to resolve the issue at the origin by eliminating the original source of the variation
- Example is 65nm to 45nm MT1 within-wafer resistance uniformity improvement due to improvements in etch and Cu CMP

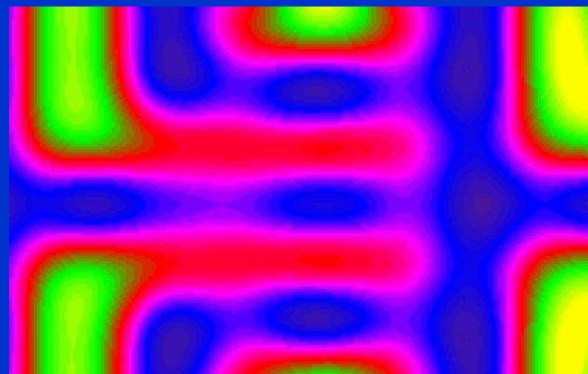
Backend Computational Lithography - DFM example

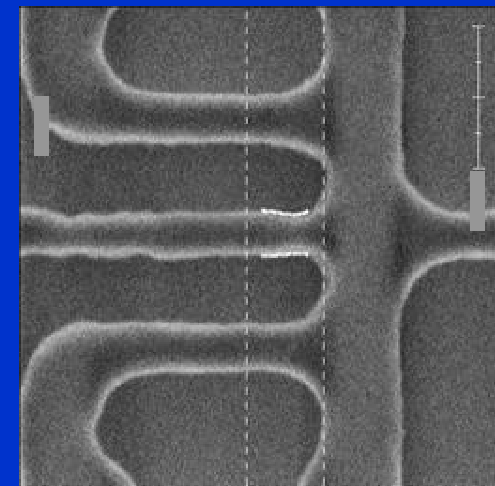




Top-down resist CD meets spec, but poor contrast leads to poor resist profile which gets transferred to metal pattern after etch, resulting in shorting marginality

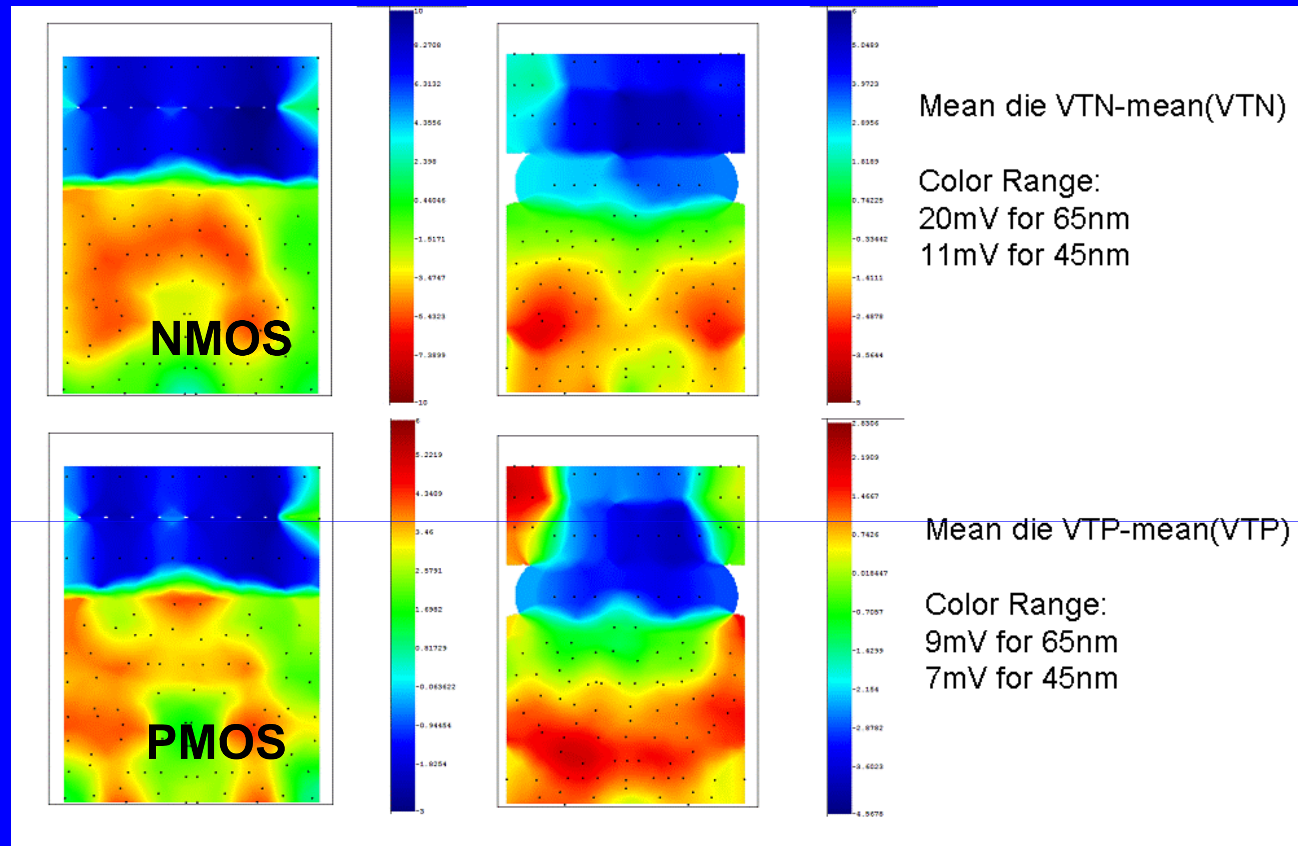






Computational lithography solution

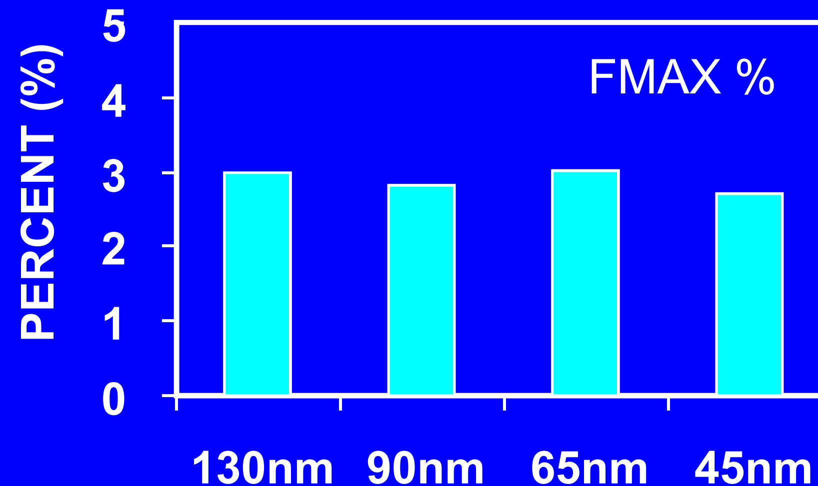
Measurement of Systematic WID Variation



65nm microprocessor **45nm microprocessor**

Comparisons from RO data show that systematic WID VT variation is improving from the 65nm to 45nm generation

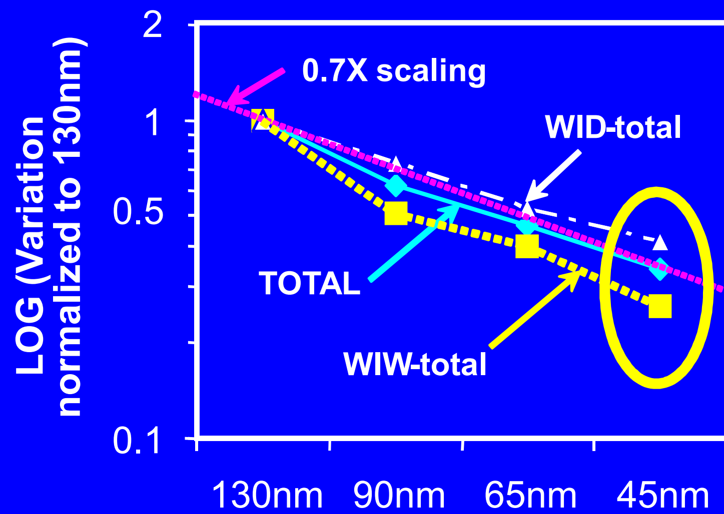
Scaling of Systematic WIW Variation

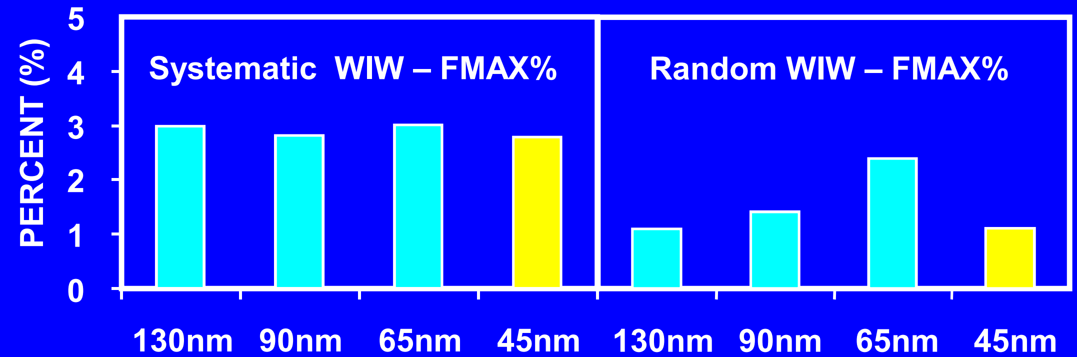


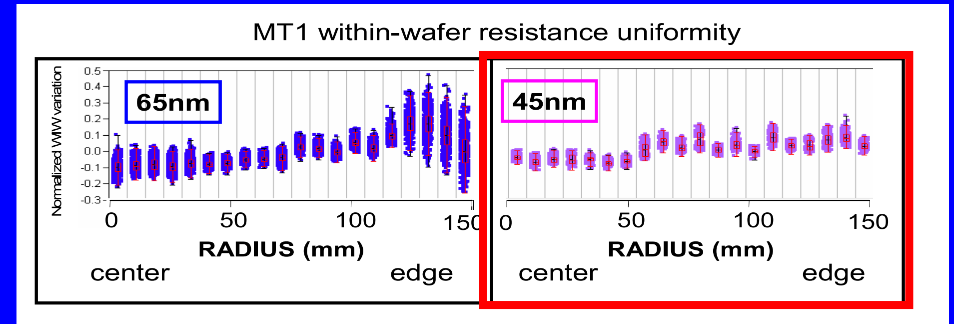
Comparisons from RO data show that systematic WIW variation is comparable from one generation to the next

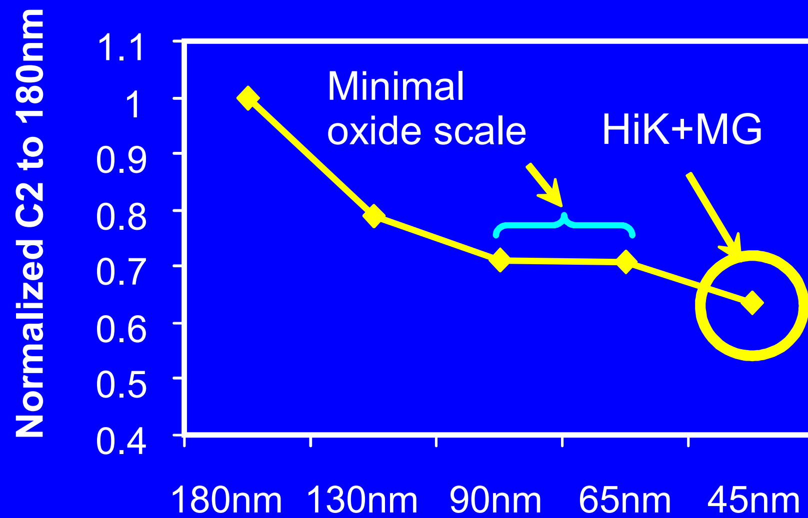
45nm variation

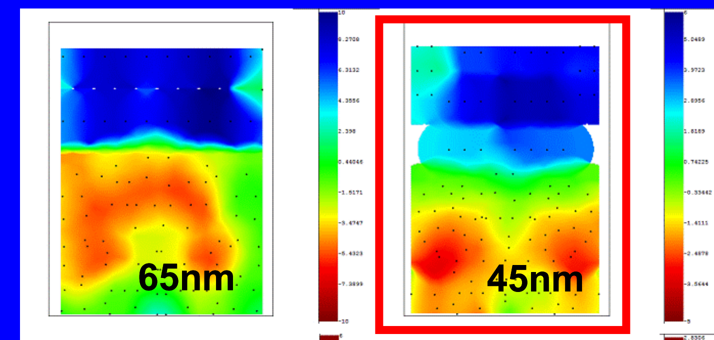
45nm: Variation matched/better to past technologies











VTN variation (Mean die VTN – VTN)
Range: 20mV for 65nm → 11mV for 45nm

Key messages

- Process variation is not a new problem
- A variety of process, design and layout techniques can be applied to mitigate the impact of random and systematic variation
- Improvements in variation in 45nm illustrate that variation does not pose an insurmountable barrier to Moore’s Law, but is simply another challenge to be overcome

Acknowledgements

The 45nm process and design teams

Individuals: Robert Bigwood, Tao Chen, Martin Giles, Mingwei-Huang, Chris Kenyon, Avner Kornfeld, Sean Ma, Peter Moon, Kevin Zhang and: Mark Bohr, Kaizad Mistry

For further information on Intel's silicon technology, please visit our Technology & Research page at: www.intel.com/technology

Q & A

REFERENCES

1. S. Borkar, "Designing reliable systems from unreliable components: the challenges of transistor variability and degradation," IEEE *Micro*, 26:6, pp. 10-16, Nov-Dec. 2005.
2. S. Springer et al., "Modeling of Variation in Submicrometer CMOS ULSI Technologies," IEEE Trans. on Elec. Dev., 53:9, pp. 2168-78, Sept. 2006,
3. H. Mahmoodi, S. Mukhopadhyay and K. Roy, "Estimation of delay variations due to random-dopant fluctuations in nanoscale CMOS circuits," IEEE J. of Solid State Circuits, 40:9, pp 1787-1795, Sept. 2005.
4. H.Fukutome et al., "Direct Evaluation of Gate Line Edge Roughness Impact on Extension Profiles in Sub-50-nm n-MOSFETs," IEEE Trans. Elec. Dev., 53:11, pp 2755 – 2763, Nov. 2006.
5. M. Miyamura, "SRAM critical yield evaluation based on comprehensive physical/statistical modeling, considering anomalous non-Gaussian intrinsic transistor fluctuations," 2007 Sym. VLSI Tech., pp. 22-23.
6. A. Asenov, S. Kaya, and J.H. Davies, "Intrinsic threshold voltage fluctuations in decanano MOSFETs due to local oxide thickness variations," IEEE Trans. on Elec. Dev., 49:1, pp. 112-119, Jan. 2002,
7. J. R. Brews, "Surface potential fluctuations generated by interface charge inhomogeneities in MOS devices," J. Appl. Phys., vol. 43, pp. 2306−2313, 1972
8. L. Capodieci, "From optical proximity correction to lithography-driven physical design (1996-2006): 10 years of resolution enhancement technology and the roadmap enablers for the next decade," Proc. SPIE Vol. 6154, 615401
9. C.T. Liu et al., " Severe thickness variation of sub-3nm gate oxide due to Si surface faceting, poly-Si intrusion and corner stress" 1999 Sym. VLSI Tech., pg. 75-76.
10. T.K. Yu, et al., "A two-dimensional low pass filter model for die-level topography variation resulting from chemical mechanical polishing of ILD films," IEDM 1999, pp 909-912.
11. I. Ahsan et al., "RTA-Driven Intra-Die Variations in Stage Delay, and Parametric Sensitivities for 65nm Technology," 2006 Sym. VLSI Tech. pp. 170-1
12. T. Tanaka et al., "Vth fluctuation induced by statistical variation of pocket dopant profile," IEDM 2006, pp 271-274
13. A. Asenov, "Simulation of Statistical Variability in Nano MOSFETs," 2007 Sym. VLSI Tech., pg. 86-7
14. E. Fetzer, "Using Adaptive Circuits to Mitigate Process Variations in a Microprocessor Design," IEEE Design.and Test of Computers, 23:6, pp. 476 – 483, June 2006.
15. P. Stolk, F. Widdershoven, and D/ Klaassen, "Modeling statistical dopant fluctuations in MOS transistors" IEEE Trans. on Elec. Dev., 45:9, pp 1960-1971, Sept. 1998.
16. A. Asenov, Random dopant induced threshold voltage lowering and fluctuations in sub-0.1 μm MOSFET's: A 3-D "atomistic" simulation study ," IEEE Trans. on Elec. Dev., 45:12, pp. 2505 – 2513, Dec. 1998.
17. H. Yang, et. al, "Current mismatch due to local dopant fluctuations in MOSFET channel," IEEE Trans. on Elec. Dev., 50:11, pp. 2248-2254, Nov. 2003.
18. J. Kavalieros et. al, "Tri-Gate Transistor Architecture with High-k Gate Dielectrics, Metal Gates and Strain Engineering, 2006 Sym. VLSI Tech., pg. 50-1.
19. K. Zhang et al., "SRAM design on 65nm CMOS technology with integrated leakage reduction scheme," 2004 Sym. VLSI Cir., pp. 294-5.
20. S. Bhunia, S. Mukhopadhyay, and K. Roy, "Process Variations and Process-Tolerant Design," Int'l Conf. on VLSI Design, 2007, pp. 699 – 704 and similar.
21. K Soumyanath, S. Borkar, Z. Chunyan and B. Bloechel, "Accurate on-chip interconnect evaluation: a time-domain technique," IEEE J. of SS Cir., pp. 623-631, May 1999.
22. V. Mehrotra, "Modeling the effects of manufacturing variation on high-speed microprocessor interconnect performance," IEDM 1998, pp767-770.