Reducing Variation in Advanced Logic Technologies: Approaches to Process and Design for Manufacturability of Nanoscale CMOS

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Abstract

This paper presents an overview of process variation effects, including examples of mitigation strategies and test methods. Experimental and theoretical comparisons are presented for both 45nm and 65nm RDF. SRAM matching and interconnect variation is discussed for both 65nm and 45nm, including examples of process and design mitigation strategies. Use of ring oscillators for detailed measurement of within-wafer and within-die variation is illustrated for 65nm and 45nm products

Introduction

Moore's Law driven technology scaling has improved VLSI performance by five orders of magnitude in the last four decades. As advanced technologies continue the pursuit of Moore's Law, a variety of challenges will need to be overcome. One of the most significant of these challenges is management of variation [1,2]. While variation is certainly not new, the continued decrease in the ratio of feature sizes to fundamental dimensions (such as atomic dimensions and light wavelengths) means that management of variation will play an increasingly important role in future technology scaling.

Variation Taxonomy

Critical to any discussion of variation (see Fig. 1) is whether the impact of a variation effect is fundamental (i.e. requiring a disruptive invention to circumvent) or resolvable (i.e. can be fixed with continued technology improvements over time). A large number of variation effects of both types have been documented in the literature [3-14]. Examples include: highly random effects (random dopant fluctuation, RDF [3], line-edge roughness, LER [4-5], local oxide thickness variations [6], interface charge nonuniformities [7]), patterning proximity effects (classical and OPC/RET [8]), proximity effects associated with stress (overlayers, PMOS epitaxy, STI-induced [9]), proximity effects associated with polish (STI and ILD [10]), proximity effects associated with anneals (RTA-generated [11]), device-related (pocket implants [12] poly grains, oxide thickness [13]), and design-related (hot spots, droop) [14.].

Random dopant fluctuation (RDF)

MOS threshold voltage variation due to random fluctuations in the number and location of dopant atoms is an increasingly significant effect. RDF is assumed to be

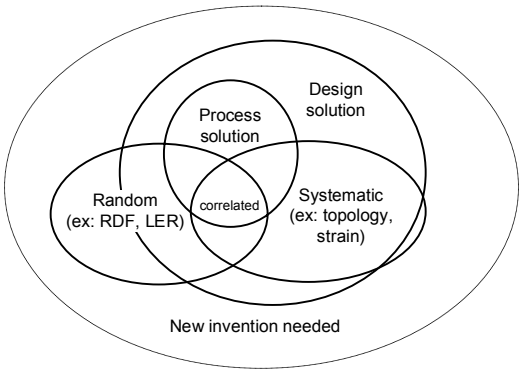

Fig.1 Typical variation effects in relation to their solution path

the major contributor to device mismatch of identical adjacent devices and is frequently represented by (1)

$$\sigma V_{Tran} = \left(\frac{\sqrt[4]{4q^3 \varepsilon_{si} \phi_B}}{2} \right) \cdot \frac{T_{ox}}{\varepsilon_{ox}} \cdot \left(\frac{\sqrt[4]{N}}{\sqrt{Weff \cdot Leff}} \right) = \frac{1}{\sqrt{2}} \left(\frac{c_2}{\sqrt{Weff \cdot Leff}} \right) \quad (1)$$

illustrating that matching improves with decreases in channel doping (*N*) and gate oxide thickness (*Tox*), and degrades when device area decreases[15].

Historical scaling suggests a continued improvement in C2 with Tox scaling. However, the historical improvement trend in C2 slowed when gate leakage concerns limited Tox scaling with conventional gate oxides at 65nm (Fig. 2). HiK+MG, enables a return to a historical scaling trend with associated matching improvement.

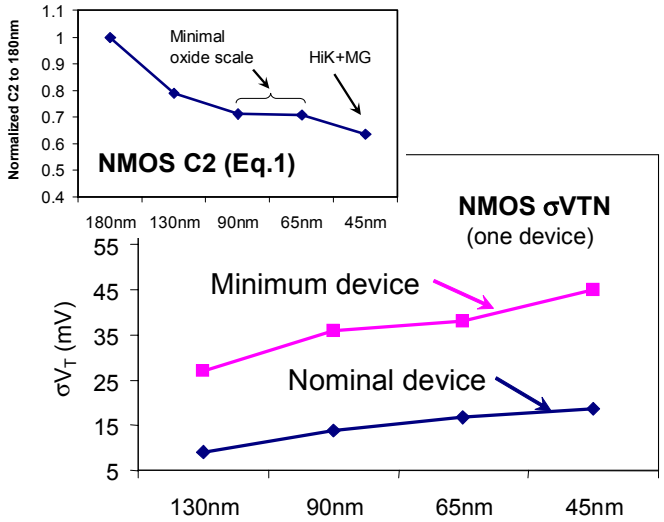

Fig.2 Scaling of σVT random variation over technology generation

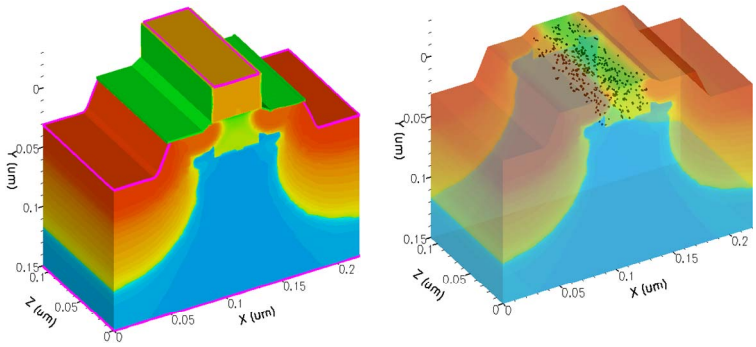

Fig.3. 3D RDF modeling – example of dopants in channel

Many studies have attempted to correlate theoretical predictions of RDF against experimental matching data [16-17]. In our work, we developed a 3D numerical model with an adaptive local meshing scheme that allows prediction of VT for arbitrary dopant profiles (see Fig. 3).

The model uses a weighted cumulative probability distribution function to statistically distribute dopant atoms in a device according to the average nonuniform background doping profile, and a Poisson probability function to obtain a statistical number of dopant atoms to be distributed in the device. We compared the results of this model for both 45nm and 65nm against device matching data (see Fig. 4).

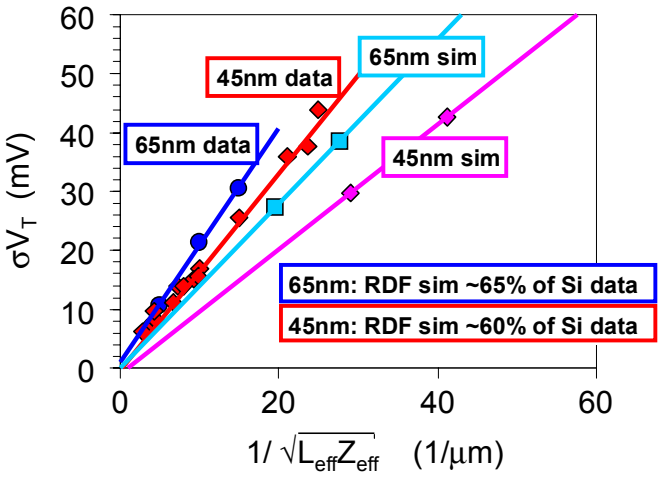

Fig.4. 65nm and 45nm transistor variation, data compared to RDF simulations under equivalent doping conditions

In comparison of simulation results to 65nm silicon data (see Fig. 4), our results show that simulated RDF is ~65% of the total sigmaVt. Similar results are obtained when comparing 45nm simulation results to data where the simulated RDF is ~60% of the total sigmaVt. The remainder can then be targeted for process improvement.

As one final point, RDF is a good example of a fundamental variation effect which requires a disruptive invention to resolve. One example of such a disruptive invention is a fully depleted device (such as an UTB or Trigate [18] device) where channel control can be maintained with significantly lower channel doping. An example of the improvement possible with a disruptive invention is illustrated with Trigate simulation data in Fig. 5. The improvement from a conventional planar to Trigate geometry (at matched doping) is 10%. The improvement at 6X reduced channel doping enabled by the improved Trigate gate control is 60%.

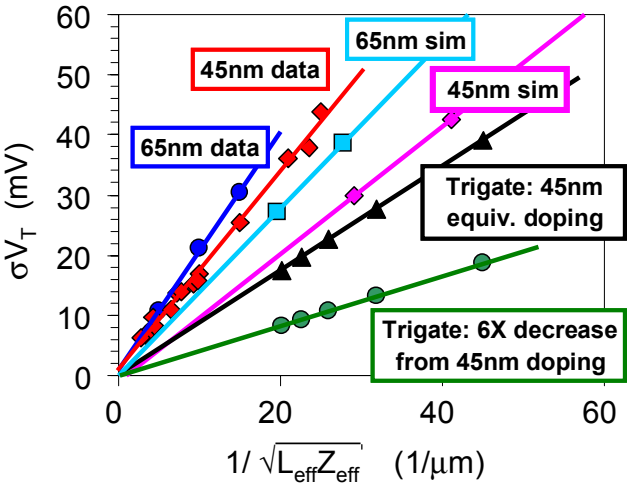

Fig.5. 65nm and 45nm transistor variation, additional benefit of a fully-depleted geometry such as Trigate

SRAM

The SRAM exercises some of the smallest area devices in the technology and the SRAM SNM is quite sensitive to device mismatch (see Fig. 6). While RDF (discussed above) likely represents the fundamental limit for mismatch in the SRAM, a variety of systematic issues (particularly lithography constraints) can contribute significantly to SRAM cell mismatch. These issues can be successfully mitigated with both design and process changes.

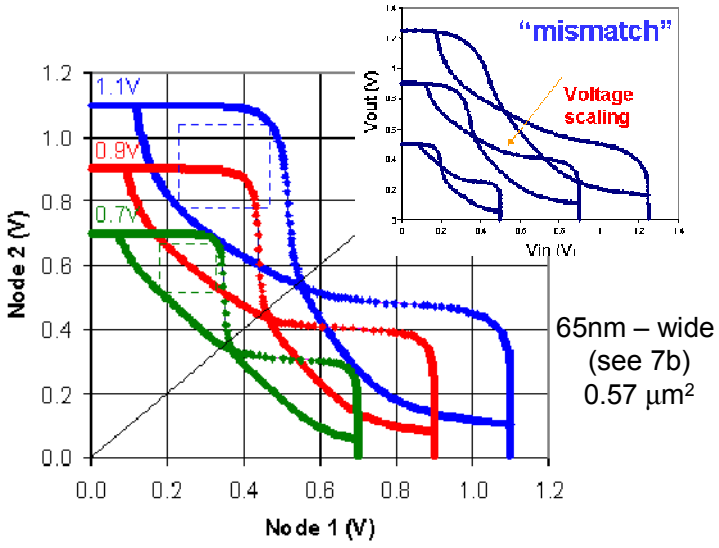

Fig.6. SRAM SNM improvement from "tall" (inset) to "wide" (main)

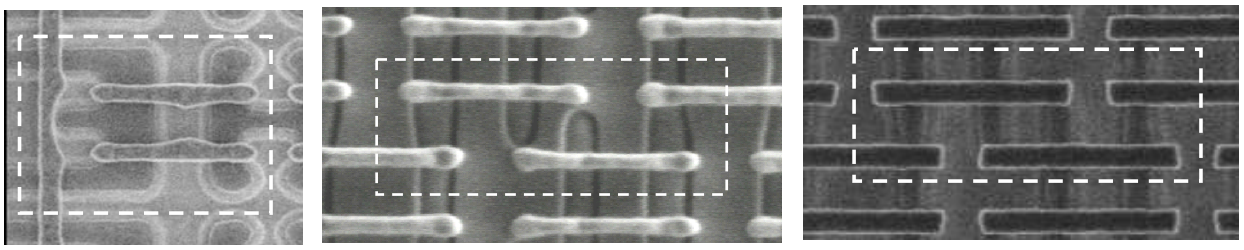

Fig.7 Cell topology enhancements for mismatch improvement

An example of a design mitigation strategy is to change the topology of the SRAM from a "tall" design to a "wide" design (see Figs. 6-7 and [19]). The wide design improves CD control and variation by aligning the poly in a single direction, eliminating diffusion corners, and relaxing some patterning constraints on other critical layers. A process mitigation strategy (Fig. 7c) is to change the poly patterning process so that the poly endcaps are square rather than rounded. Square endcaps eliminate the variation associated with "dogbone" and "icicle" endcaps.

Front-end

Transistor variation is driven by many factors [3-14], however poly Lgate control and the control of diffusion anneal steps are particularly significant. Fig. 8 provides an example of variation improvement over time in poly CD enabled by continuous process technology improvements. Fig. 9 shows an example of a design mitigation strategy where dummy features were incorporated to improve poly density and thus improve RTA temperature uniformity to reduce systematic transistor variation.

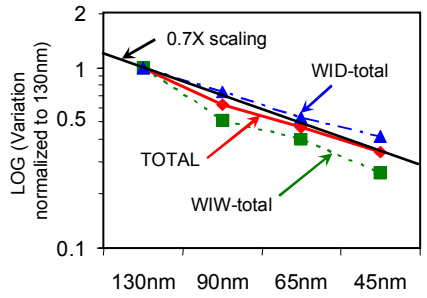

Fig.8 Poly CD variation improvements per generation

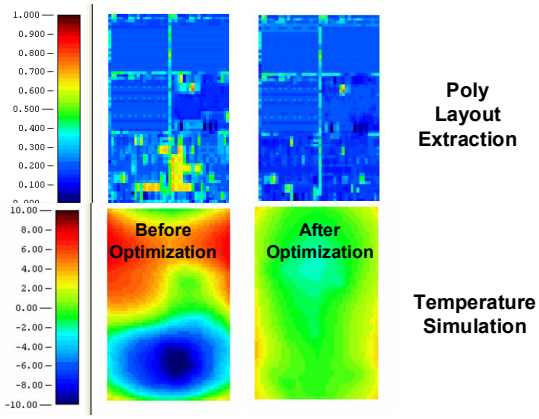

Fig.9. RTA temperature uniformity improvements with poly dummies

Interconnect

Much recent literature has been devoted to the topic of modeling interconnect variation [20-22]. While improved modeling can be valuable, our approach is to resolve the issue at the origin by eliminating the original source of the variation. One example is shown in Fig. 10, which illustrates the improvement in 45nm MT1 within-wafer resistance uniformity over 65nm due to improvements in Cu CMP. A second example is shown in Fig. 11, which shows the improvement resulting from an OPC/RET update which resolved the issue of a poor resist profile causing variation in metal pattern after etch.

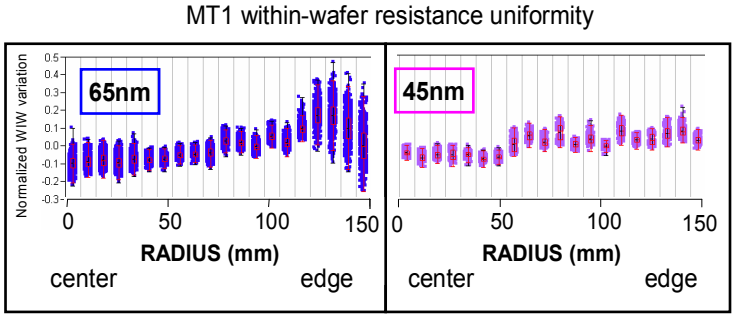

Fig.10. Improvement in MT1 uniformity enabled by Cu CMP

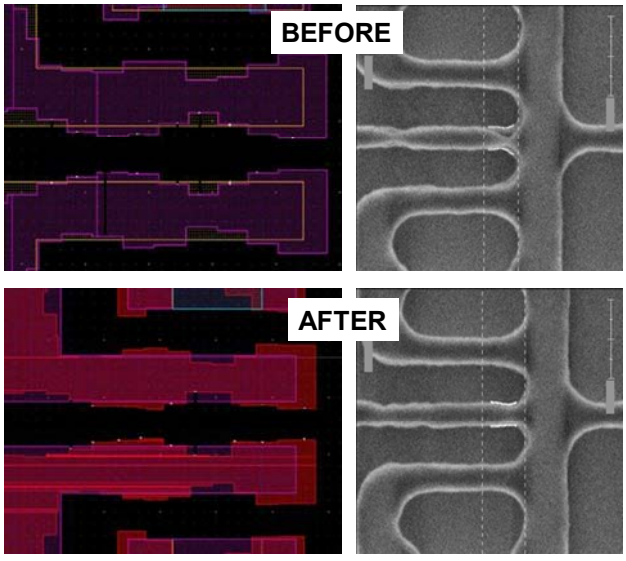

Fig.11 Improvement in MT1 resist profiles with OPC/RET

Measurement of variation with ring oscillators

One powerful tool for assessment of variation is locating ring-oscillators (ROs) routinely in all product designs. The detailed RO data can be used to identify areas of concern for process teams to resolve. Figs. 12-13 show examples of the use of RO f_{max} to determine systematic and random within-wafer (WIW) variation across generations. Fig. 14 gives a example of RO data (used in conjunction with a calibration structure) to extract 65nm to 45nm systematic within-die (WID) VT variation comparisons. The comparisons from RO data show that both WIW and WID variation is not increasing from one generation to the next.

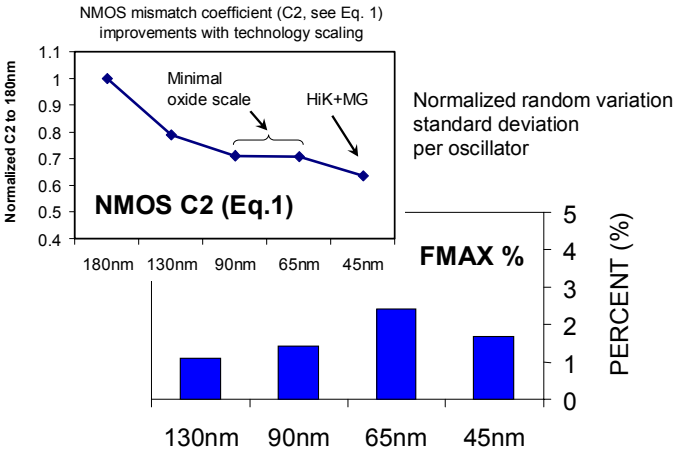

Fig.12. Technology scaling of WIW random variation from RO data

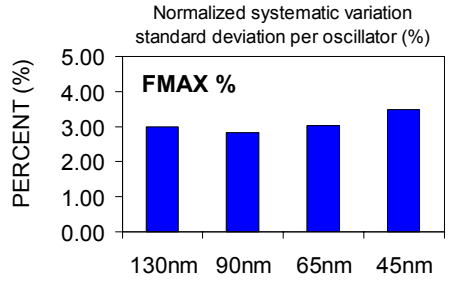

Fig.13.Technology scaling of WIW systematic variation from RO data

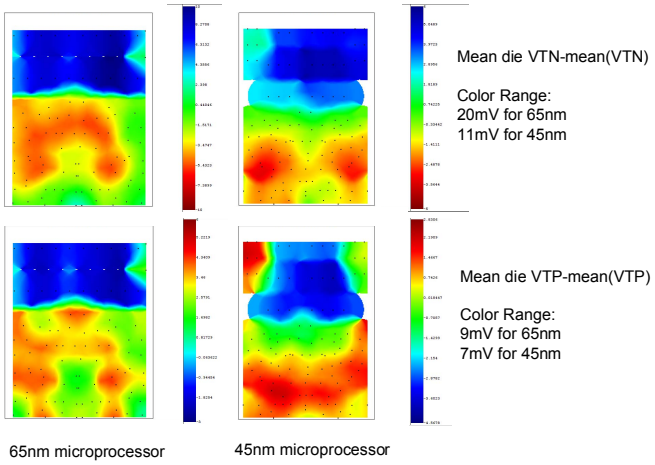

Fig.14. 65nm to 45nm systematic WID VT comparison from RO data

Conclusion

While management of variation is likely to play an increasingly important role in future technology scaling, a variety of process, design and layout techniques can be applied to mitigate the impact of this variation. Variation does not pose an insurmountable barrier to Moore's Law, but is simply another challenge to be overcome.

References

1. S. Borkar, "Designing reliable systems from unreliable components: the challenges of transistor variability and degradation," *IEEE Micro*, 26:6, pp. 10-16, Nov-Dec. 2005.
2. S. Springer et al., "Modeling of Variation in Submicrometer CMOS ULSI Technologies," IEEE Trans. on Elec. Dev., 53:9, pp. 2168-78, Sept. 2006,
3. H. Mahmoodi, S. Mukhopadhyay and K. Roy, "Estimation of delay variations due to random-dopant fluctuations in nanoscale CMOS circuits," IEEE J. of Solid State Circuits, 40:9, pp 1787-1795, Sept. 2005.
4. H.Fukutome et al., "Direct Evaluation of Gate Line Edge Roughness Impact on Extension Profiles in Sub-50-nm n-MOSFETs," IEEE Trans. Elec. Dev., 53:11, pp 2755 – 2763, Nov. 2006.
5. M. Miyamura, "SRAM critical yield evaluation based on comprehensive physical/statistical modeling, considering anomalous non-Gaussian intrinsic transistor fluctuations," 2007 Sym. VLSI Tech., pp. 22-23.
6. A. Asenov, S. Kaya, and J.H. Davies, **"**Intrinsic threshold voltage fluctuations in decanano MOSFETs due to local oxide thickness variations," IEEE Trans. on Elec. Dev., 49:1, pp. 112-119, Jan. 2002,
7. J. R. Brews, "Surface potential fluctuations generated by interface charge inhomogeneities in MOS devices," J. Appl. Phys., vol. 43, pp. 2306−2313, 1972
8. L. Capodieci, "From optical proximity correction to lithography-driven physical design (1996-2006): 10 years of resolution enhancement technology and the roadmap enablers for the next decade," Proc. SPIE Vol. 6154, 615401
9. C.T. Liu et al., " Severe thickness variation of sub-3nm gate oxide due to Si surface faceting, poly-Si intrusion and corner stress" 006 Sym. VLSI Tech., pg. 75
10. T.K. Yu, et al., "A two-dimensional low pass filter model for die-level topography variation resulting from chemical mechanical polishing of ILD films," IEDM 1999, pp 909-912.
11. I. Ahsan et al., "RTA-Driven Intra-Die Variations in Stage Delay, and Parametric Sensitivities for 65nm Technology," 2006 Sym. VLSI Tech. pp. 170-1
12. T. Tanaka et al., "Vth fluctuation induced by statistical variation of pocket dopant profile," IEDM 2006, pp 271-274
13. A. Asenov, "Simulation of Statistical Variability in Nano MOSFETs," 2007 Sym. VLSI Tech., pg. 86-7
14. E. Fetzer, "Using Adaptive Circuits to Mitigate Process Variations in a Microprocessor Design," IEEE Design.and Test of Computers, 23:6, pp. 476 – 483, June 2006.
15. P. Stolk, F. Widdershoven, and D/ Klaassen, **"**Modeling statistical dopant fluctuations in MOS transistors" IEEE Trans. on Elec. Dev., 45:9, pp 1960-1971, Sept. 1998.
16. A. Asenov, Random dopant induced threshold voltage lowering and fluctuations in sub-0.1 µm MOSFET's: A 3-D "atomistic" simulation study ," IEEE Trans. on Elec. Dev., 45:12, pp. 2505 – 2513, Dec. 1998.
17. H. Yang, et. al, "Current mismatch due to local dopant fluctuations in MOSFET channel," IEEE Trans. on Elec. Dev., 50:11, pp. 2248-2254, Nov. 2003.
18. J. Kavalieros et. al, "Tri-Gate Transistor Architecture with High-k Gate Dielectrics, Metal Gates and Strain Engineering, 2006 Sym. VLSI Tech., pg. 50-1.
19. K. Zhang et al., "SRAM design on 65nm CMOS technology with integrated leakage reduction scheme," 2004 Sym. VLSI Cir., pp. 294-5.
20. S. Bhunia, S. Mukhopadhyay, and K. Roy, "Process Variations and Process-Tolerant Design," Int'l Conf. on VLSI Design, 2007, pp. 699 – 704 and similar.
21. K Soumyanath, S. Borkar, Z. Chunyan and B. Bloechel, "Accurate on-chip interconnect evaluation: a time-domain technique," IEEE J. of SS Cir., pp. 623-631, May 1999.
22. V. Mehrotra, "Modeling the effects of manufacturing variation on high-speed microprocessor interconnect performance," IEDM 1998, pp767-770.