A 32nm Logic Technology Featuring 2nd-Generation High-k + Metal-Gate Transistors, Enhanced Channel Strain and 0.171um^2 SRAM Cell Size in a 291Mb Array

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Logic Technology Development, *QRE, ** TCAD

Intel Corporation

Outline

- **Process Features**
- Transistors
- Interconnects
- Circuits
- Conclusions

Process Features

- 32nm Groundrules
- 193nm Immersion Lithography
- 2nd Generation High-K + Metal Gate
- 4th Generation Strained Silicon
- 9 Cu Interconnect Layers
  - Low-k CDO / SiCN dielectric
- Cu bump with Lead-free Packaging

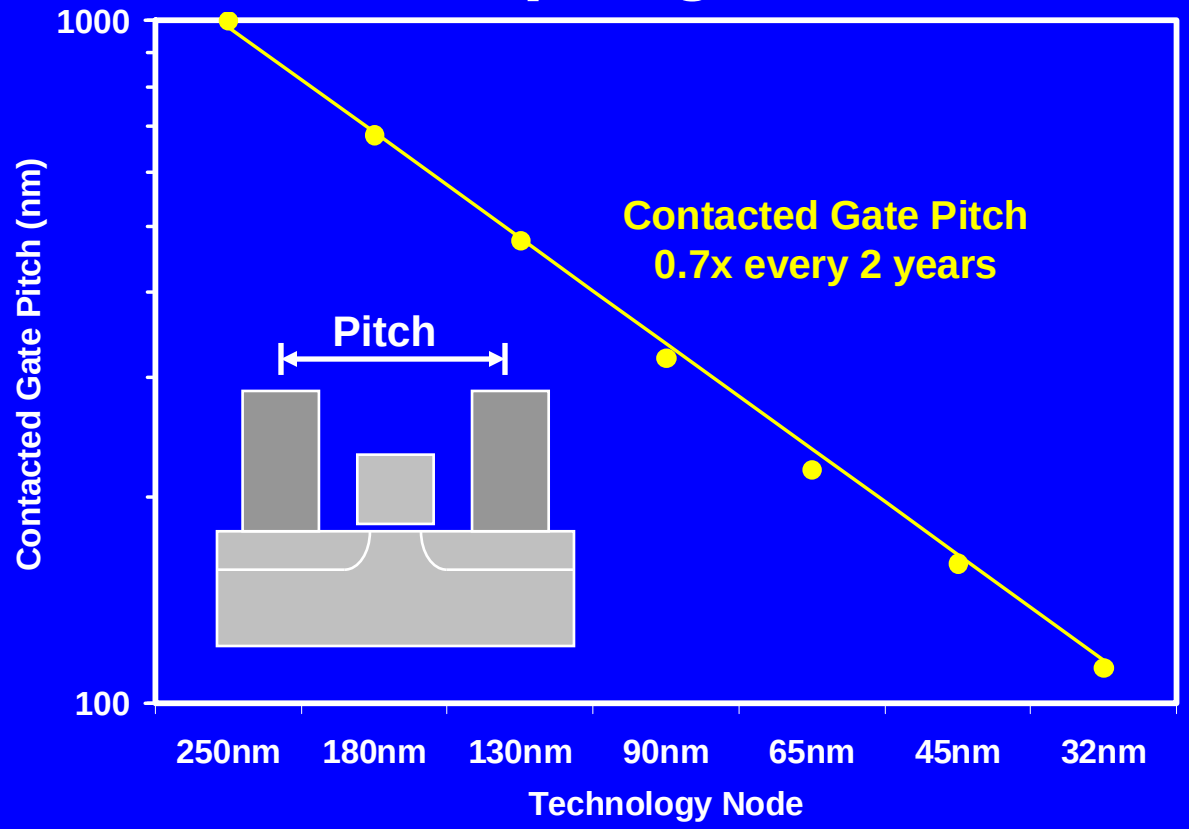
32nm Design Rules

Layer	Pitch (nm)	Thick (nm)	Aspect Ratio
Isolation	140.0	200	--
Contacted Gate	112.5	35	--
Metal 1	112.5	95	1.7
Metal 2	112.5	95	1.7
Metal 3	112.5	95	1.7
Metal 4	168.8	151	1.8
Metal 5	225.0	204	1.8
Metal 6	337.6	303	1.8
Metal 7	450.1	388	1.7
Metal 8	566.5	504	1.8
Metal 9	19.4um	8um	1.5

~0.7x linear scaling from 45nm

Contacted Gate Pitch

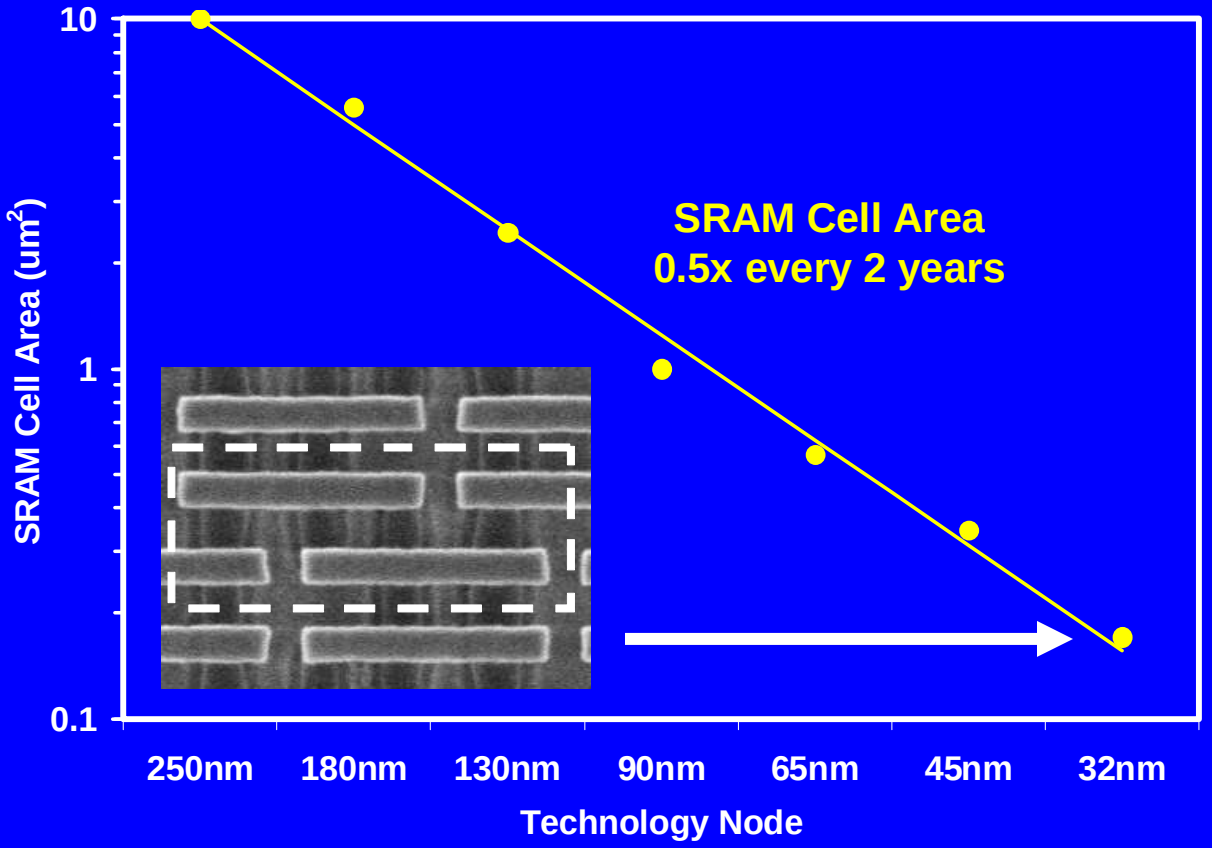
- Transistor gate pitch of 112.5nm
- Continues 0.7x per generation scaling



Tightest contacted gate pitch reported for 32nm generation

SRAM Cells

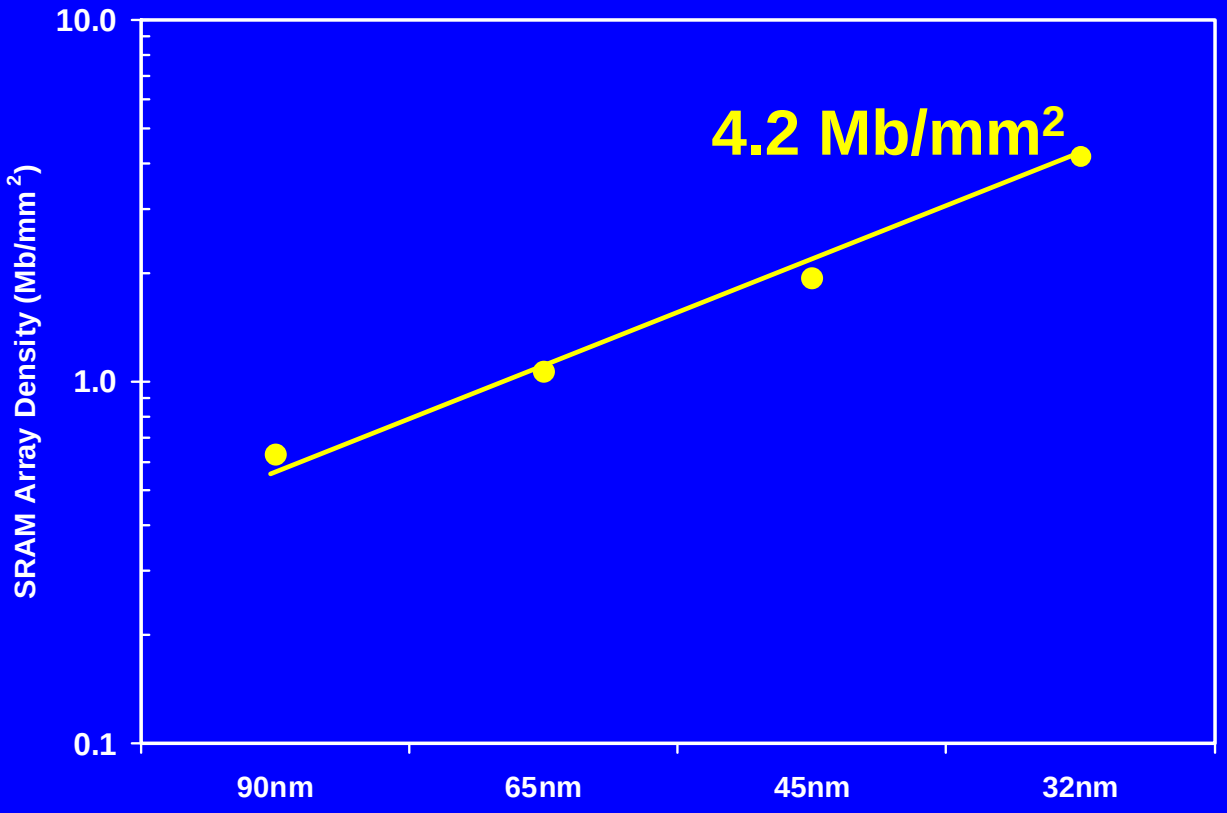
- 0.171 um^2 SRAM cell



Transistor density doubles every two years

SRAM Array Density

- SRAM array density achieves 4.2 Mb/mm^2
  - Includes row/column drivers and other circuitry



Array density scales at ~2X per generation

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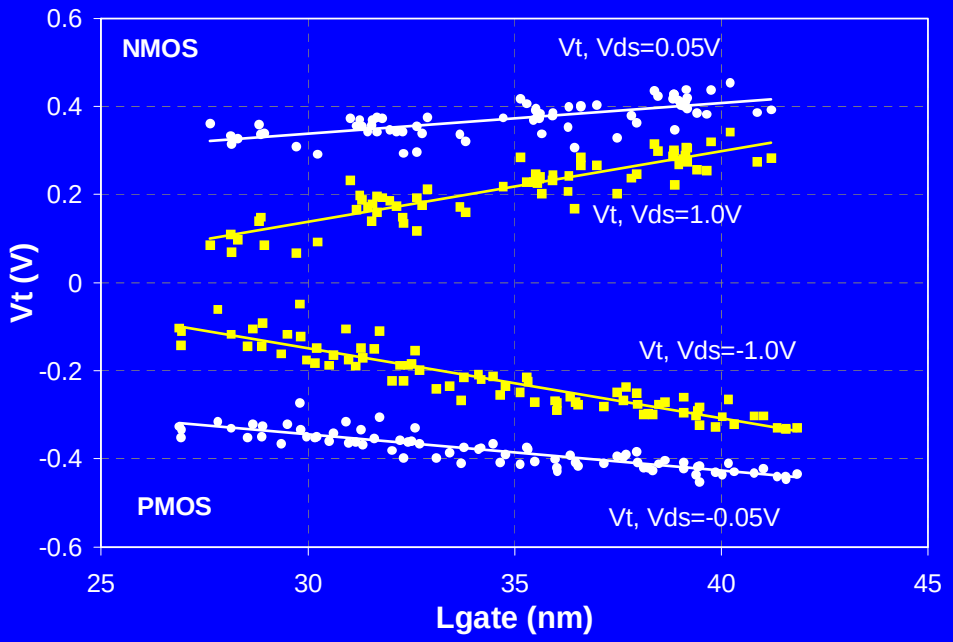
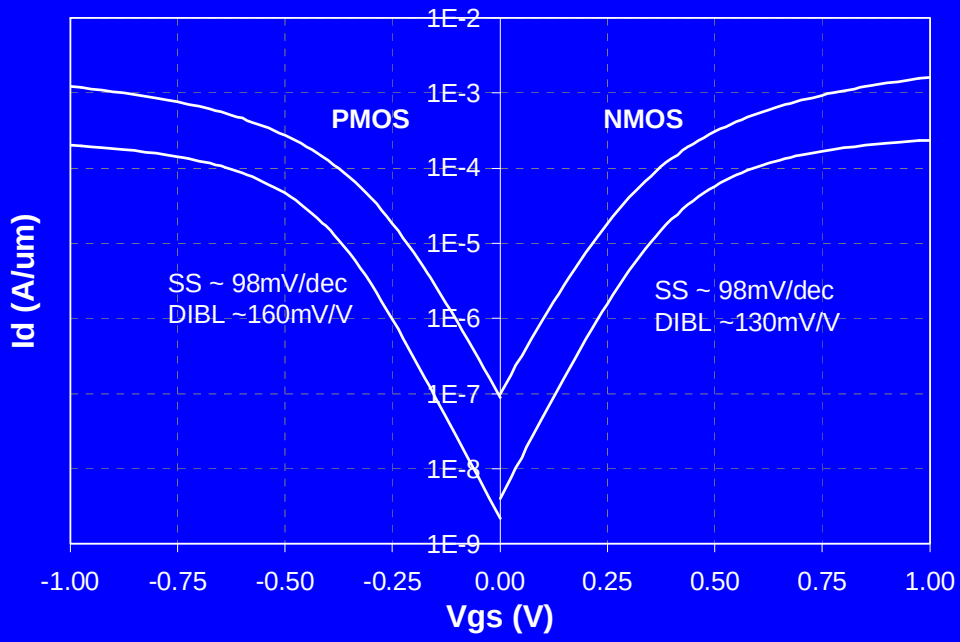
Key Transistor Features

- 30nm gate length with 112.5nm contacted gate pitch
- 2nd generation Hi-k + Metal Gate
  - 0.9nm EOT Hi-K with dual workfunction metal gate electrodes
  - Continued use of Replacement Metal Gate approach
    - Metal gate deposition after high temperature anneals
    - Integrated with strained silicon process
  - Transistor mask count same as 45nm
  - Adds ~4% process cost over non hi-k/MG
- 4th generation of strained silicon

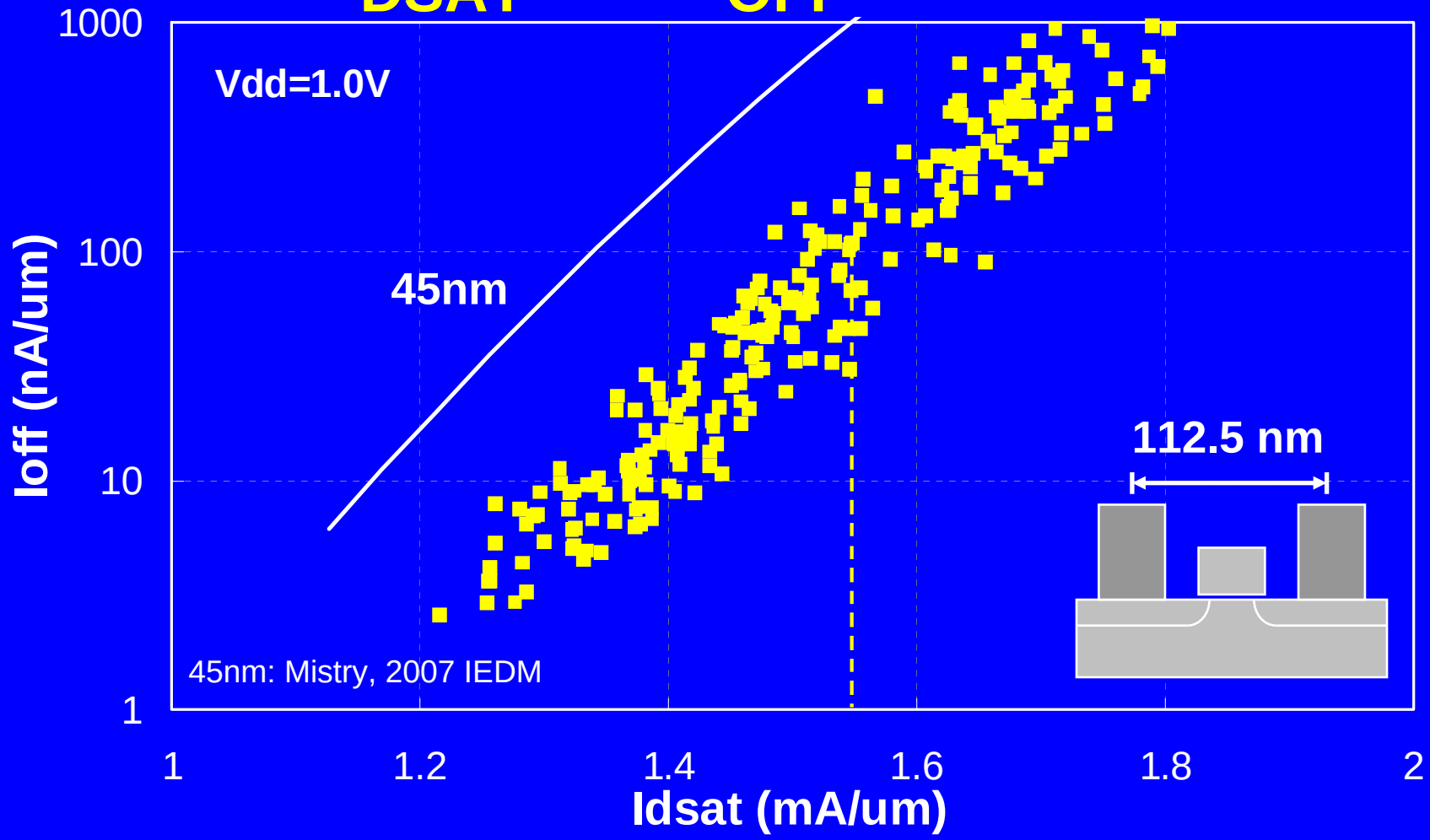
Device Characteristics





Excellent Vt roll-off and DIBL
Well controlled short channel effects
Subthreshold slope ~100 mV/decade

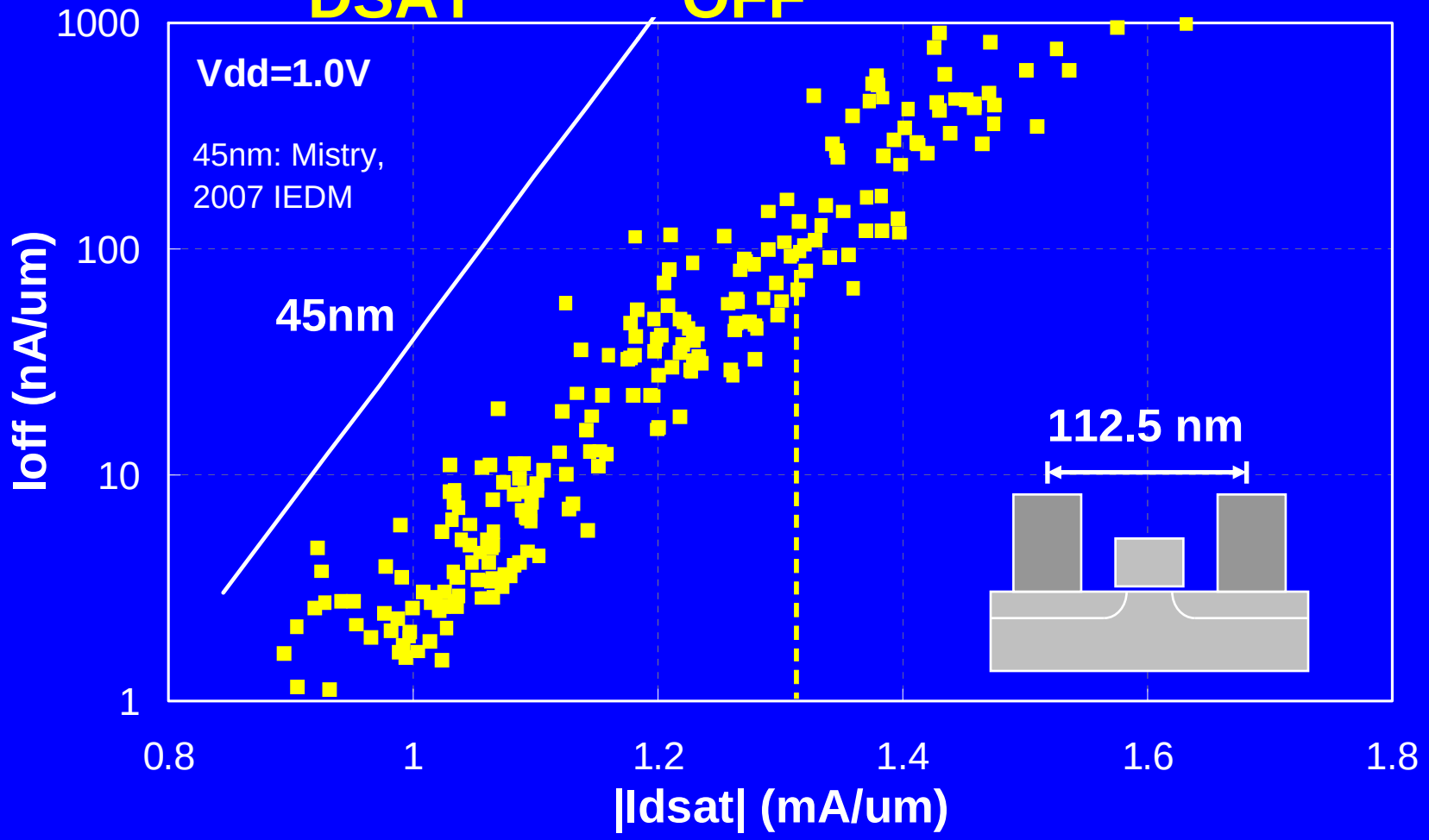
NMOS I_{DSAT} vs. I_{OFF}



1.55 mA/μm at I_{OFF} = 100 nA/μm

14% better than 45nm

PMOS I_{DSAT} vs. I_{OFF}

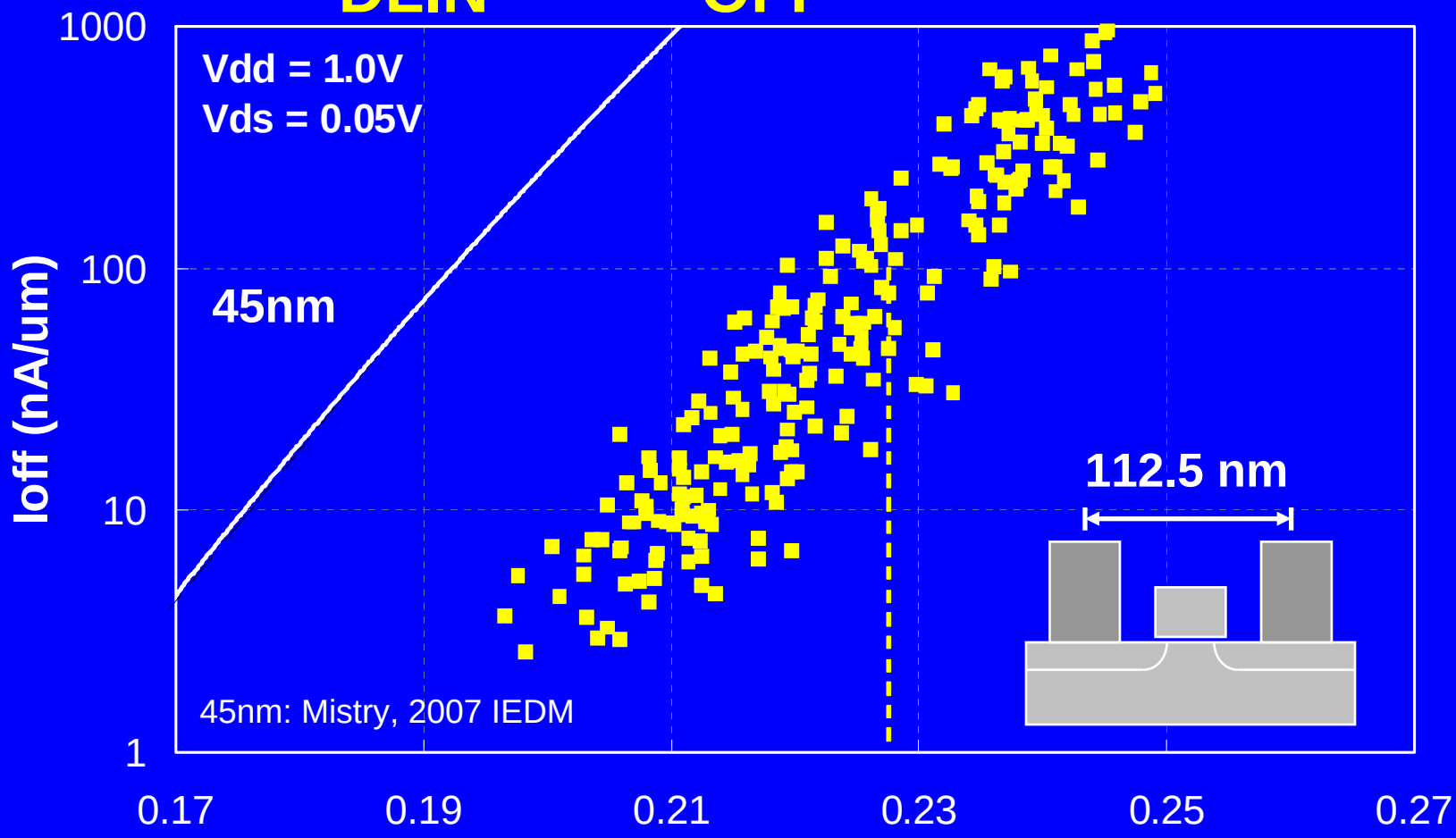


1.31 mA/μm at I_{OFF} = 100 nA/μm

22% better than 45nm

32nm PMOS Idsat almost equal to 45nm NMOS Idsat!

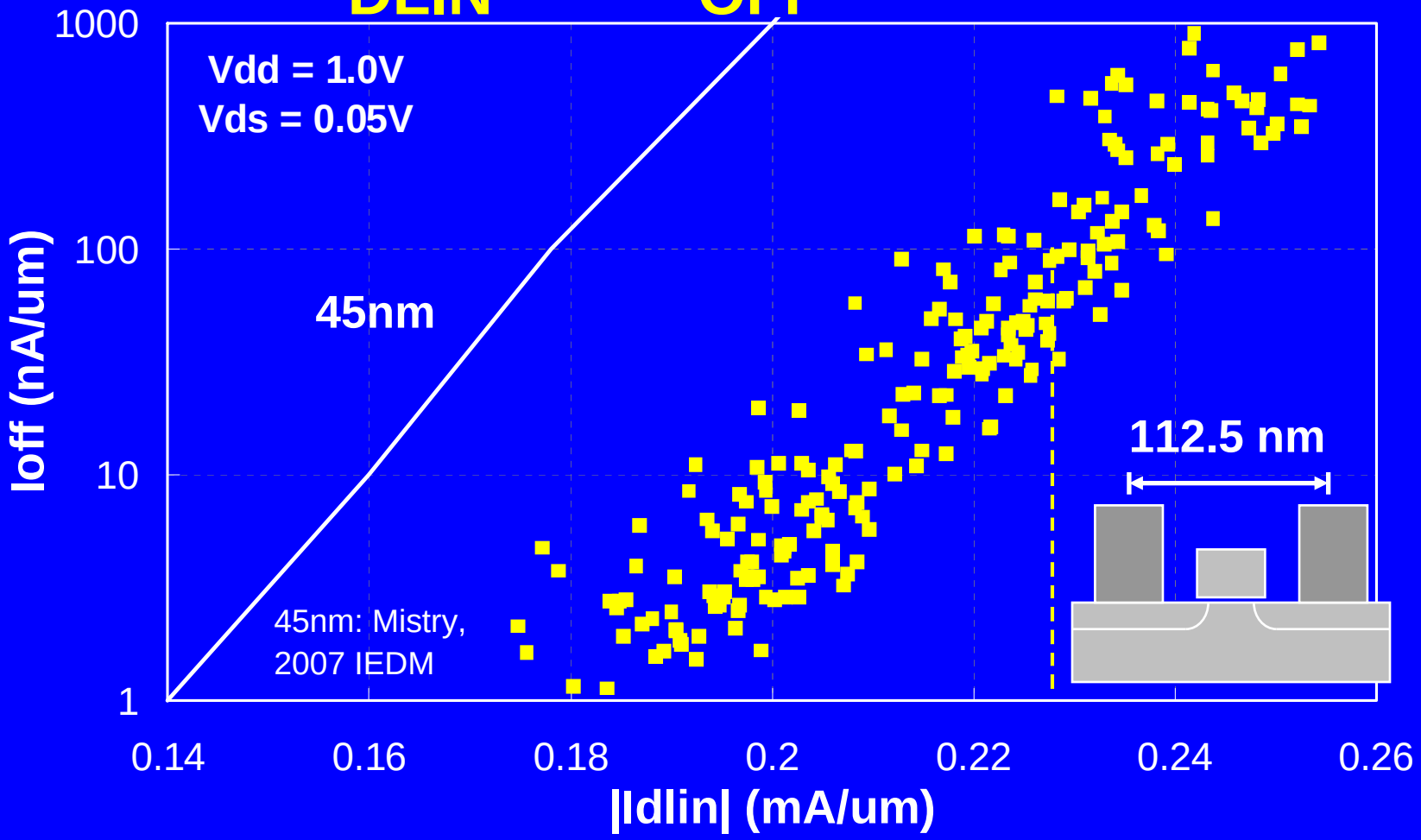
NMOS I_{DLIN} vs. I_{OFF}



0.228 mA/μm at I_{OFF} = 100 nA/μm

19% better than 45nm

PMOS I_{DLIN} vs. I_{OFF}

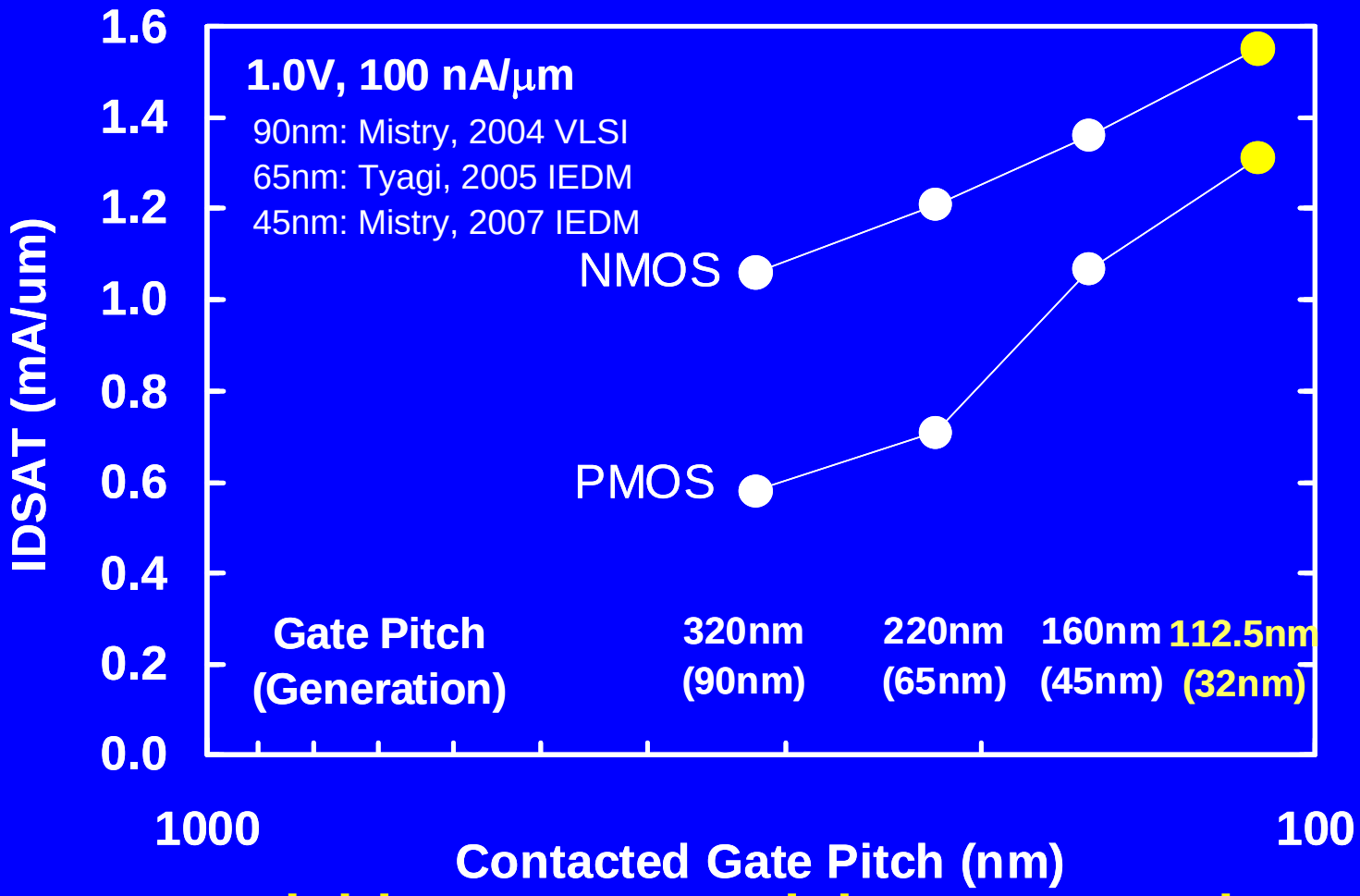


0.228 mA/μm at I_{OFF} = 100 nA/μm

28% better than 45nm

Average 20% NMOS/PMOS Sat/Lin drive current gain over 45nm

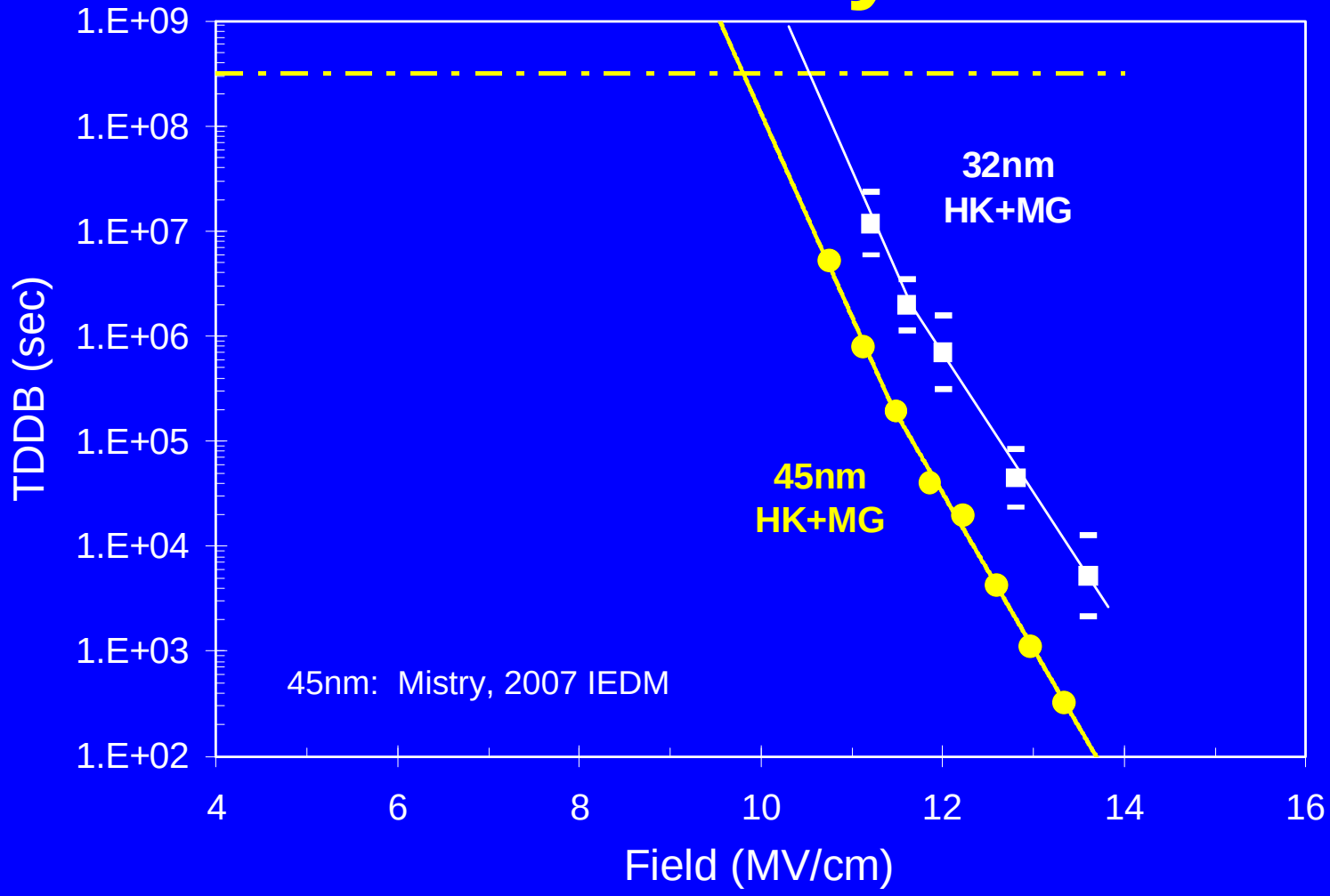
Transistor Performance vs. Gate Pitch



Highest reported drive current at tightest reported gate pitch

Simultaneous performance and density improvement

Transistor Reliability - TDDB



32nm supports 10-15% higher E-field

Enables same voltage with lower EOT

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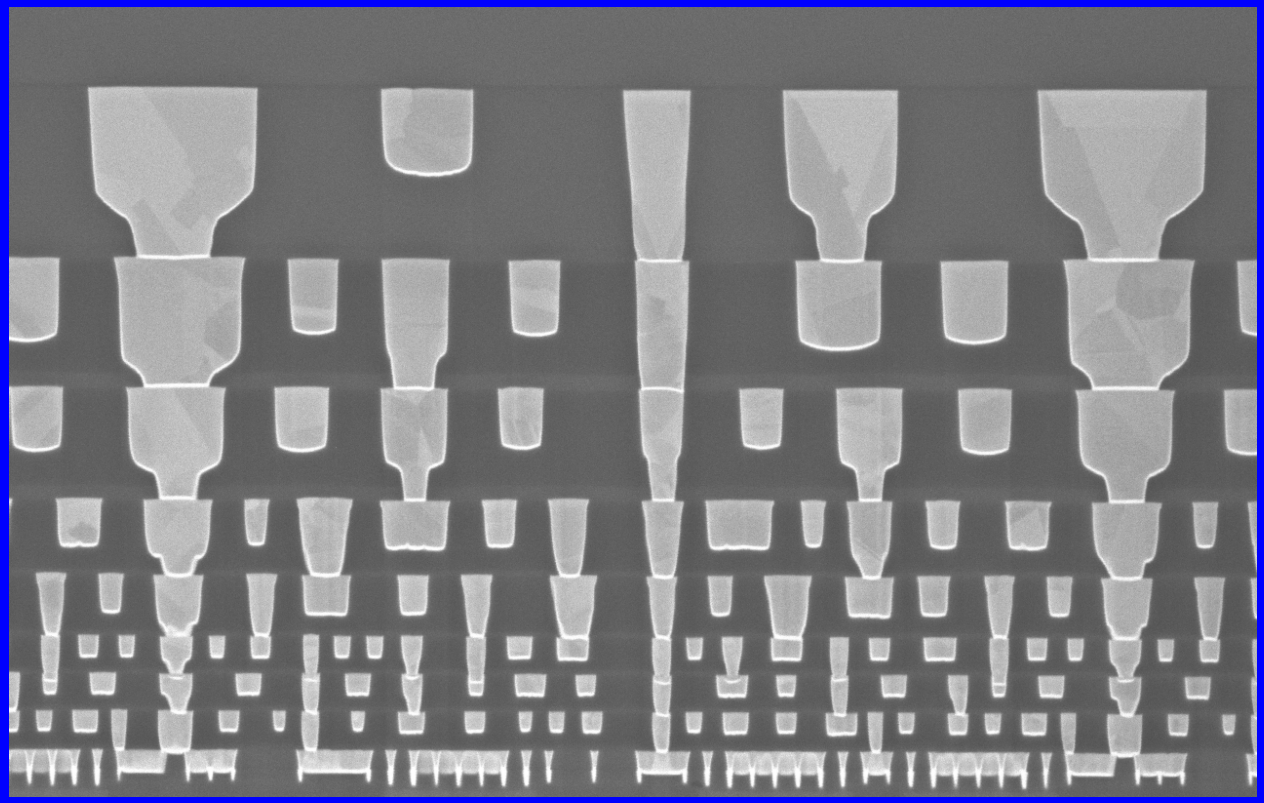
Interconnects



- Metal 1-3 pitches match transistor pitch
- Graduated upper level pitches optimize density & performance
- Extensive use of low-k ILD and SiCN

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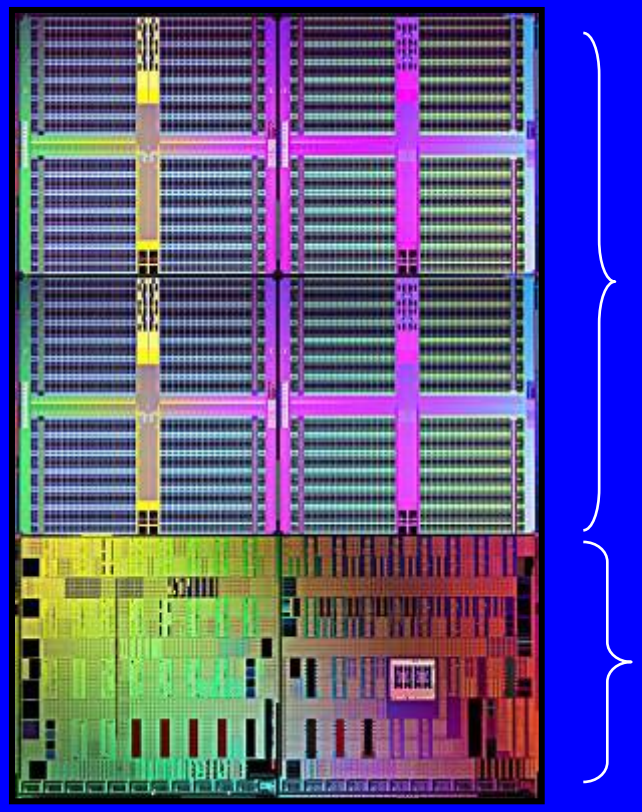
32nm Shuttle



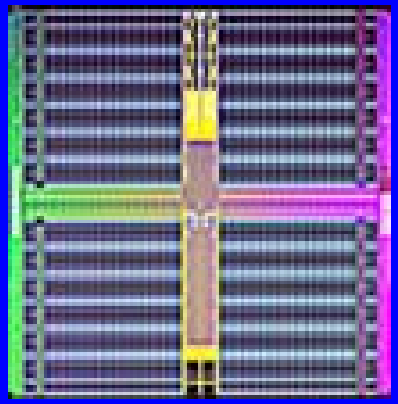
291 Mbit SRAM array
PROM array
High speed register file
High speed I/O circuits
High frequency
PLL/Clock

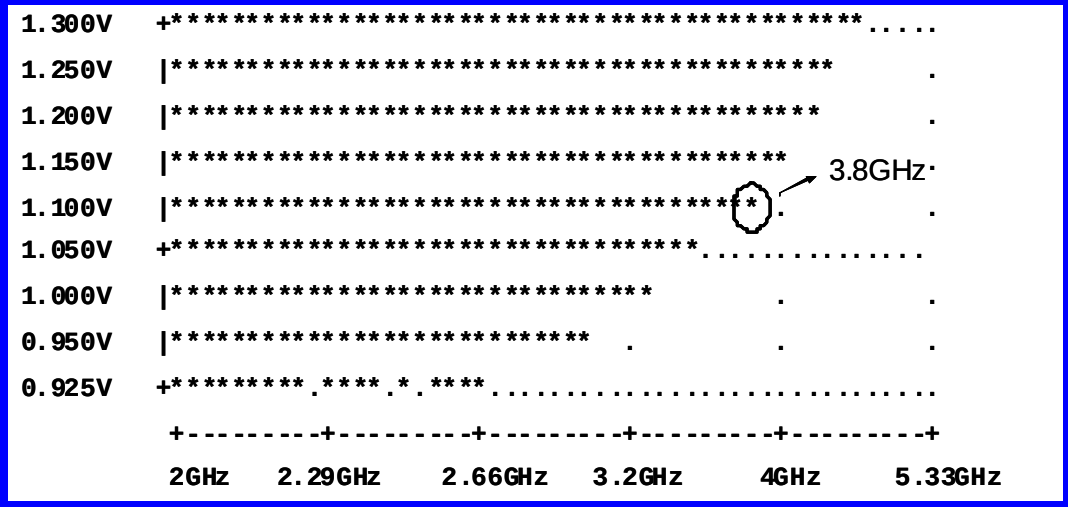
Discrete test structures

32nm shuttle with SRAM and key Logic circuits
Allows early co-optimization of process and design

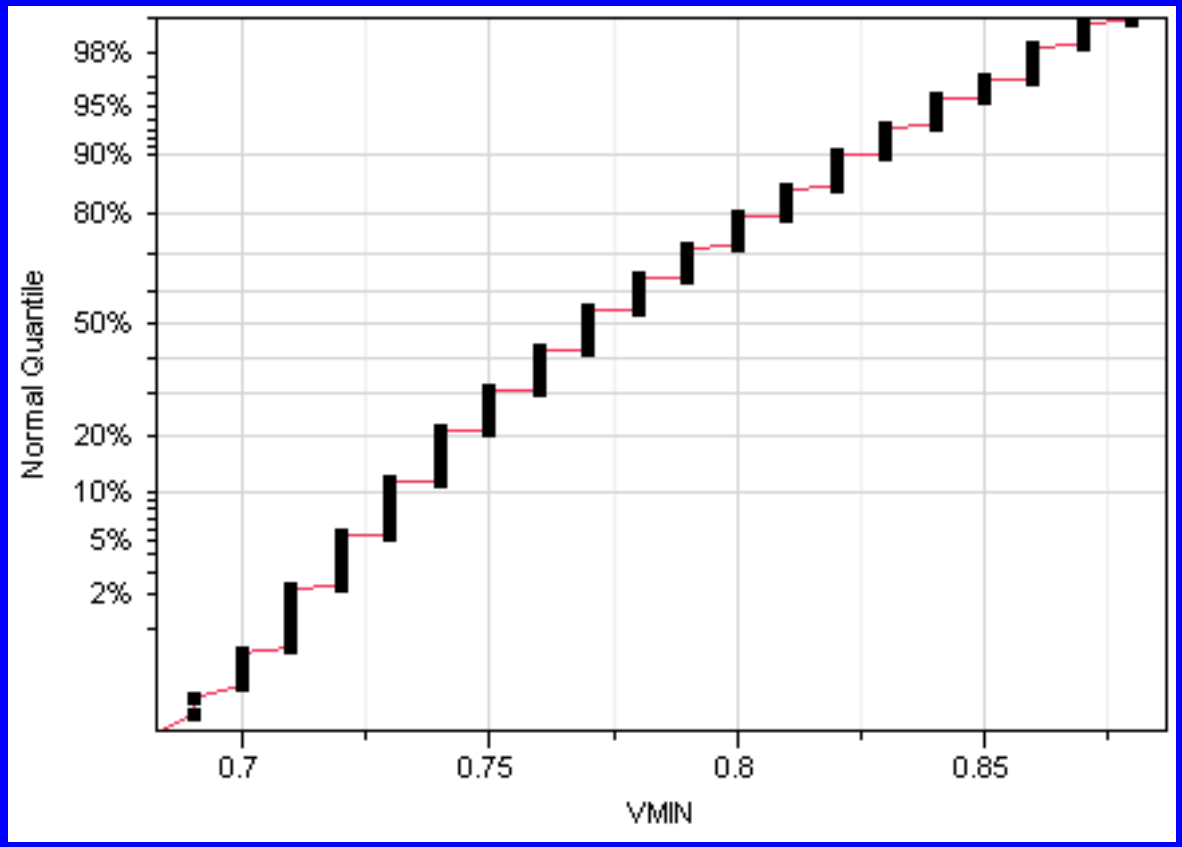
SRAM Test Vehicle

- 291 Mb, 0.171um2 SRAM Cell
  - >1.9B transistors
  - First reported functional operation in Sep '07
- Process learning vehicle demonstrates
  - High yield
  - High performance
  - Stable low voltage operation





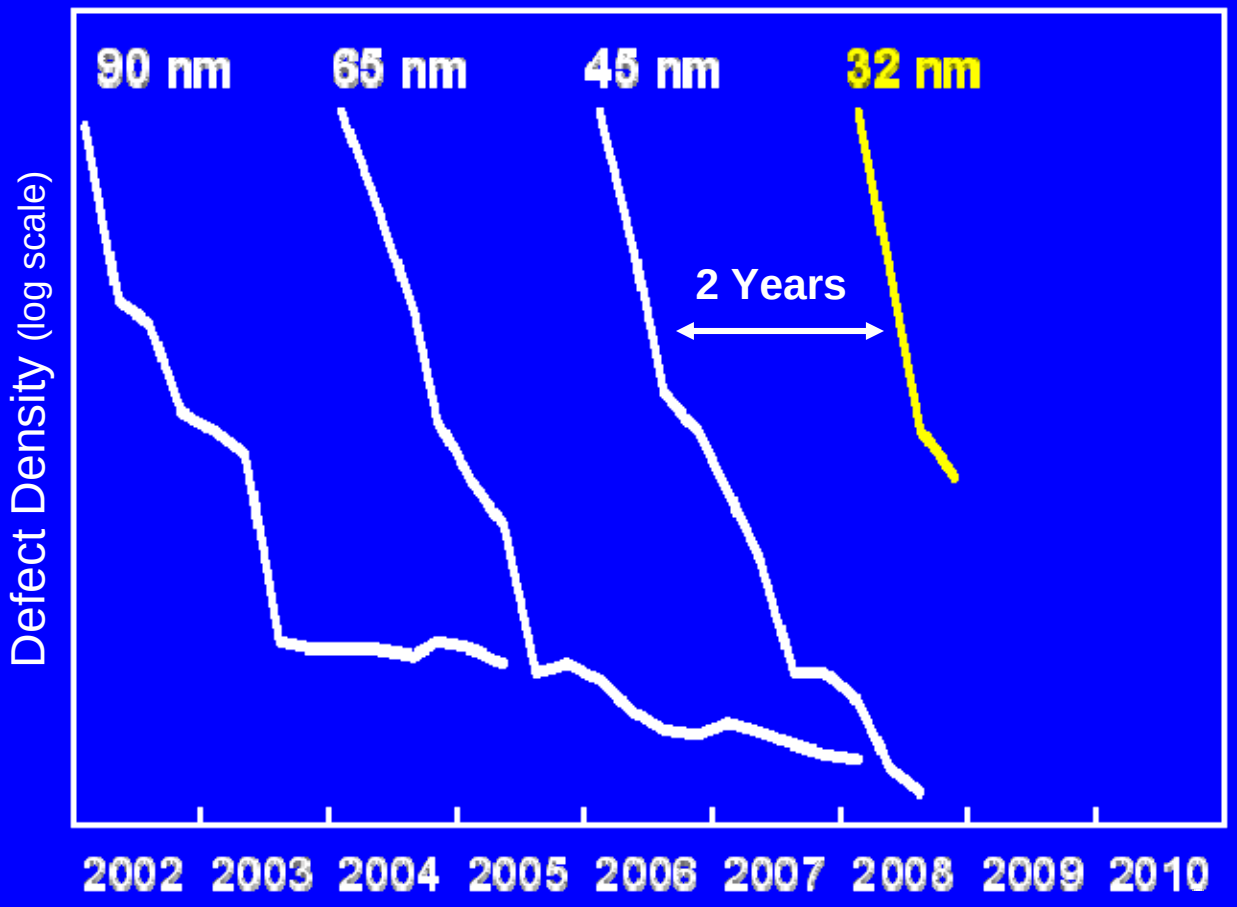
SRAM Vmin



Vmin distribution for 3.25Mb sub-arrays

Healthy 770mV median Vmin

SRAM Yield



32nm SRAM yield maintains 2-year cadence

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Conclusions

- An industry leading 32nm logic technology is presented
- Continues Moore's law relative to 45nm:
  - 0.7x contacted gate pitch scaling
  - 0.5x SRAM cell size scaling
  - 2.2x array density scaling
- Record linear and saturated transistor drive currents achieved
  - Average of 20% improvement in drive current over 45nm
- Healthy yield achieved on 291Mb SRAM with 0.171 um^2 SRAM cell size and excellent low voltage operation
- Completed development phase on 32nm CMOS
  - On track for production readiness in H2'09

Acknowledgements

- The authors gratefully acknowledge the many people in the following organizations at Intel who contributed to this work:
  - Logic Technology Development
  - Quality and Reliability Engineering
  - Technology CAD
  - Assembly & Test Technology Development

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