High Performance High-K + Metal Gate Strain Enhanced Transistors on (110) Silicon

Paul Packan, S. Cea*, H. Deshpande, T. Ghani, M. Giles*, O. Golonzka, M. Hattendorf, R. Kotlyar*, K. Kuhn, A. Murthy, P. Ranade, L. Shifren*, C. Weber* and K. Zawadzki

Logic Technology Development, *Process Technology Modeling

Intel Corporation

IEDM 2008

Outline

- Transistor Scaling
- Stress Effects on Mobility
- Comparison of (100) and (110) Silicon Substrates
- Device Performance
- Summary

Key Messages

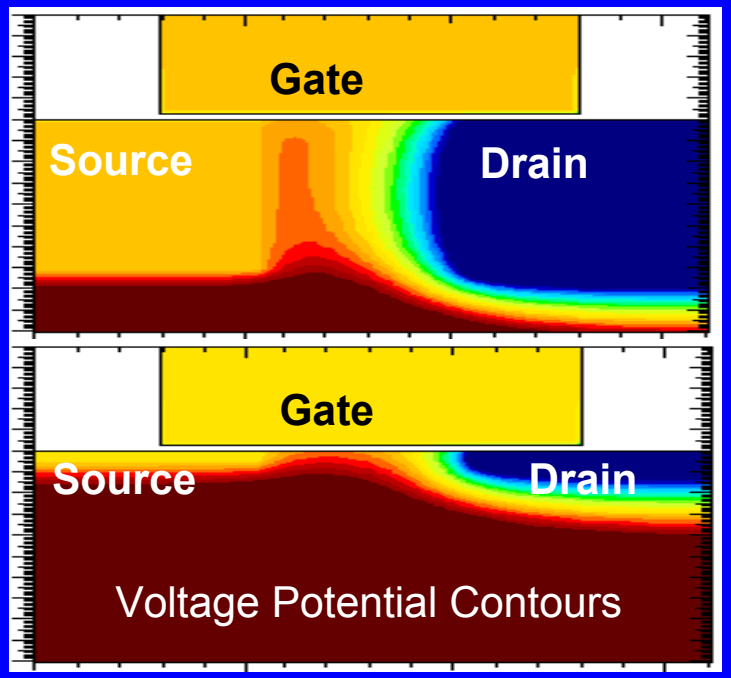
- Record PMOS drive current of 1.2mA/um is presented for devices on (110) silicon substrates
- For short gate lengths, NMOS drive currents on (110) substrates are not degraded as much as believed by many in literature
- The fundamental physics behind these behaviors is understood

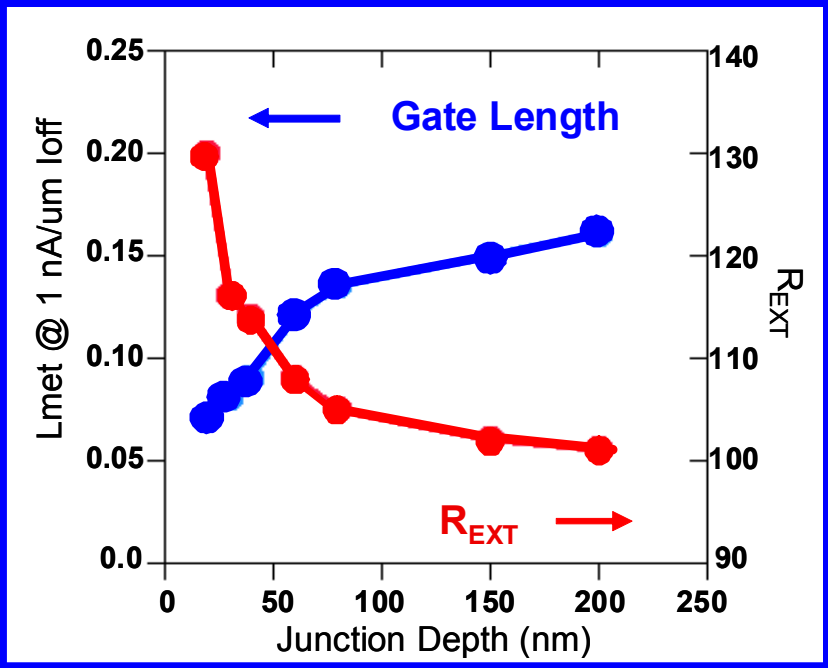
Outline

- **Transistor Scaling**
- Stress Effects on Mobility
- Comparison of (100) and (110) Silicon Substrates
- Device Performance
- Summary

Traditional Scaling

$Id=\mu Cox/Le(Vg-Vt)^{\alpha}$

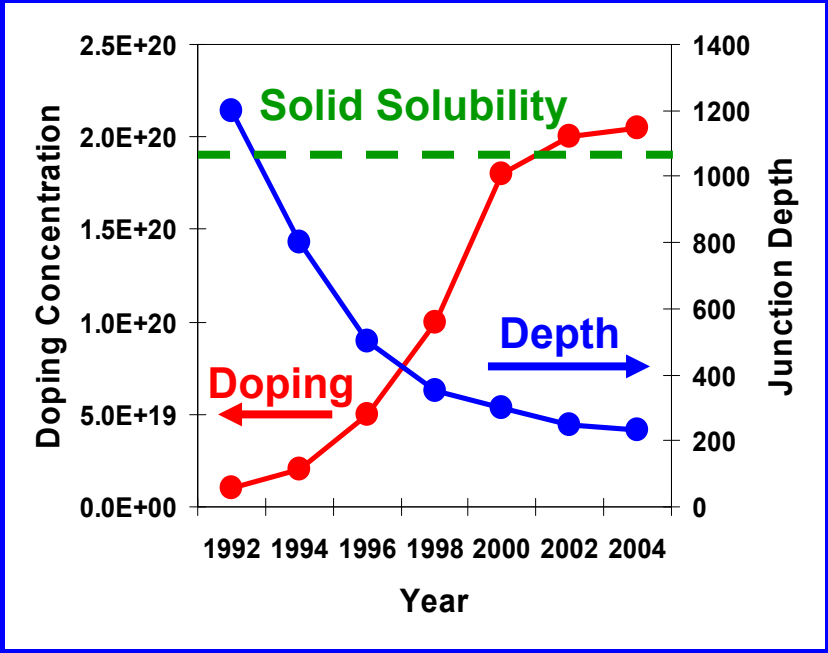


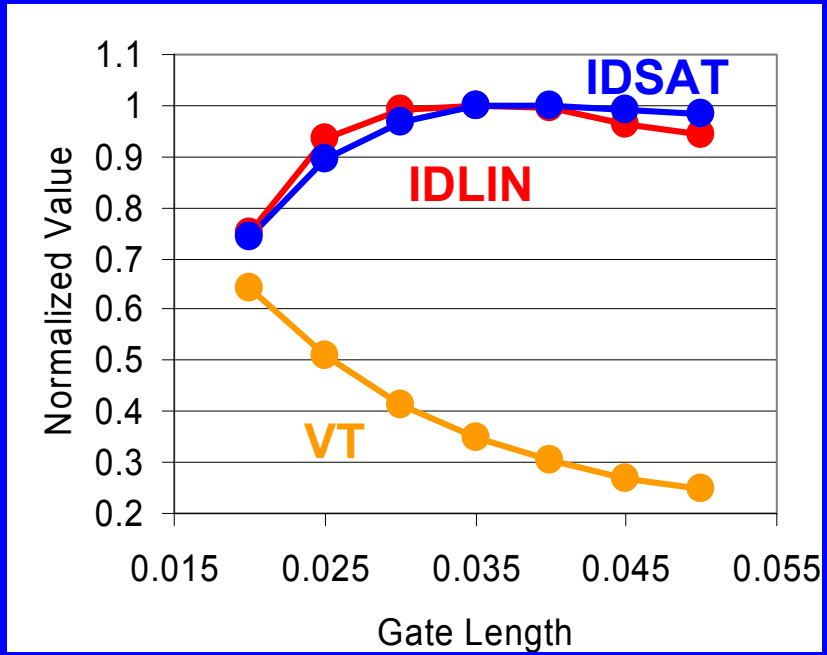


- Traditional device scaling requires all dimensions to scale to maintain performance and leakage
- Scaling junction depths and S/D areas is causing Rext increase

Constant Leakage Scaling

$Id=\mu Cox/Le(Vg-Vt)^{\alpha}$



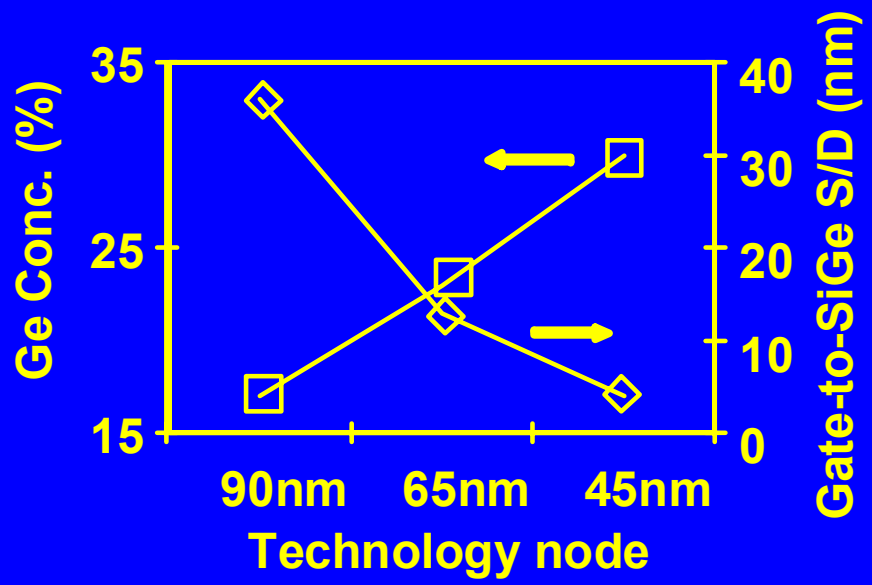


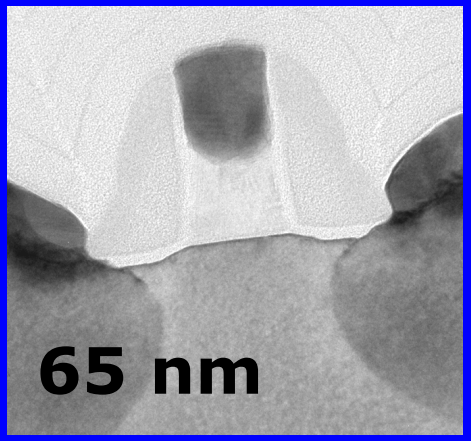
- Junction scaling is slowing due to unacceptable resistance increases
- Scaling gate lengths at constant leakage requires increasing Vt which results in drive current reduction
- Traditional device scaling is losing steam

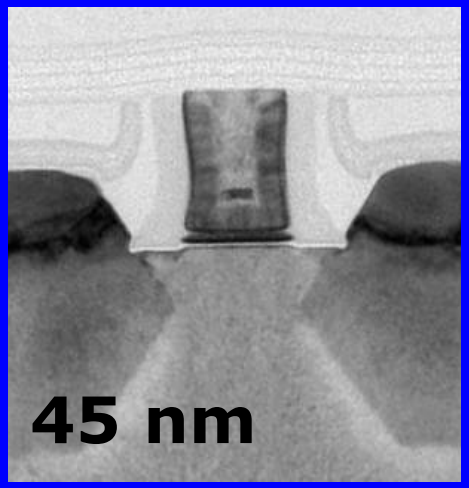
Mobility Scaling

$$Id=\mu Cox/Le(Vg-Vt)^{\alpha}$$

- Increasing mobility increases device performance without increasing leakage
- Reducing scattering mechanisms, applying stress and surface orientation all affect mobility



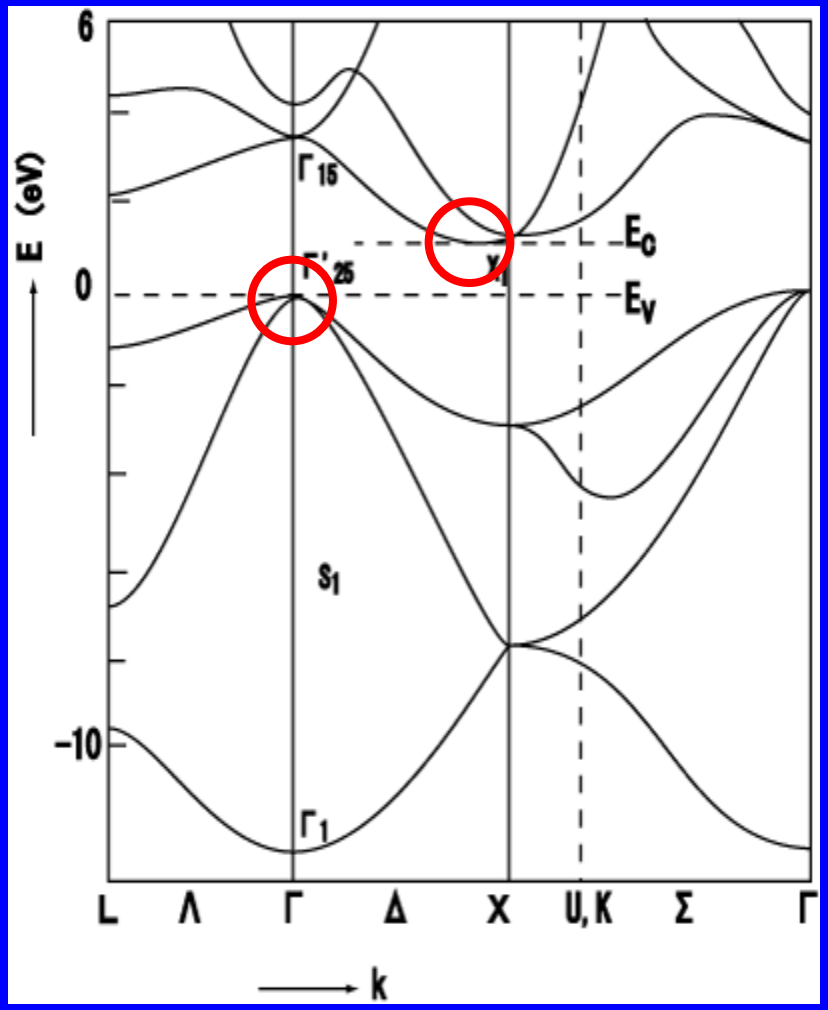




Outline

- Transistor Scaling
- **Stress Effects on Mobility**
- Comparison of (100) and (110) Silicon Substrates
- Device Performance
- Summary

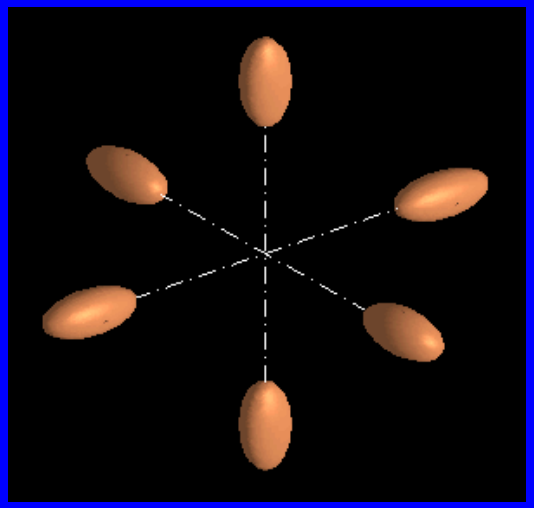
Silicon Band Structure



conduction band for electrons

gap

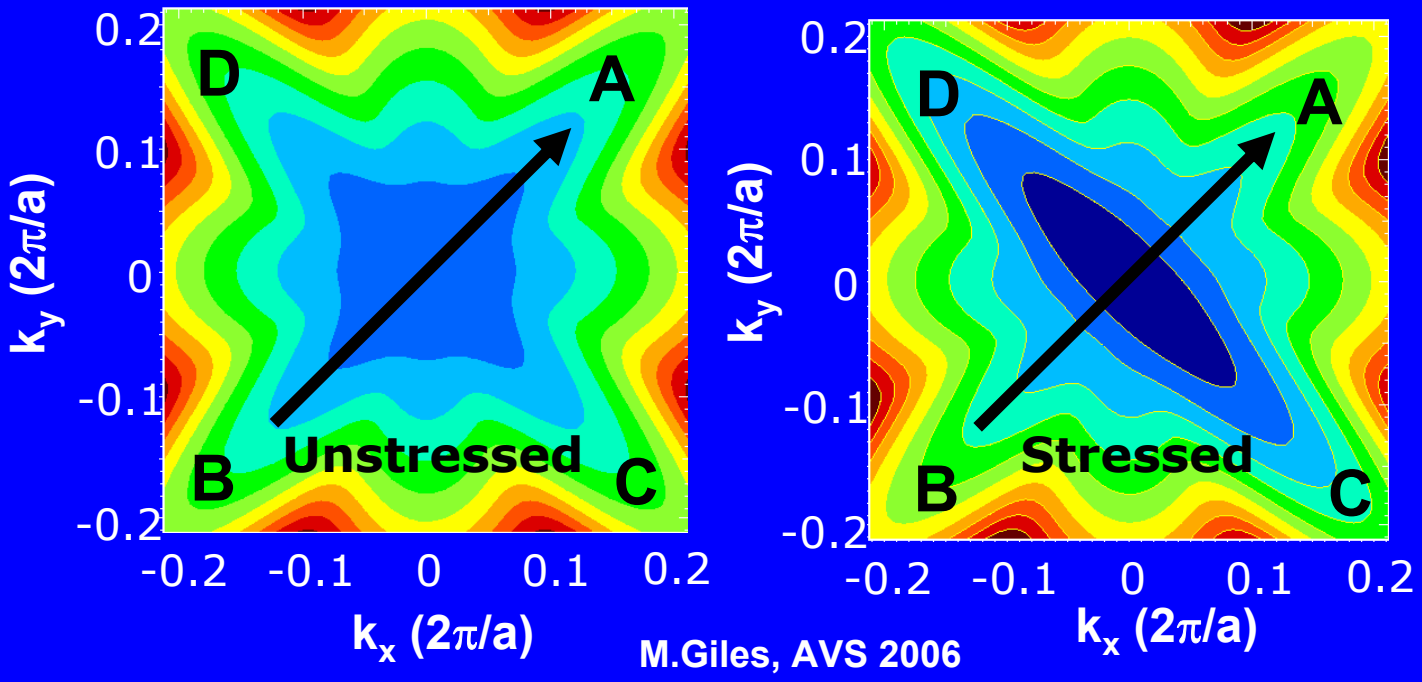
valence band for holes



Electron

Hole

Stress and Band Structure



M.Giles, AVS 2006

(001) surface

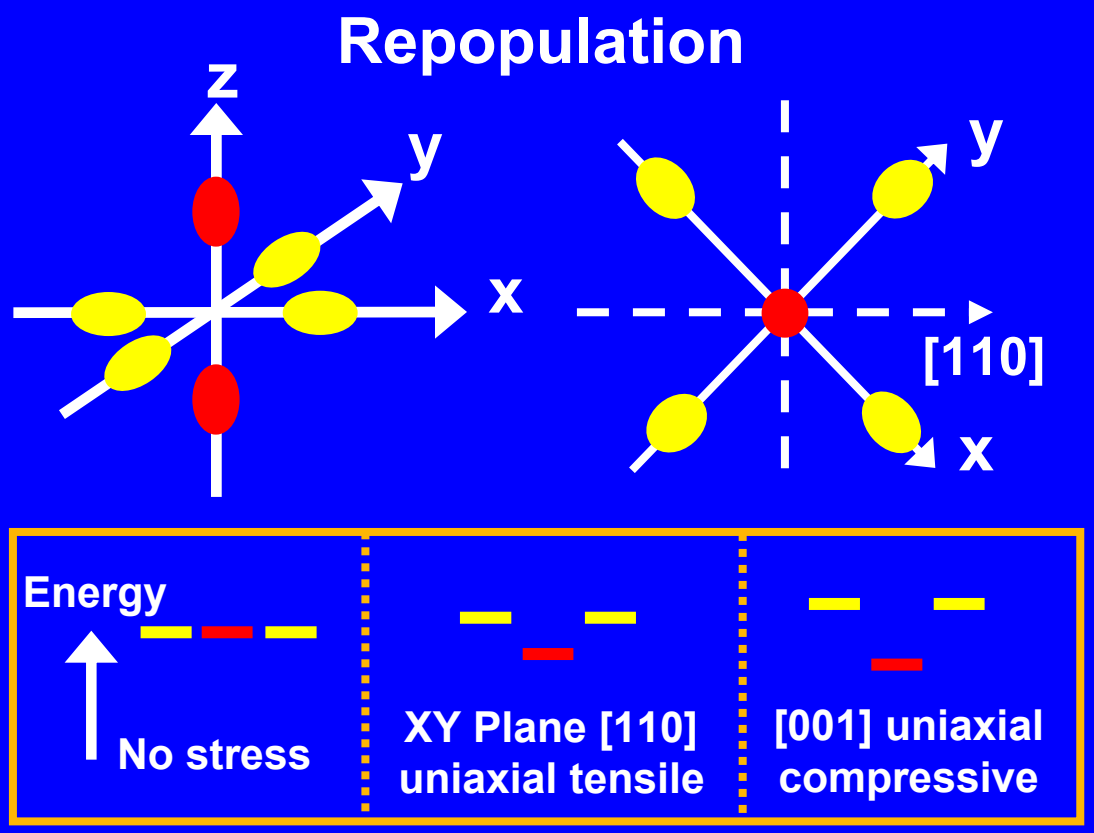
1GPa uniaxial stress [110]

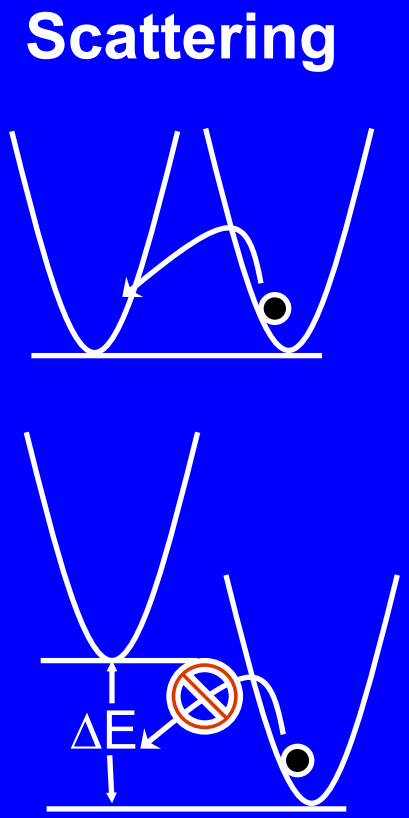
1 MV/cm vertical field

30meV energy contours

- Compression lowers the energy of (C,D)
- Holes redistribute from (A,B) to (C,D)
- The effective mass is reduced

Conduction Band Stress Response

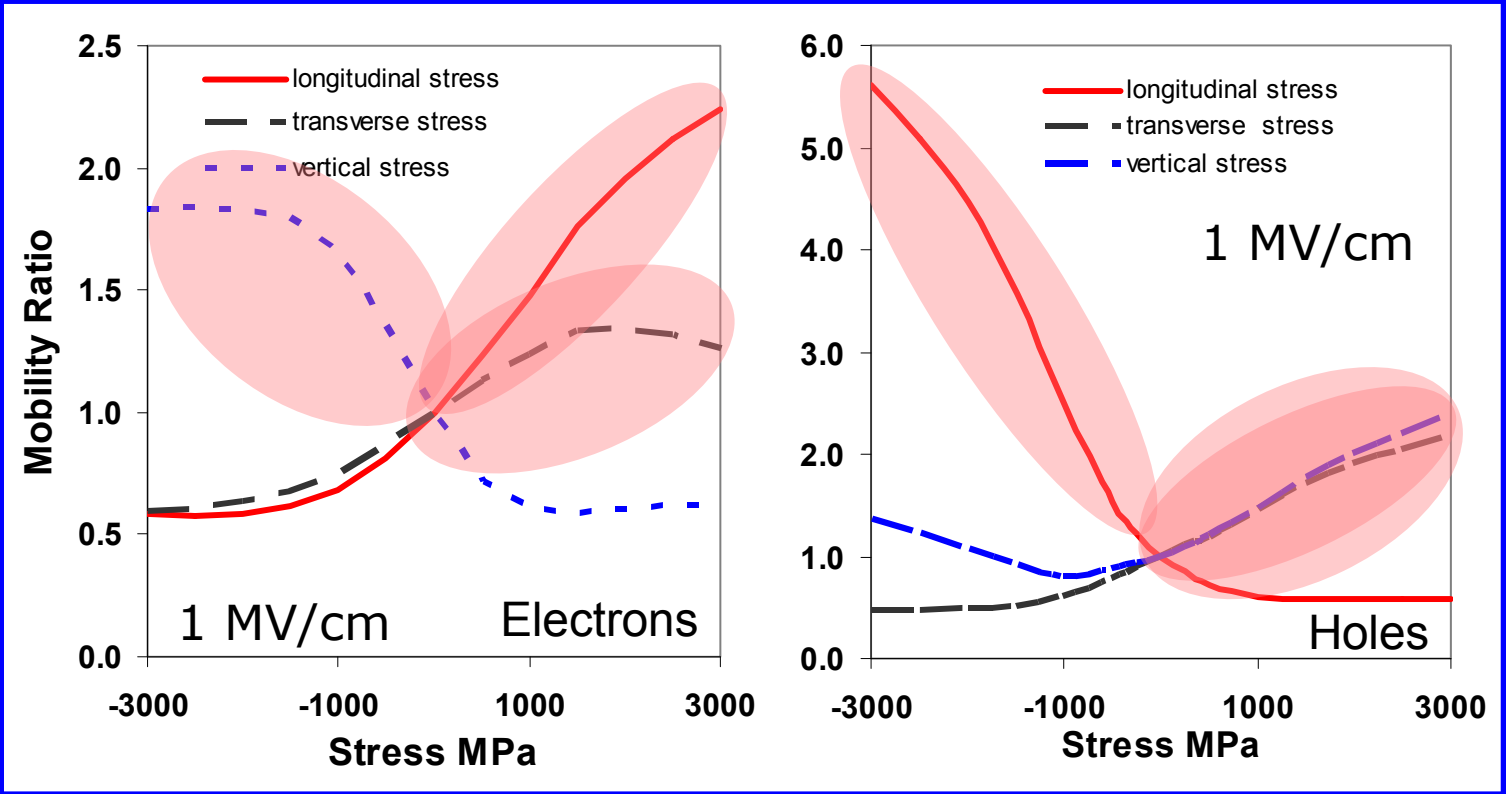




M.Giles, AVS 2006

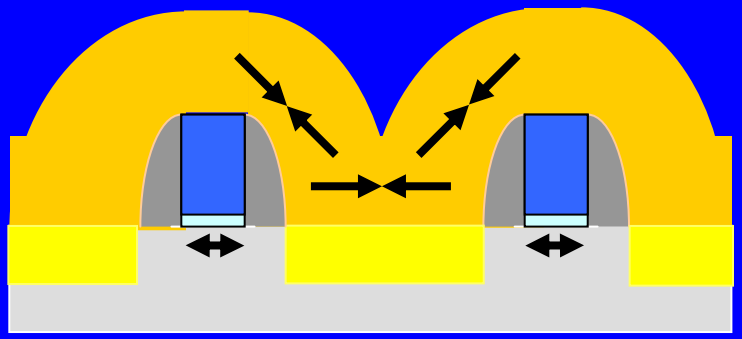
Mobility gain comes from valley repopulation, valley warping, and scattering suppression

Stress Effects on Mobility

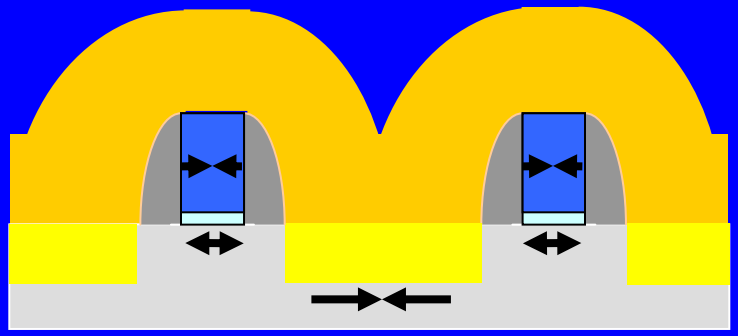


- Longitudinal tension and vertical compression increases electron mobility
- Longitudinal compression and vertical tension increases hole mobility
- Transverse tension increases both electron and hole mobility
- Hole mobility shows a greater sensitivity to stress for (100)

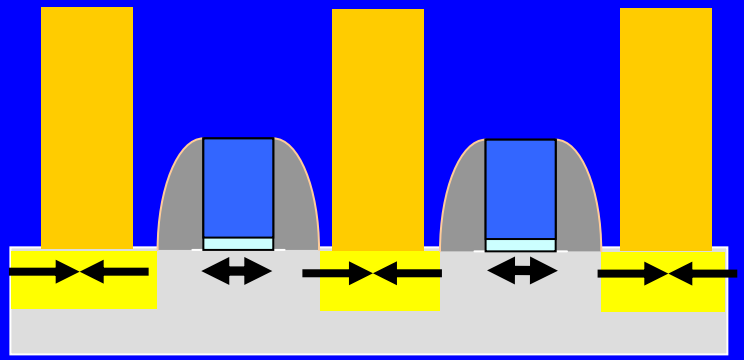
Stress Methods



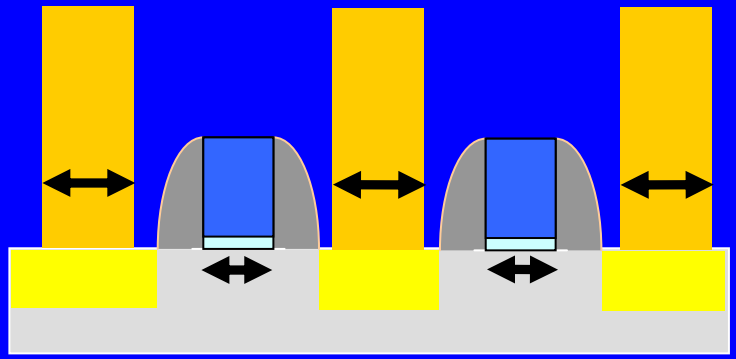
Capping Layers



Gate Induced



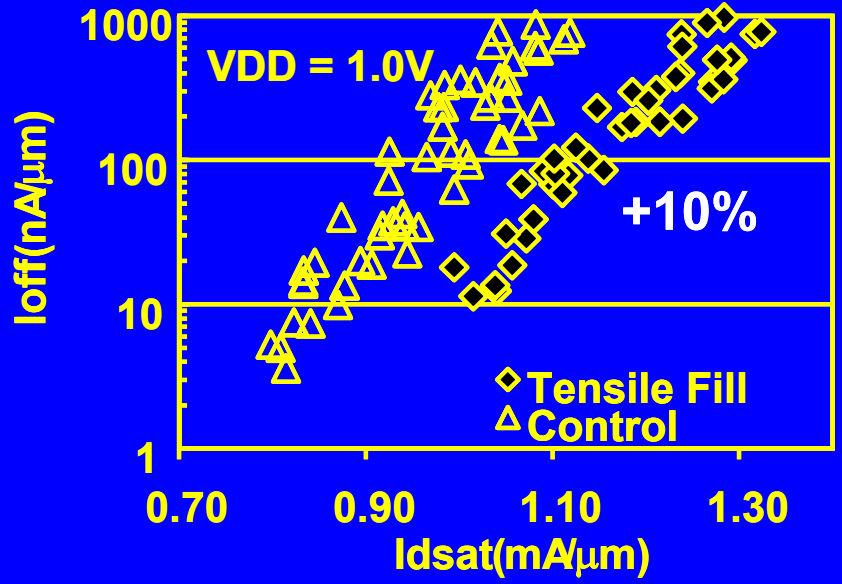
Epitaxial Layers

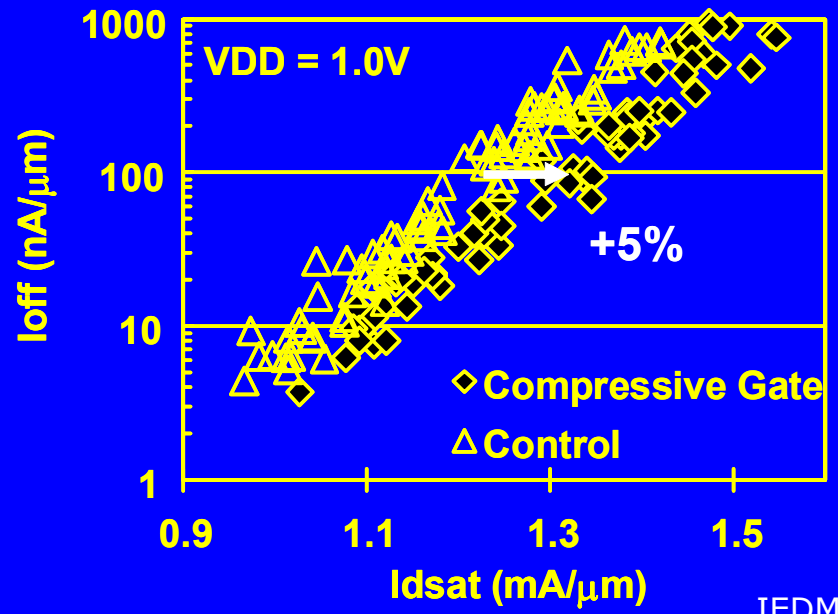


Contacts

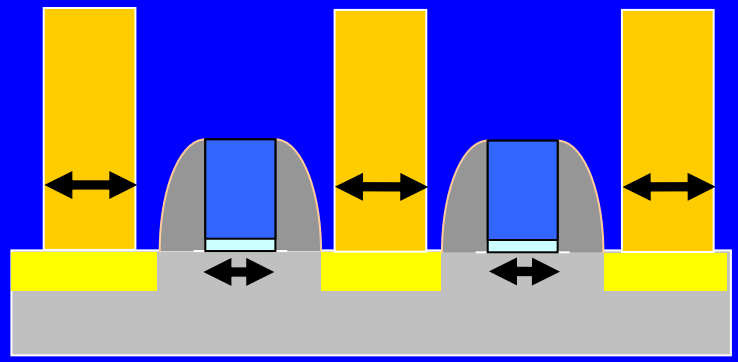
C. Auth, VLSI 2008

NMOS Stress

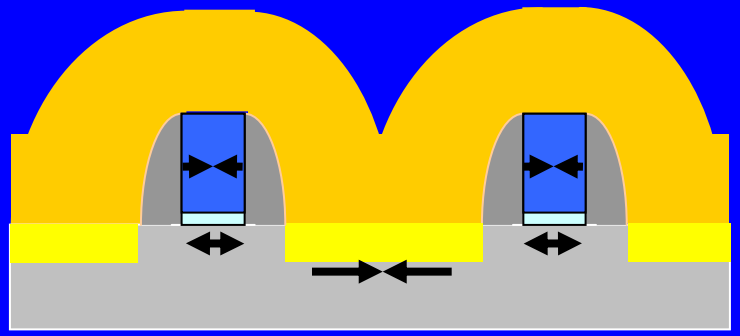




Contact Stress

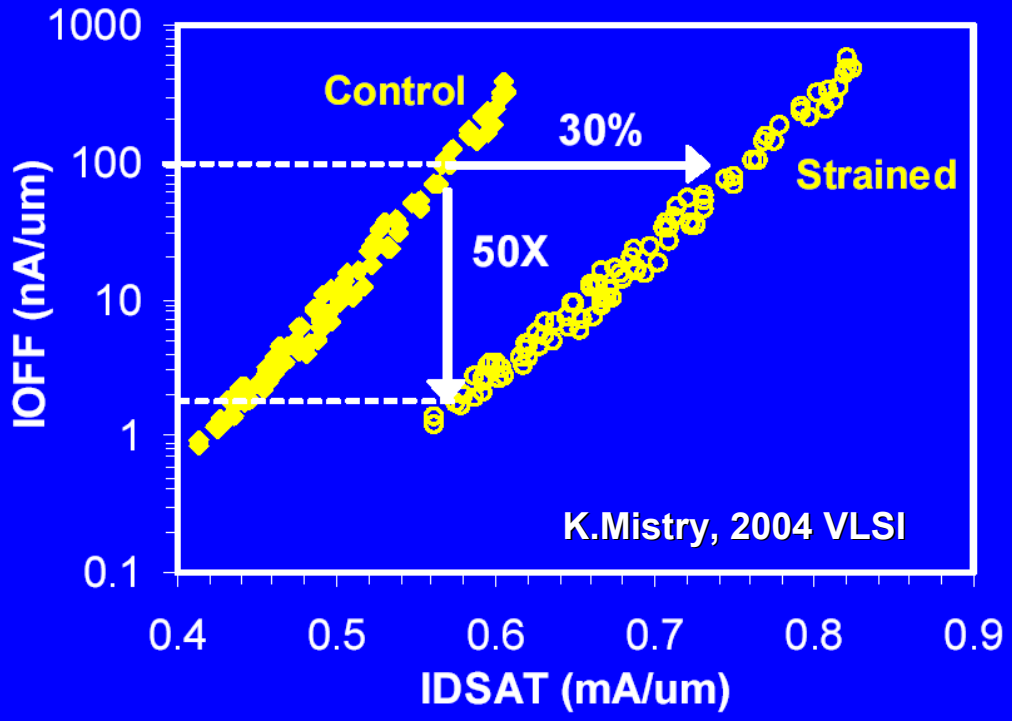


Gate Stress

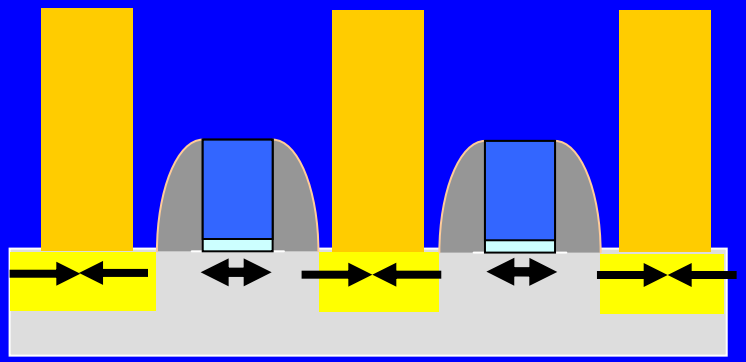


C. Auth, VLSI 2008

PMOS Stress



SiGe Stress

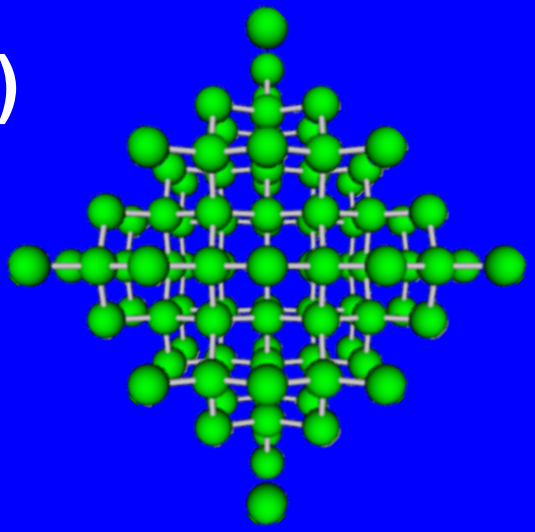


Outline

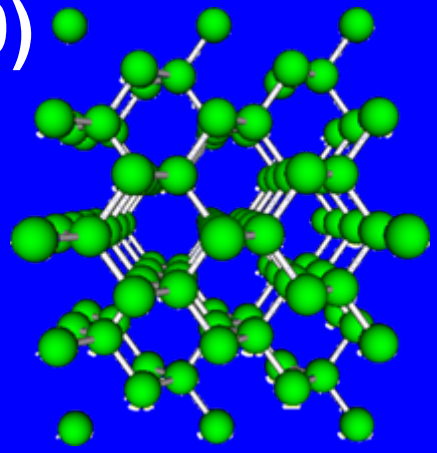
- Transistor Scaling
- Stress Effects on Mobility
- **Comparison of (100) and (110) Silicon Substrates**
- Device Performance
- Summary

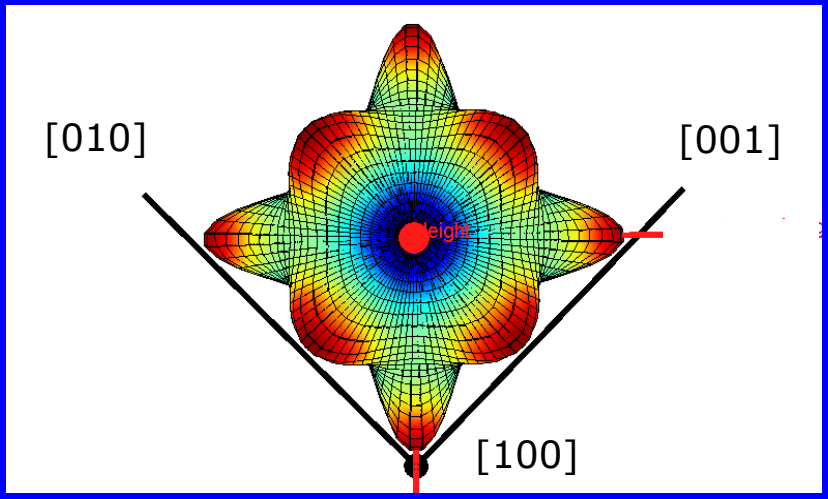
Substrate Orientation

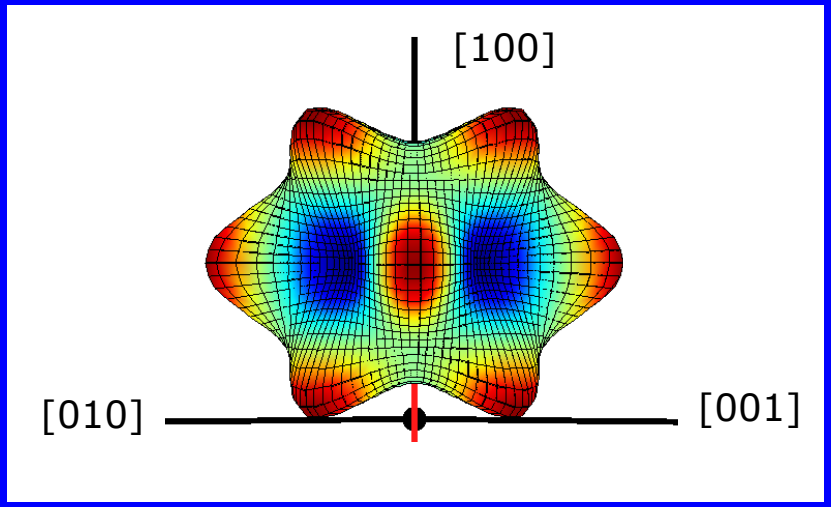
(100)



(110)

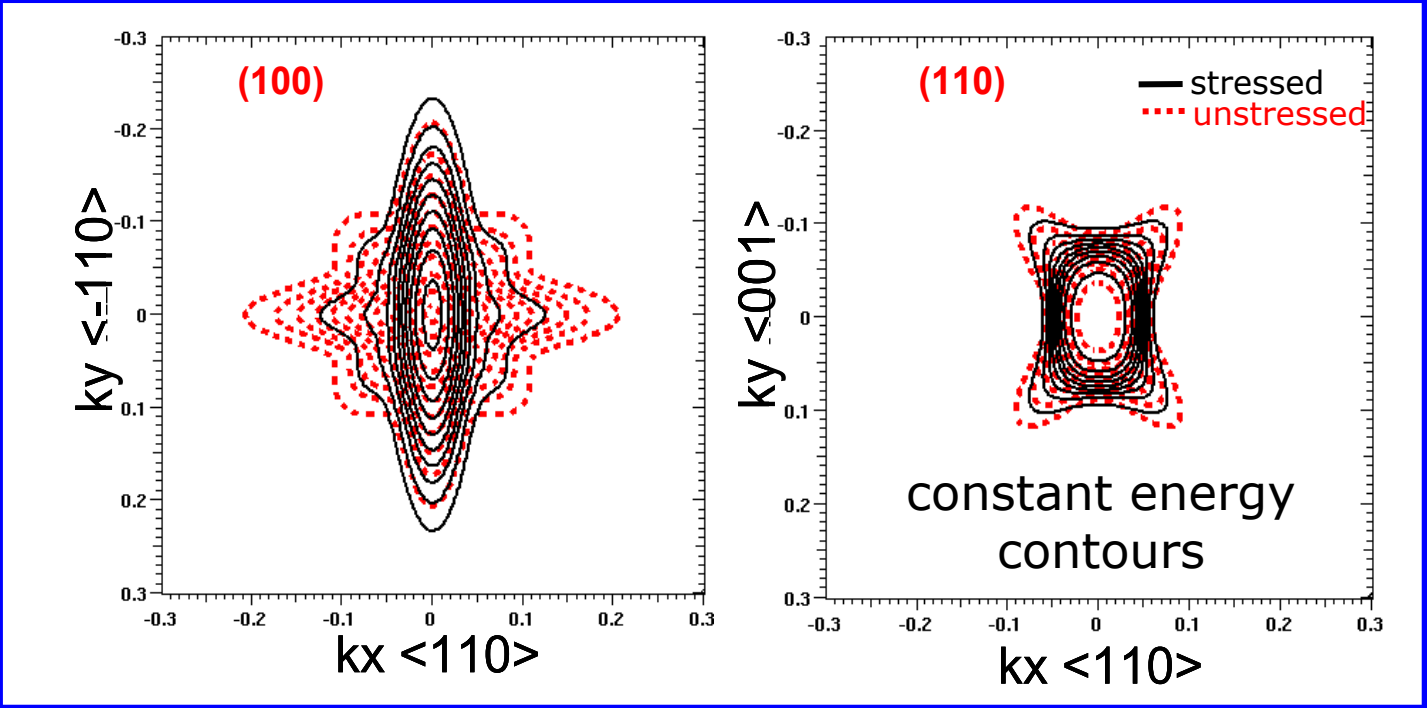






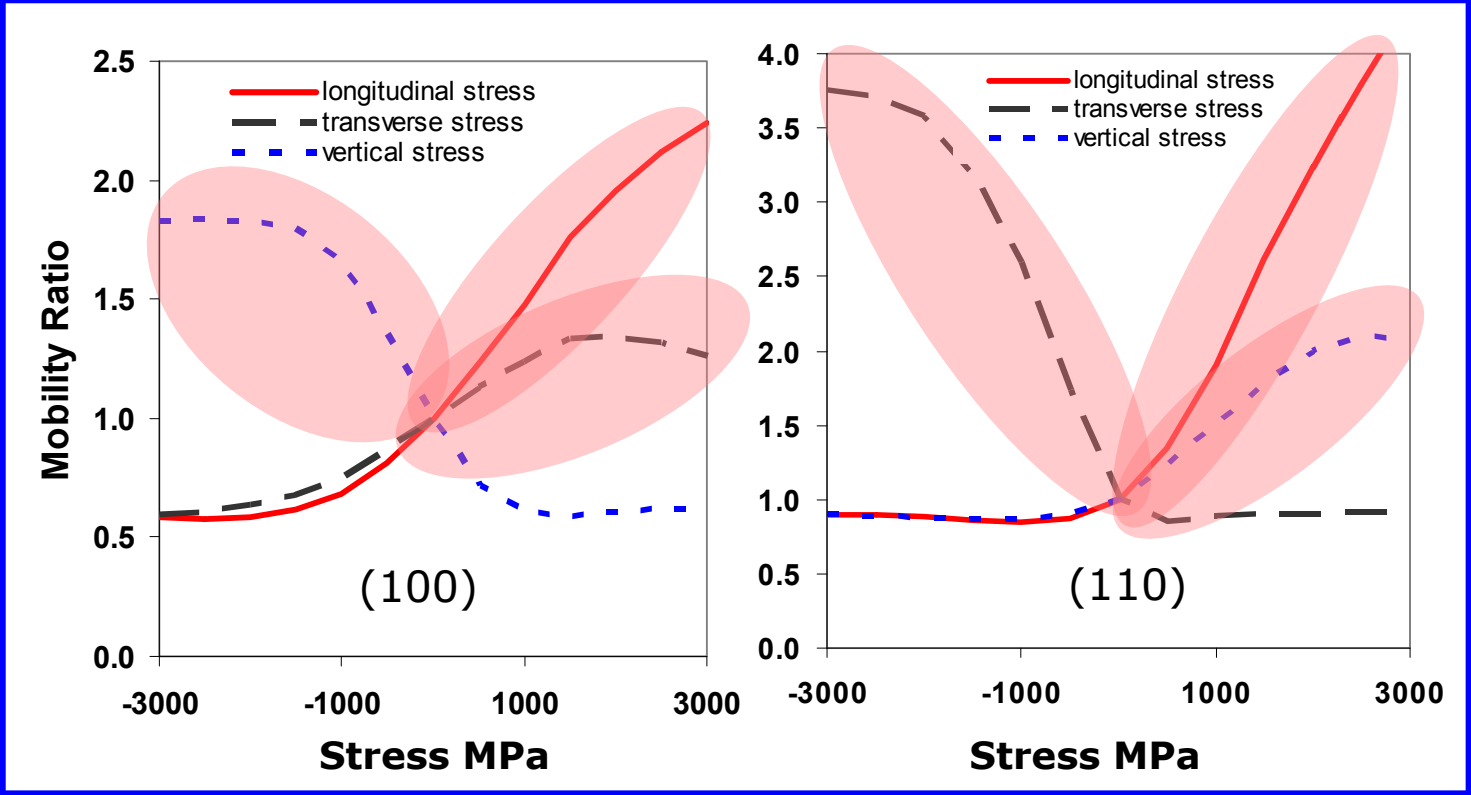
calculated using MASTAR (http://www.itrs.net/models.html)

PMOS Hole Occupation and Band Structure



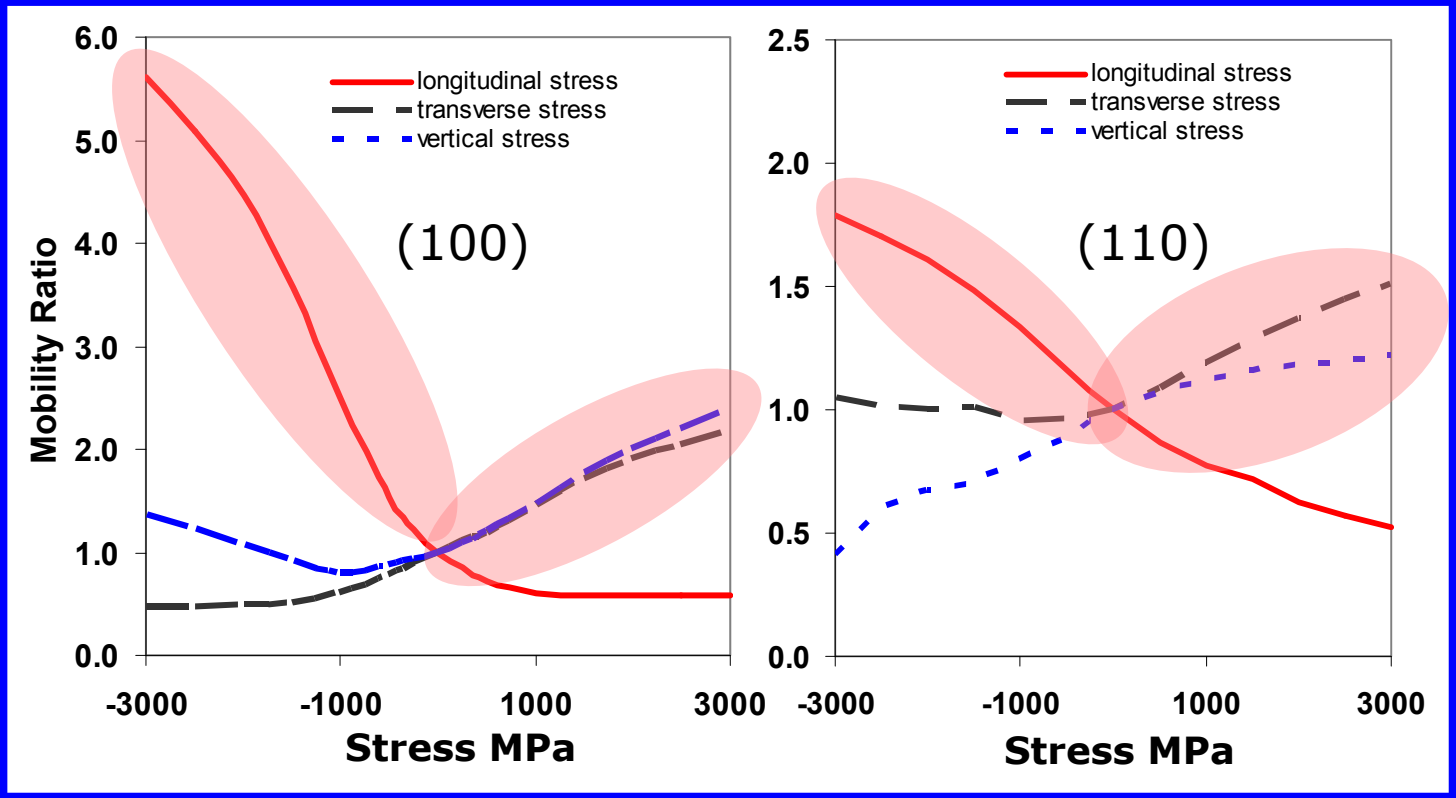
- More dense contour lines show lower effective mass for (110)
- PMOS hole occupation of band structure shows a larger difference between unstressed and stressed devices for (100)

Stress Response of Electron Mobility



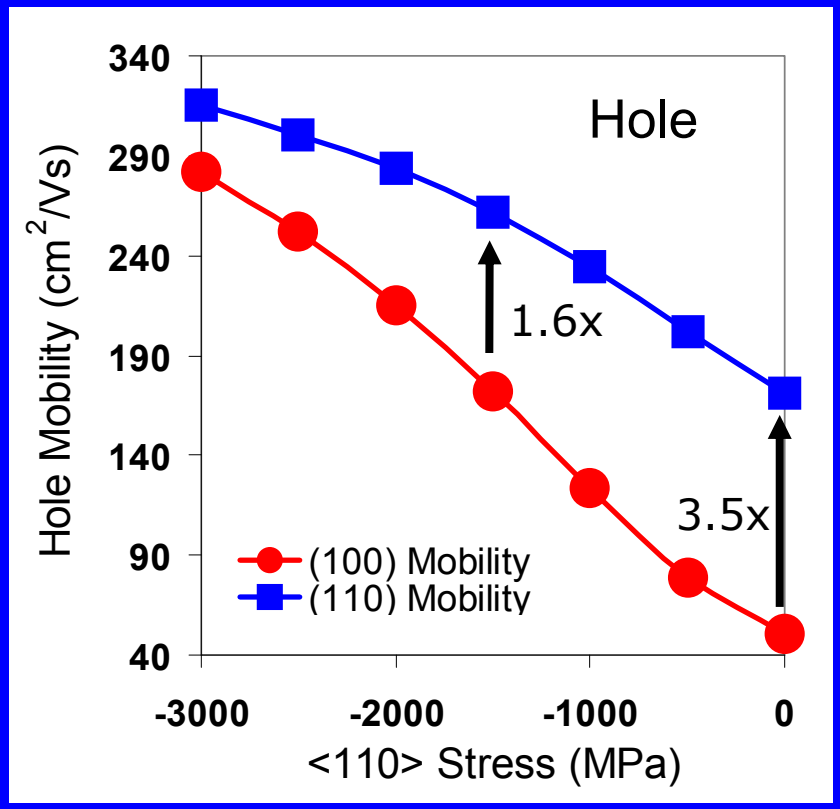
- Longitudinal tension improves (100) and (110) mobility
- Vertical and transverse stress show opposite dependencies
- Stress sensitivity is larger for (110) substrate orientation

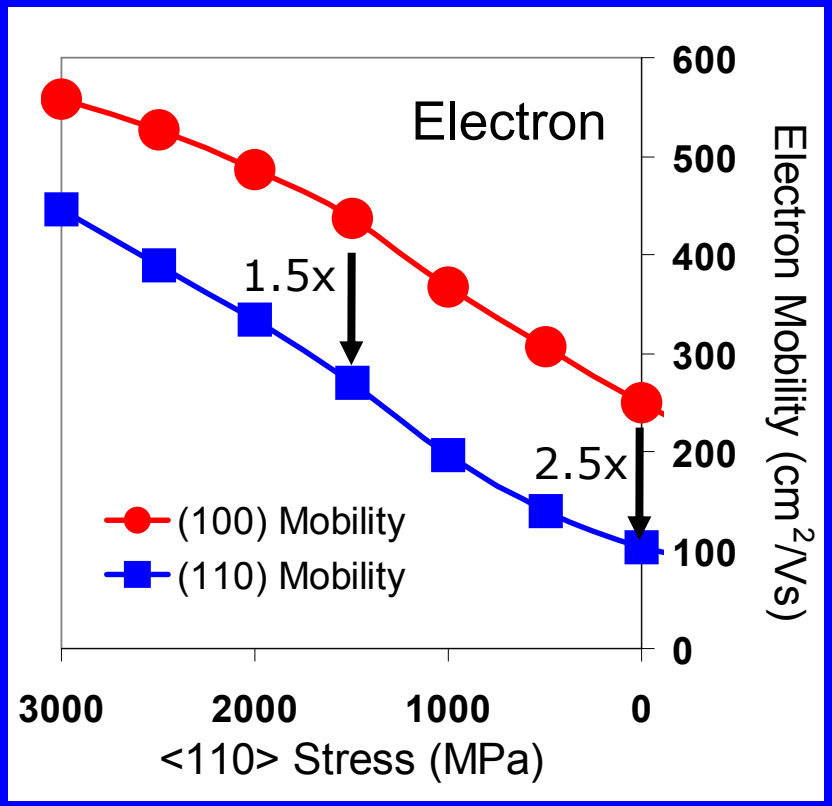
Stress Response of Hole Mobility



- Longitudinal compression improves (100) and (110) mobility
- Vertical and transverse tension improves (100) and (110) mobility
- Stress sensitivity is larger for (100) substrate orientation

Simulated Hole and Electron Mobility





- Hole mobility increases and electron mobility decreases for (110) substrates
- The difference in mobility depends on device stress

Outline

- Transistor Scaling
- Stress Effects on Mobility
- Comparison of (100) and (110) Silicon Substrates
- **Device Performance**
- Summary

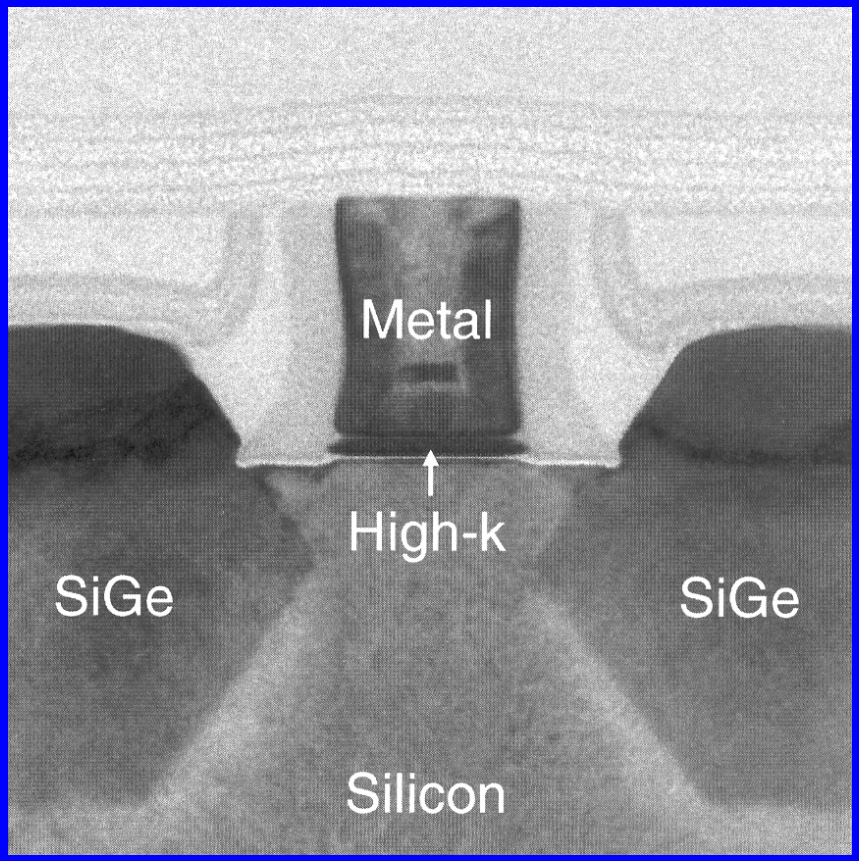
45 nm Hi-K+Metal Gate Technology

- Based on Intel's 45 nm process technology
- High-k first, metal gate last process architecture

- 35nm gate length
- 160 nm contacted gate pitch

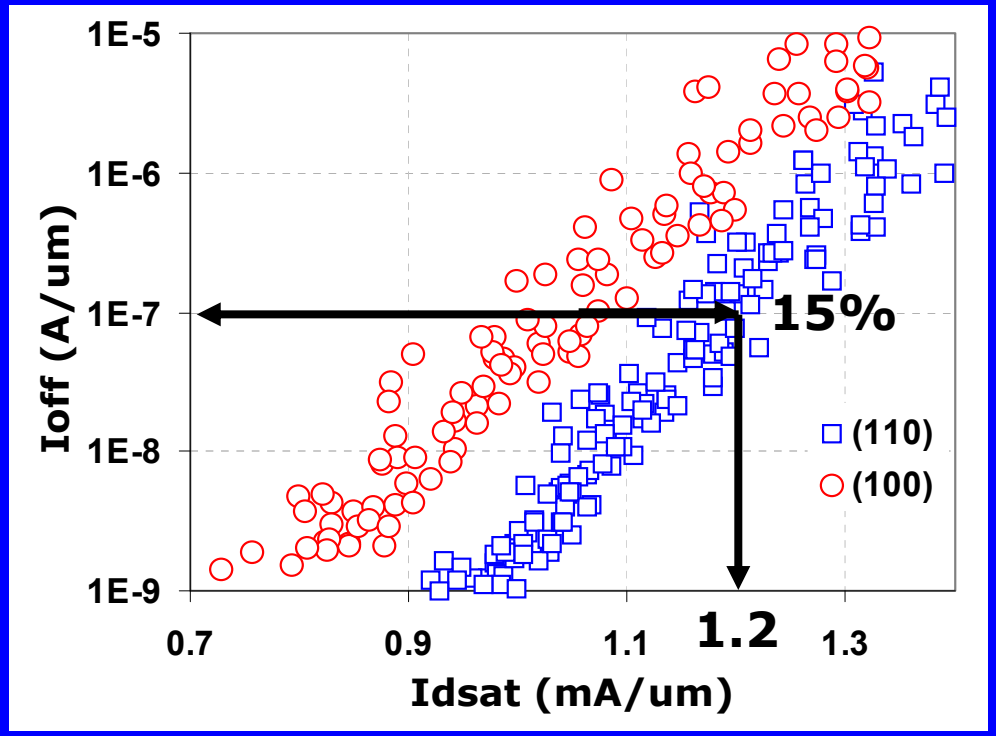
- 1.0 nm EOT High-k
- Dual workfunction metal gate electrodes

- 3RD generation strained silicon



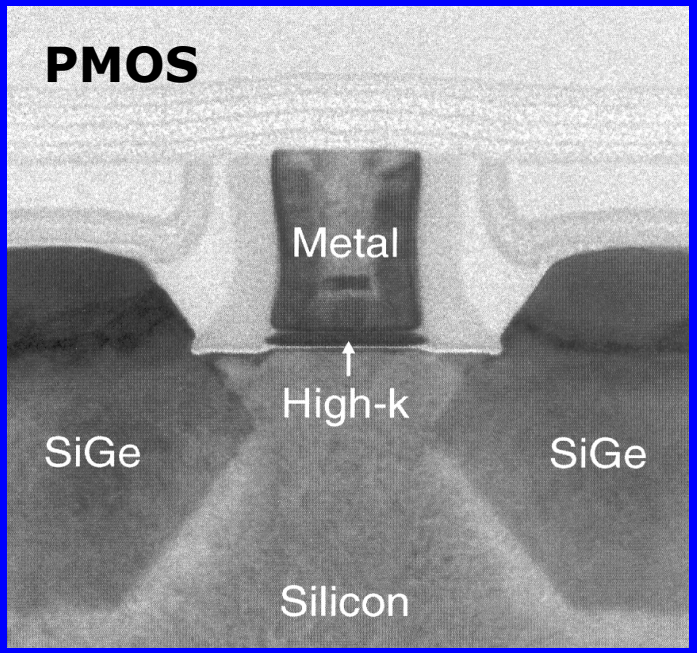
K.Mistry IEDM 2007

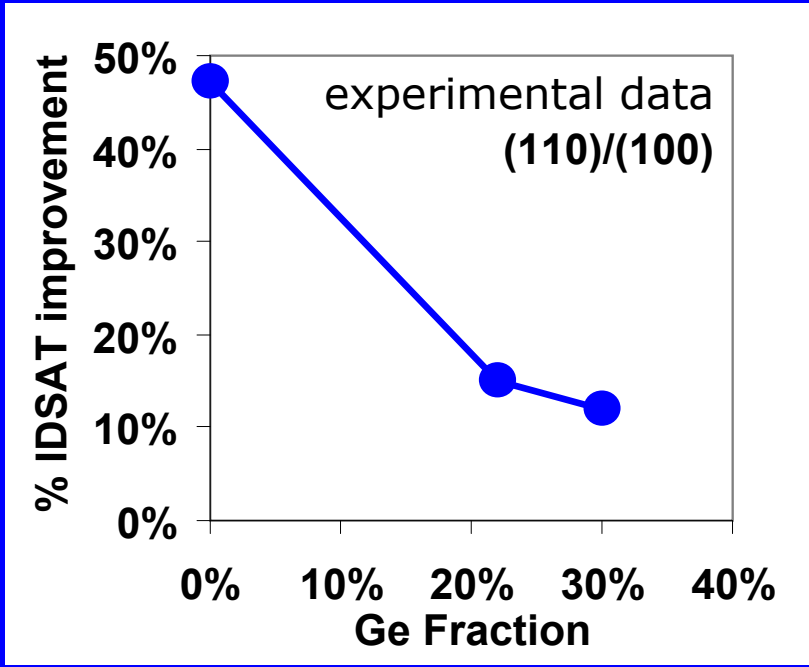
(110) and (100) PMOS Idsat



- Record PMOS drive currents of 1.2 mA/um at 1.0V and 100nA/um Ioff are reported for (110) substrates
- The performance improvement is 15% for (110) substrates compared to (100) substrates

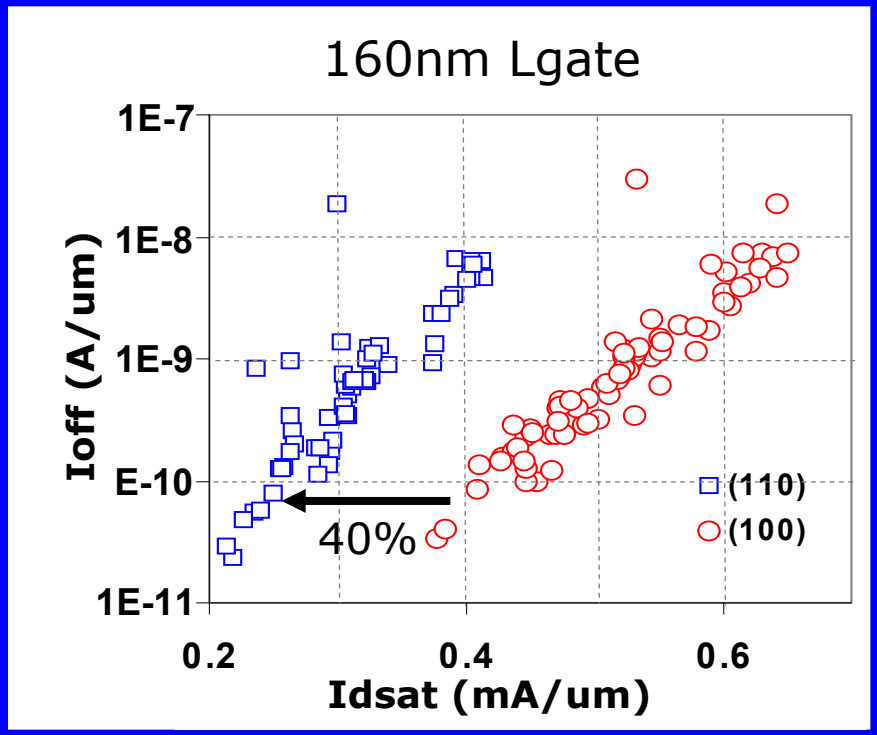
PMOS (110)/(100) Idsat Improvement versus Stress

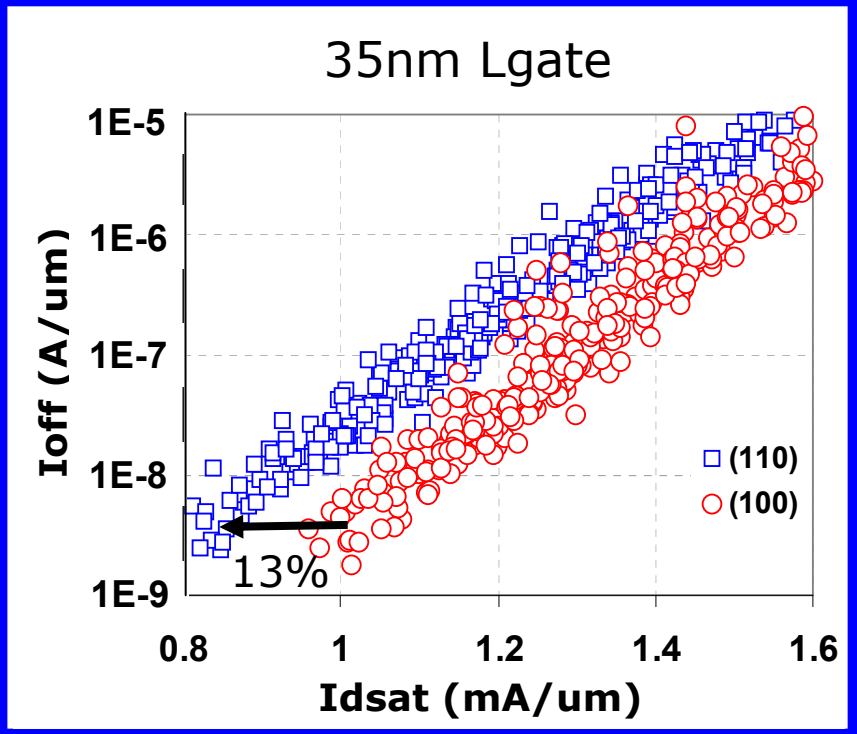




- Under stress, the relative hole mobility between (110) and (100) substrates decreases due to the larger stress sensitivity of mobility on the (100) substrate
- Even under high stress, substantial performance improvement is seen

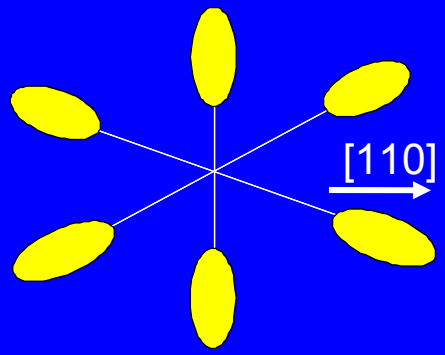
(110) and (100) NMOS Idsat





- As channel lengths are decreased, NMOS performance loss on (110) substrates is reduced
- Why is the degradation reduced?

Surface Confinement Effect

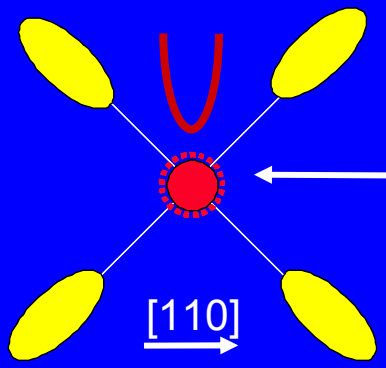


Bulk conduction

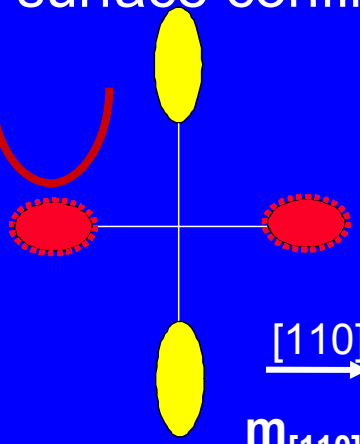
$m_{[110]}=0.43m_e$

(100) surface confinement

(110) surface confinement



Ground state

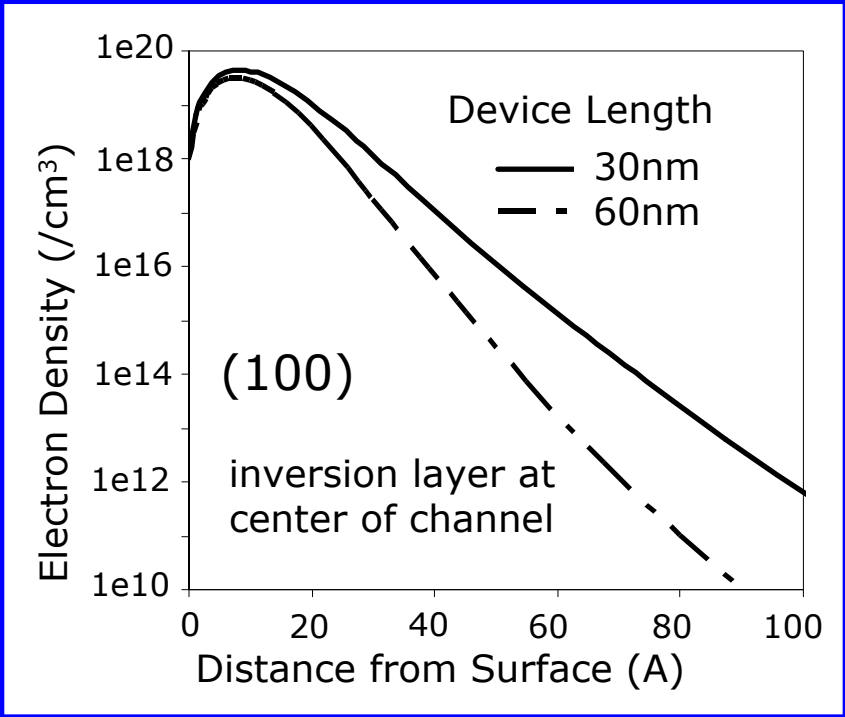


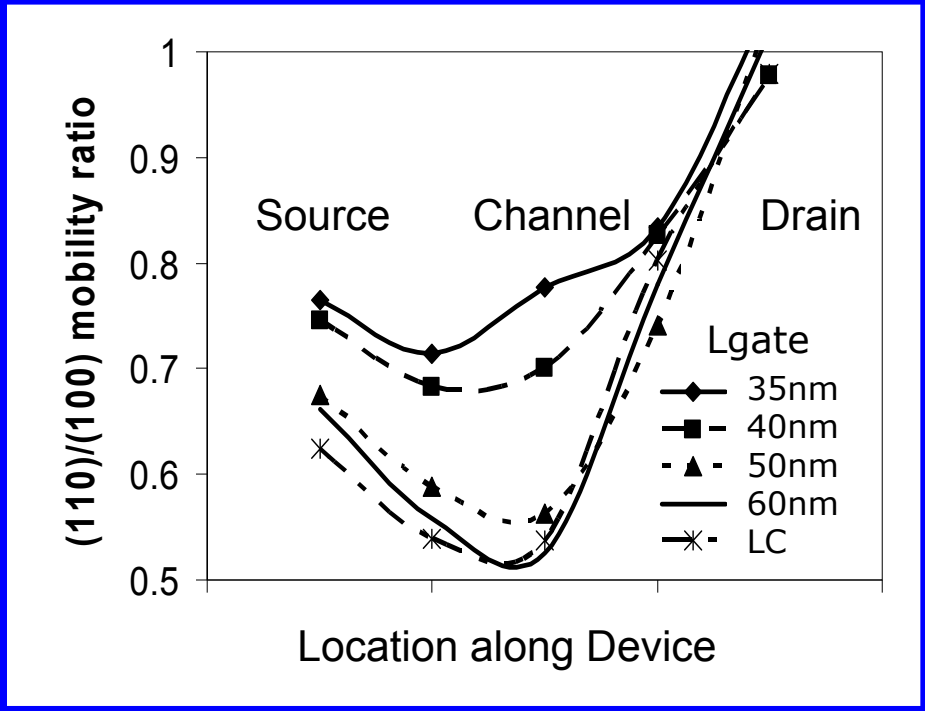
$m_{[110]}=0.19m_e$

$m_{[110]}=0.55m_e$

- Surface confinement changes ground state transport mass
- Separation depends on confinement field

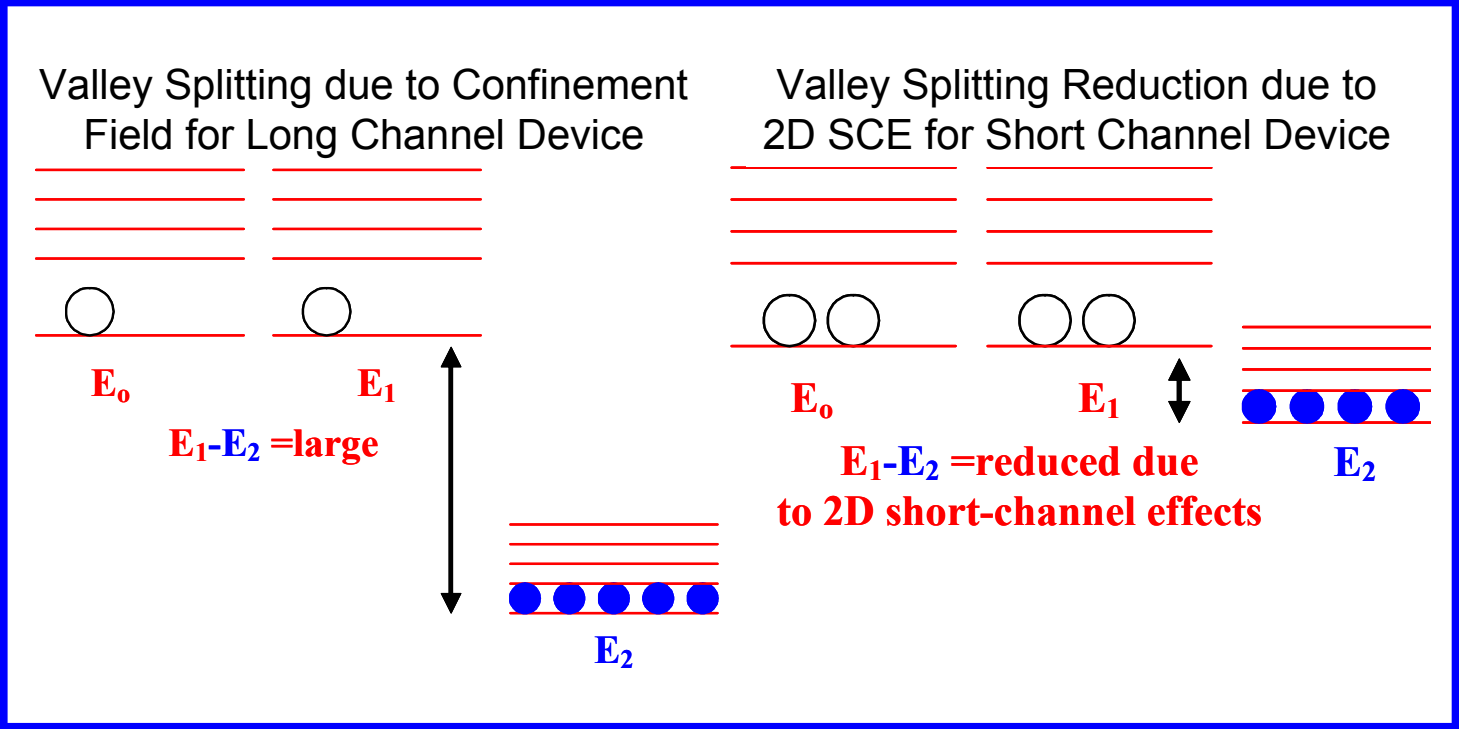
Local Electron Mobility





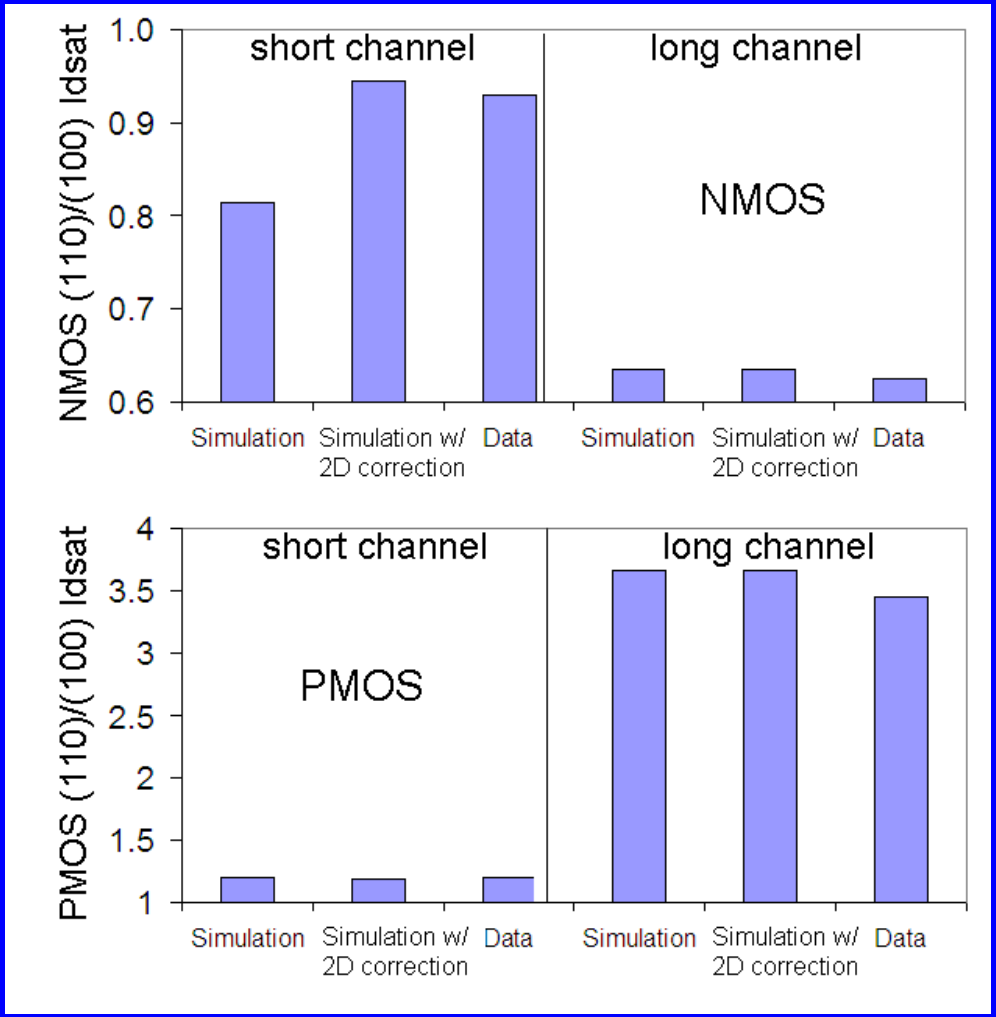
- **k·p** calculations for an unstressed device show the maximum degradation occurs near the middle of the channel
- As the channel lengths is decreases, the carrier confinement is reduced due to 2D short channel effects

2D Effects on Valley Splitting



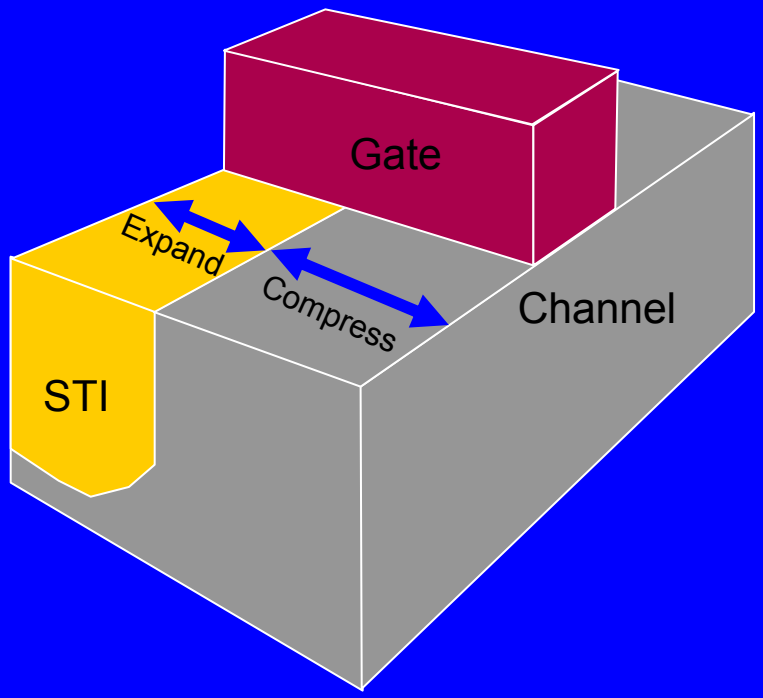
- Reduced carrier confinement in short channel devices due to 2D effects reduce the valley splitting
- This reduction results in reduced NMOS performance loss for (110) substrates

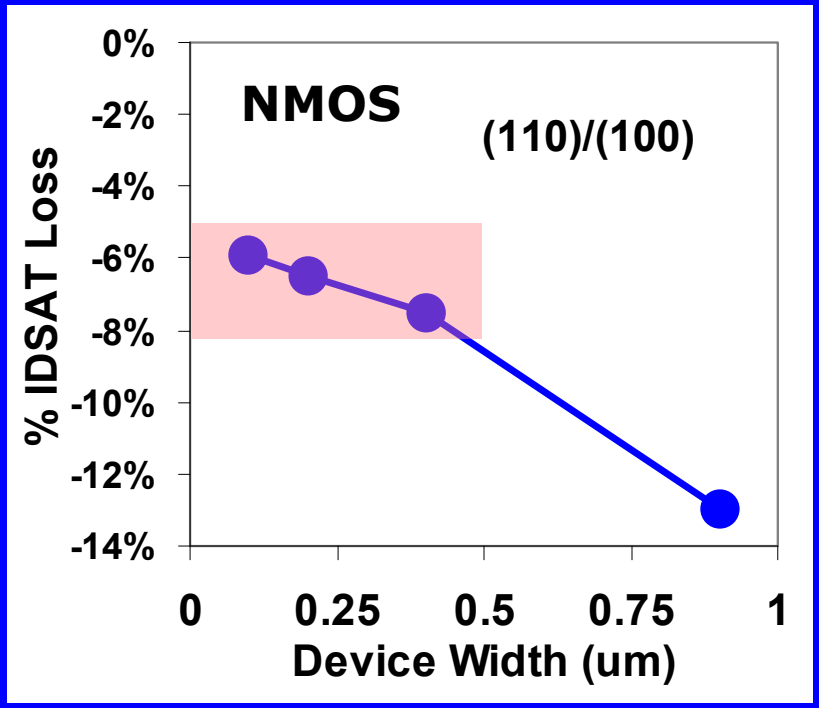
Simulated 2D Effects



- Simulated NMOS and PMOS performance both with and without 2D effects
- The NMOS devices shows a large reduction in short channel degradation when 2D effects are included
- Due to high stress effects in the PMOS device, little change is seen by including the 2D effects.

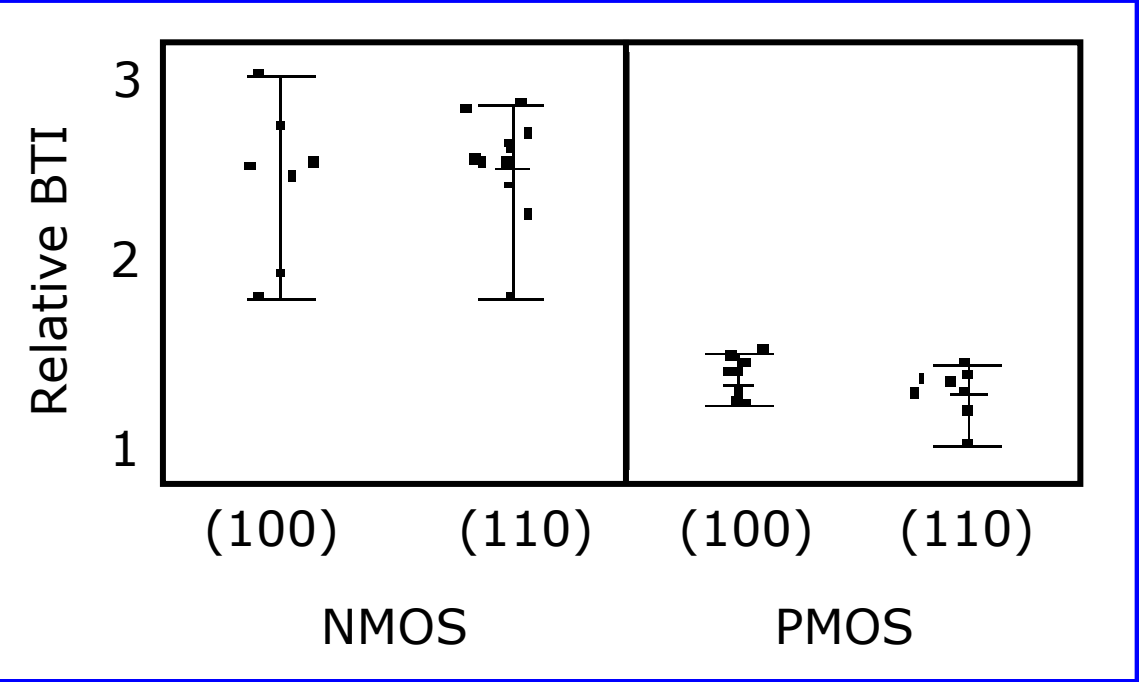
Narrow Width Stress Effects





- STI causes compressive transverse stress in the channel which increases at narrower device widths
- Transverse compression improves (110) and degrades (100) electron mobility
- NMOS performance for typical devices is only degraded by 5-8%

Reliability Data



- BTI reliability data for 45nm high-k+metal gate devices show no intrinsic difference between (100) and (110) substrate orientations

Outline

- Transistor Scaling
- Stress Effects on Mobility
- Comparison of (100) and (110) Silicon Substrates
- Device Performance
- **Summary**

Summary

- Record PMOS drive current of 1.2mA/um are shown
- PMOS drive currents on (110) substrates show a 15% performance improvement
- NMOS drive currents on (110) substrates for typical device widths are only degraded 5-8%
- The fundamental physical reason behind these behaviors is understood
- The use of (110) silicon substrates is a promising technology option

For further information on Intel's silicon technology, please visit our Technology & Research page at www.intel.com/technology