High Performance Hi-K + Metal Gate Strain Enhanced Transistors on (110) Silicon

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Abstract

For the first time, the performance impact of (110) silicon substrates on high-k + metal gate strained 45nm node NMOS and PMOS devices is presented. Record PMOS drive currents of 1.2 mA/um at 1.0V and 100nA/um Ioff are reported. It will be demonstrated that 2D short channel effects strongly mitigate the negative impact of (110) substrates on NMOS performance. Narrow width (110) device performance is shown and compared to (100) for the first time. Device reliability is reported showing no fundamental issue for (110) substrates.

Introduction

As traditional device scaling is facing increasingly difficult challenges, novel solutions are enabling continued performance scaling. One key to the continued performance improvements has been strain engineering for mobility improvement. In recent years, embedded SiGe, stress capping films and stress memorization have been used in the industry for performance improvement [1-6]. Another potentially attractive method for increasing mobility is the use of different Si substrate orientations. In particular, the use of (110) substrates for PMOS device improvement is being given considerable attention [2-4]. This paper will present for the first time PMOS and NMOS performance results for high-k + metal gate devices on (110) silicon substrates in the <110> direction including short channel, narrow width and reliability effects.

Background

Figure 1 shows the electron and hole mobility as a function of stress in the transport direction for long channel NMOS and PMOS devices for (100) and (110) substrates. Simulations are based on 6-band **k·p** Luttinger Hamiltonian calculations [7]. With no applied stress, a 2.5x reduction in electron mobility and a 3.5x enhancement in hole mobility is seen for the (110) substrate. Under compressive stress, the relative hole mobility improvement decreases as the (100) substrate has a larger sensitivity to stress due to the band structure (Fig. 2). Figures 3 and 4 show simulations of the electron and hole mobility response to longitudinal, transverse and vertical stress for (100) and (110) substrates. Due to band structure differences, the mobility response to longitudinal, transverse and vertical stress can be quite different for the different cases. For example, transverse compressive stress will reduce electron mobility for (100) and improve mobility for (110) substrate orientations.

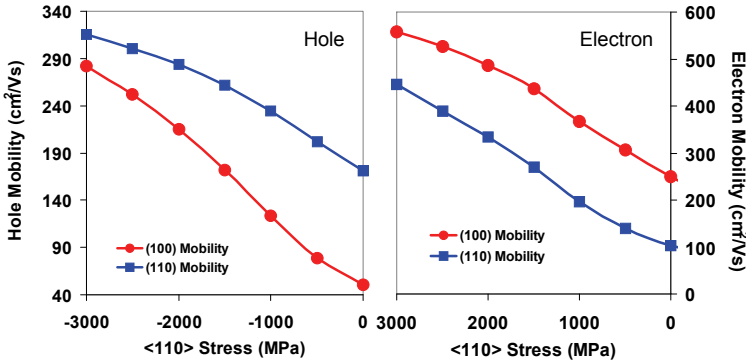

Fig. 1 – Simulated hole and electron mobility for (100) and (110) silicon substrates as a function of stress.

Results

A 45nm node technology high-k + metal gate process flow similar to one presented previously [5,6] was used to fabricate PMOS and NMOS devices on (110) substrates in the <110> transport direction. Figure 5 shows an Ioff vs. Ion curve for a 160nm Lg NMOS device on (100) and (110) substrates. As expected from the mobility calculations, there is a degradation in drive current. However, the drive current degradation is significantly less than the mobility degradation observed in Fig. 1. Figure 6 shows the Ioff vs. Ion curve for a 35nm Lg NMOS device. Again, Idsat degradation is observed but its magnitude is only 13%, even less than the 160nm Lg device. Figure 7 shows the same Ioff vs. Ion plot for a 35nm Lg uniaxial strained 22% embedded

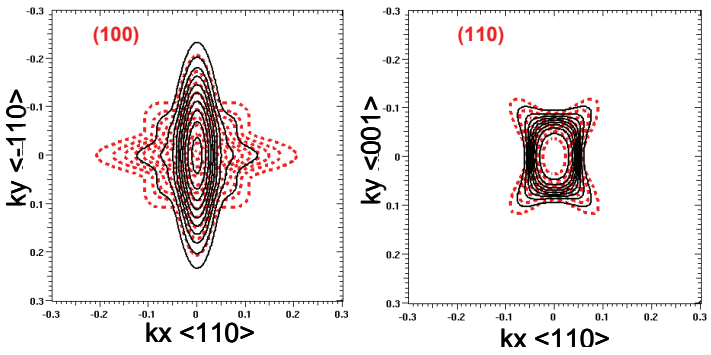

Fig. 2 – PMOS hole occupation of band structure and stress response for (100) and (110) substrate orientations. Dashed lines represent no stress and solid lines represent with applied stress.

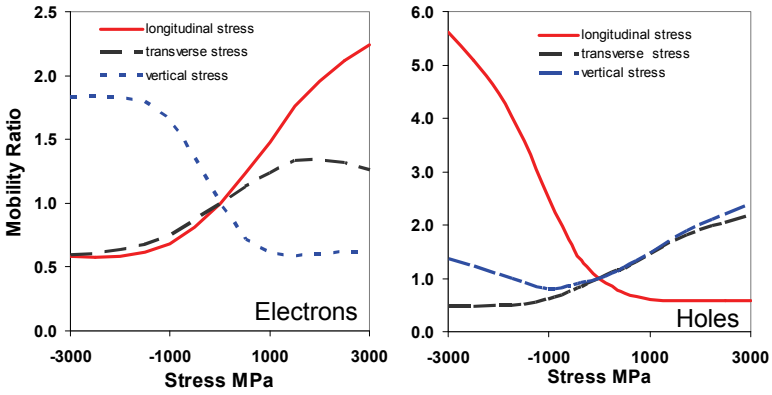

Fig. 3 – Normalized electron and hole mobility ratios for longitudinal, transverse and vertical stress for (100) silicon.

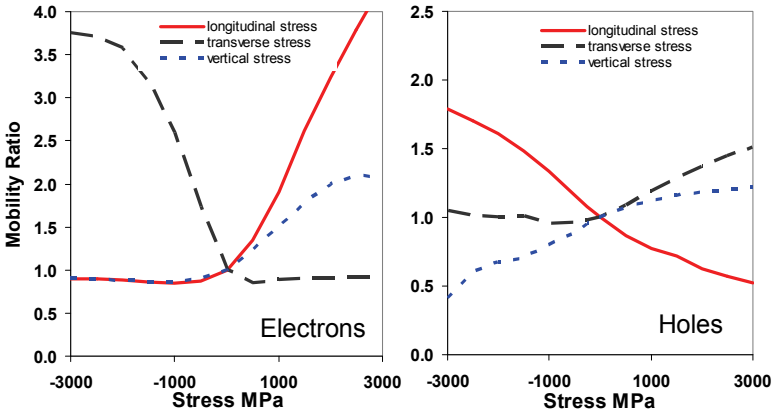

Fig. 4 – Normalized electron and hole mobility ratios for longitudinal, transverse and vertical stress for (110) silicon.

SiGe (eSiGe) PMOS device [5]. For the PMOS case, the (110) substrate orientation shows a 15% Idsat improvement and demonstrates a record 1.2 mA/um drive current at 1.0V and 100nA/um Ioff. This is in agreement with the mobility trend seen in Fig. 1 but again, lower in magnitude. Figure 8 shows PMOS Idsat as a function of Ge concentration for uniaxial strained eSiGe [5].

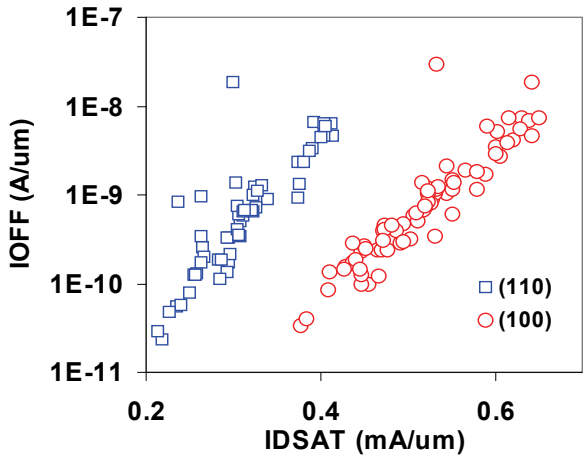

Fig. 5 – NMOS Ioff vs. Idsat for (100) and (110) substrates for a 160nm Lg device showing a 40% Idsat reduction.

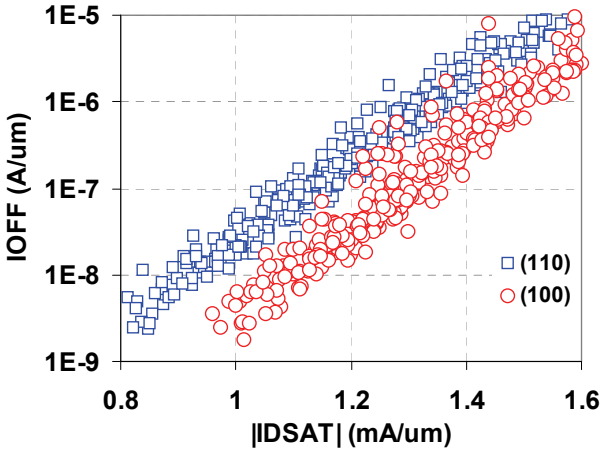

Fig. 6 – NMOS Ioff vs. Idsat for (100) and (110) substrates for a 35nm Lg device showing a 13% Idsat reduction.

As expected from Fig. 1, there is a reduction in the enhancement of the (110) substrate compared to the (100) substrate as the compressive stress is increased. This reduction is consistent with amount of strain generated by the uniaxial eSiGe structures and Fig. 1. Figure 9 shows the effect of 35nm Lg NMOS device width on Idsat degradation for (110) versus (100) substrates. As the width of the device is reduced, the Idsat degradation also reduces going from 13% degradation for a 0.9um wide device to 6% for a 0.1um wide device.

Discussion

As seen in Figs. 5 and 6, as the gate length is reduced for the NMOS devices the Idsat degradation of (110) compared to (100) is reduced. This effect can be explained by 2D short channel effects as seen in **k·p** calculations. Figure 10 shows this effect schematically. As the channel length is reduced, 2D source-drain electrostatics lead to a reduction in charge confinement in the channel. This reduction in confinement reduces the valley splitting at shorter channel lengths lowering the anisotropy and reducing the differences between (110) and (100) substrates.

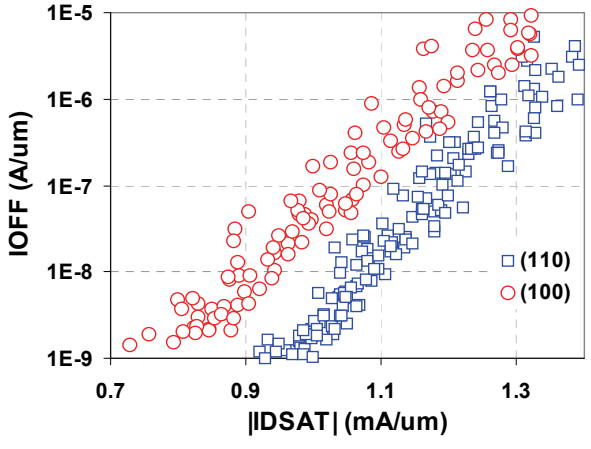

Fig. 7 – PMOS Ioff vs. Idsat for (100) and (110) substrates for a 35nm Lg device showing a 15% performance improvement.

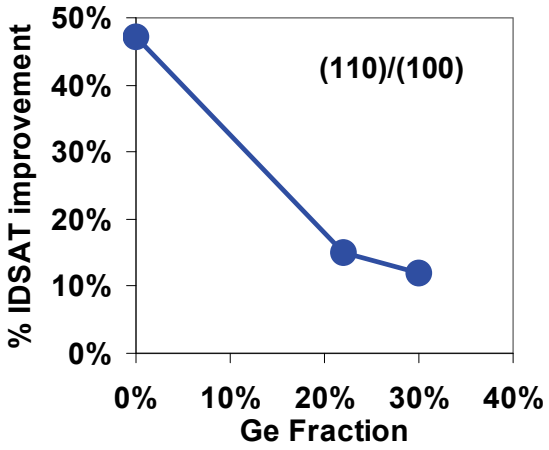

Fig. 8 – Measured PMOS Idsat improvement for (110) vs. (100) substrates as a function of uniaxial stress generated by eSiGe.

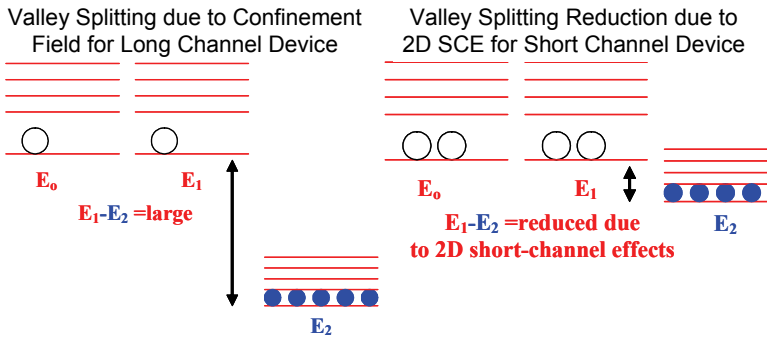

Fig. 10 – Schematic representation showing the reduction in valley splitting for short channel (100) devices. E0, E1 and E2 represent the X, Y and Z valleys. This reduction results in reduced NMOS performance degradation for smaller devices.

In Fig. 11, this 2D effect is taken into account by using **k·p** calculations for vertical slices across the channel to calculate a mobility scaling factor for each point in the channel, source and drain region. This scale factor determines the local mobility which is then used in the device simulations. As seen, this method accurately matches the experimental data for both long and short channel devices. The reduction in NMOS Idsat degradation for (110) devices at narrower widths (Fig. 9) is a direct result of (110) and (100) electron mobility response to transverse stress. As the channel width is narrowed, the effect of the isolation region stress increases. The influence of the transverse stress generated by the isolation improves the (110) mobility and reduces the (100) mobility (Figs. 4 and 5). Finally, electrical bias temp stress measurements at 125°C show no intrinsic difference between (100) and (110) substrate orientations (Fig. 12).

Conclusion

The effects of (110) substrate orientation for 45nm node high-k+metal gate strained devices have been presented for the first time. Record PMOS device performance of 1.2 mA/um at 1.0V and 100nA/um Ioff have been shown. 2D confinement interactions reduce the negative performance impact of NMOS devices at short gate lengths. Stress effects reduce the NMOS (110) degradation for narrow width devices. Finally, no intrinsic reliability issues are seen with (110) substrate orientations.

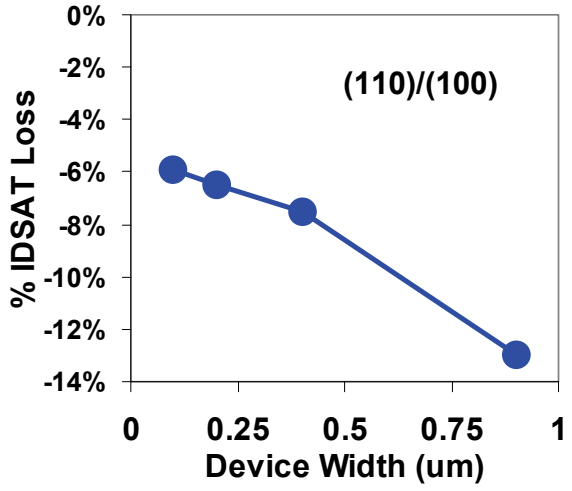

Fig. 9 – Measured NMOS Idsat reduction as a function of device width. Narrower devices show less degradation due to transverse stress interactions.

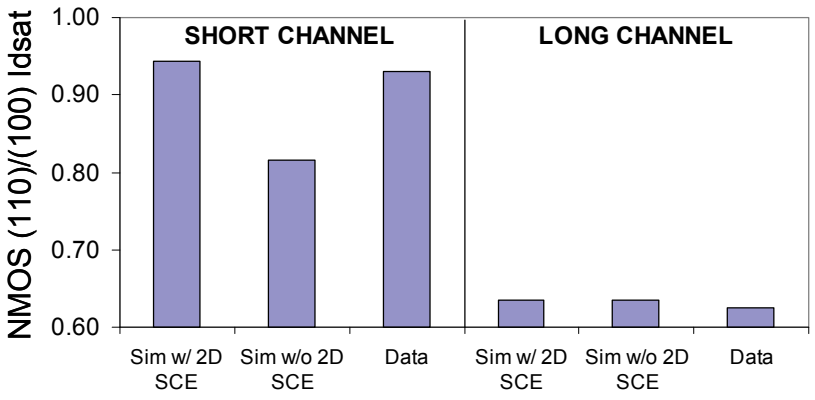

Fig. 11 – NMOS performance degradation simulations both with and without 2D effects. Simulations for 2D effects use multiple device slices where **k·p** and Schrödinger simulations are done.

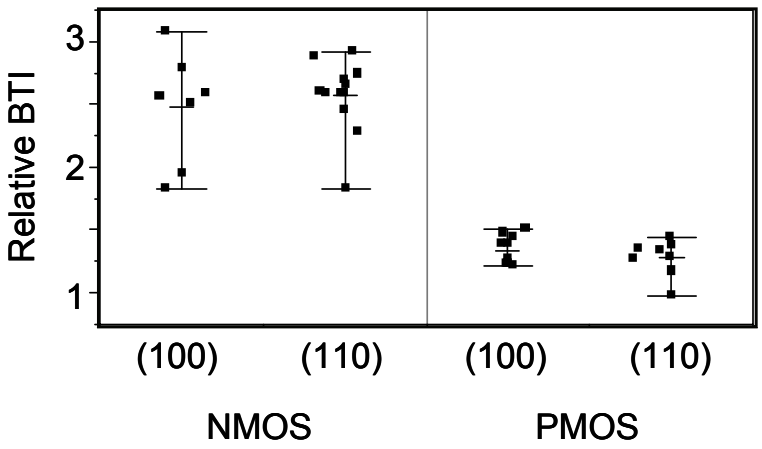

Fig. 12 – BTI reliability data for 45nm (110) high-k+metal gate devices. These results show no intrinsic issue with (110) device reliability.

References

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