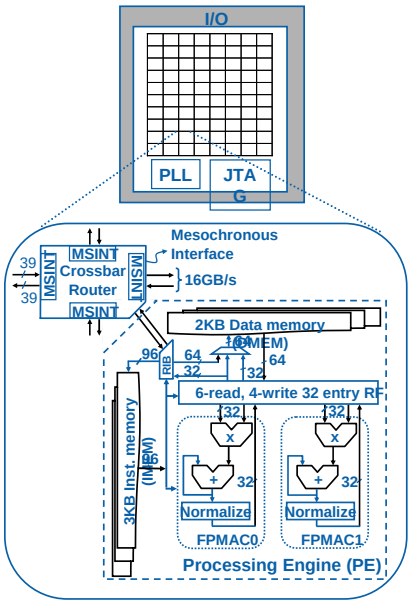
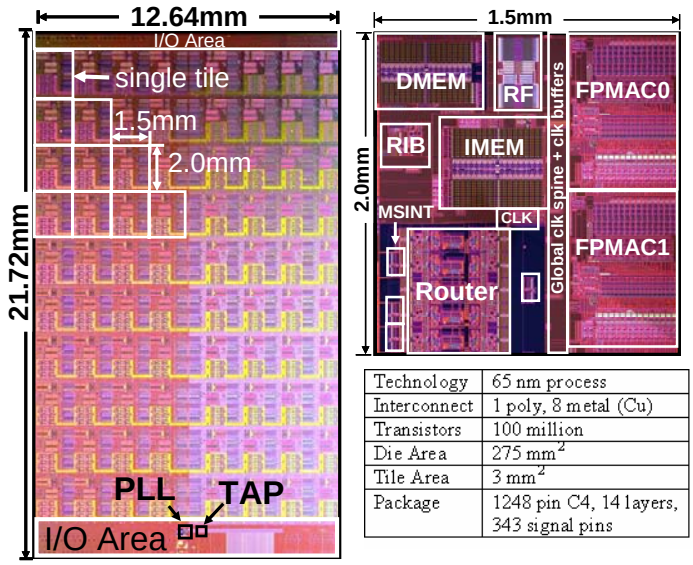
80 core Teraflops Research Processor

First tera-scale silicon prototype

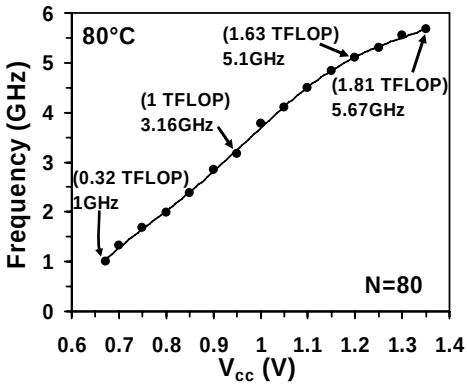


Tiled architecture

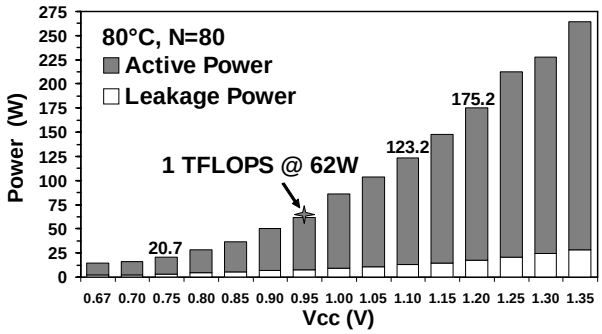


Technology	65 nm process
Interconnect	1 poly, 8 metal (Cu)
Transistors	100 million
Die Area	275 mm^2
Tile Area	3 mm^2
Package	1248 pin C4, 14 layers, 343 signal pins

Chip micrograph and characteristics



Measured frequency with peak teraflops



Measured power with peak teraflops

Key Features

- ✧ 80 tiles connected in a 2D mesh
- ✧ Single precision FPMAC cores
- ✧ Non-blocking double-pumped crossbar router w/ 6 ports, 2 VCs
- ✧ Dynamic power management
- ✧ 1.01 teraflops @ 0.95V, 62 W
- ✧ 19.4 gigaflops @ 0.75V

Research at Intel

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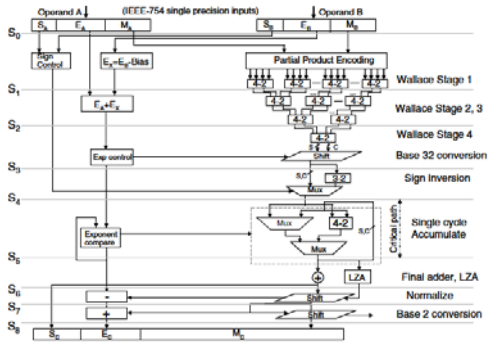
Compute Core

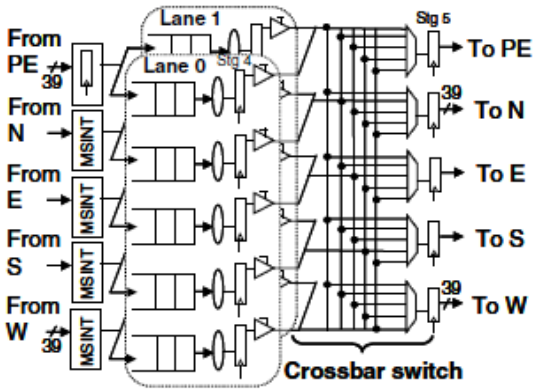
★Single Precision FPMAC engine.
- ✧Fast single-cycle accumulate loop.
- ✧Sustained throughput: 2FLOPS/cycle



FPMAC engine

On-die Interconnect

★ 2-dimensional mesh
- ✧ Scalable, reconfigurable, partitionable, power-aware
- ✧ 1.62 Terabits/s bisection BW 75 GB/s aggregate BW



Router

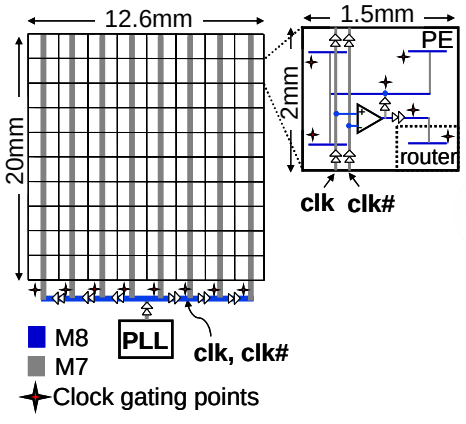
Power Management

★ Mesochronous clocking
- ✧ Scalable, low-power Dynamic sleep instructions
- ✧ Put FP engine or tile to sleep

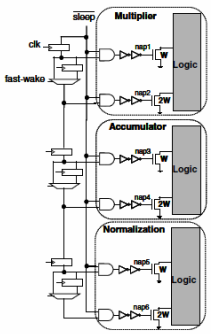
★ Memory clamping circuits
- ✧ Retain state in arrays in sleep

★ Sleep transistors
- ✧ 6x standby leakage reduction

★ Voltage and frequency control



Mesochronous clocking



FPMAC wakeup

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